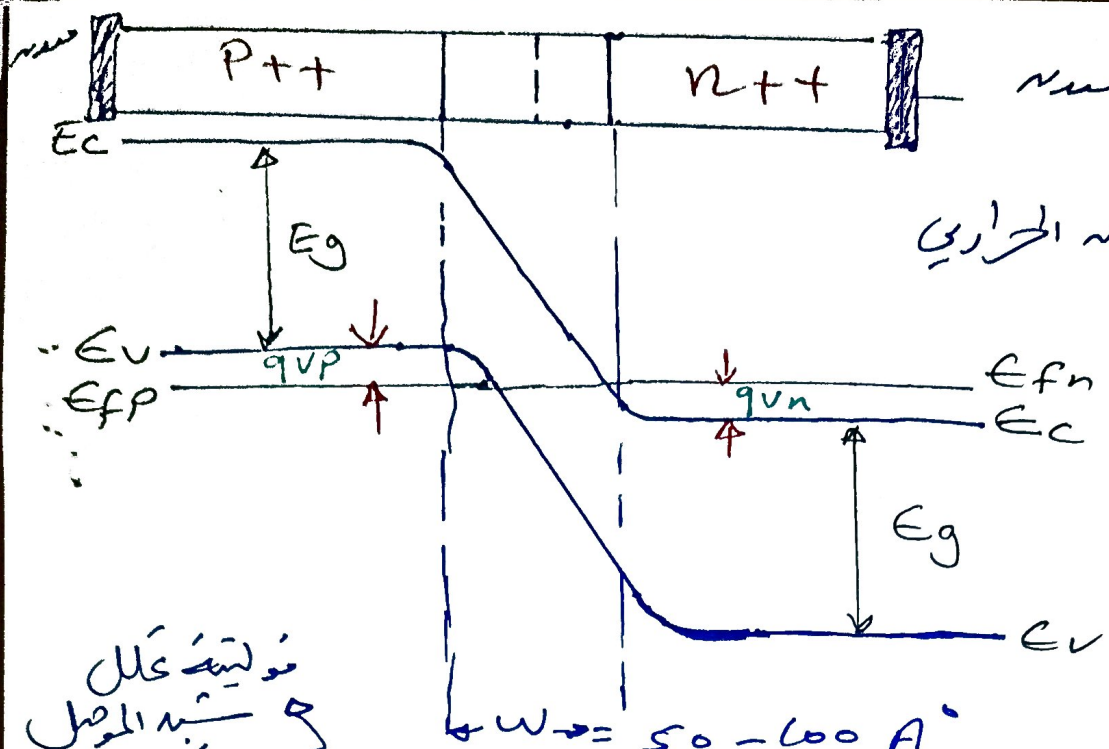
Lectures of Electrical Engineering Department

Subject Title: Microelectronics

Class: 4th Electronic and Communications

Lecture Contents	**Lecture sequences:**	**First lecture**	**Instructor Name:**
	The major contents: **1- Tunnel Diode** **2-** **3-** **4-**		
	The detailed contents: **1- Working principle** **2- Characteristics** **3- Applications**		

اسم التدريسي: F.H. Aldabbagh & Firas عنوان البريد الاليكتروني f.h.aldabbagh@uomosul.edu.iq



حالة الاتزان الحراري
لا يوجد
Biasing

فولتية حاجز
سد الموصل
نوع P

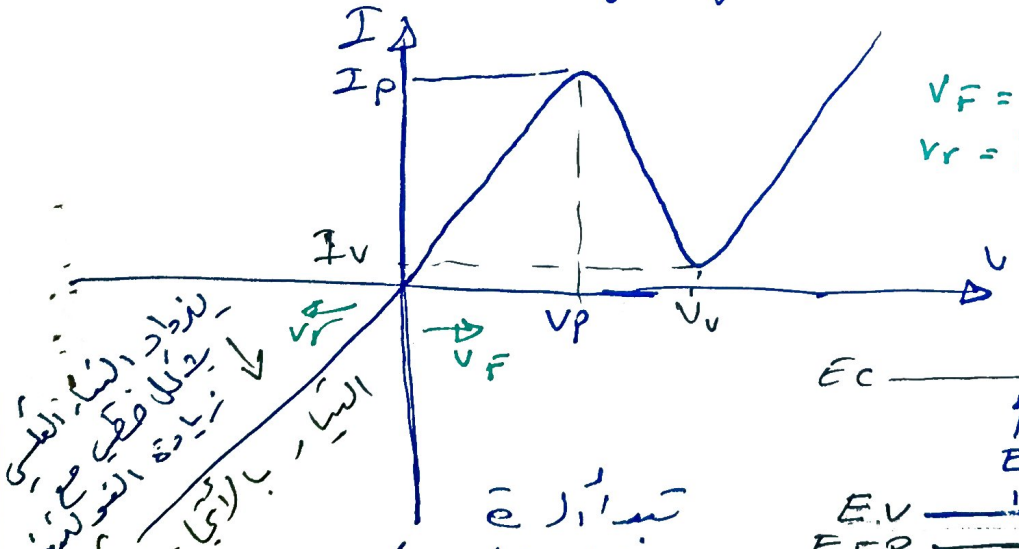
$$V_p = \frac{|E_v - E_{FP}|}{e} \cong 50 - 100\ mV$$

فولتية حاجز
سد الموصل
نوع N

$$V_N = \frac{|E_{Fn} - E_c|}{e} \cong 50 - 100\ mV$$

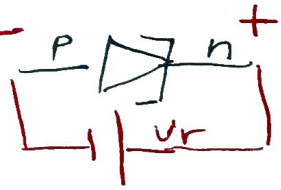
$q V_n = e V_n$ ← $e = q$ = شحنة الالكترون

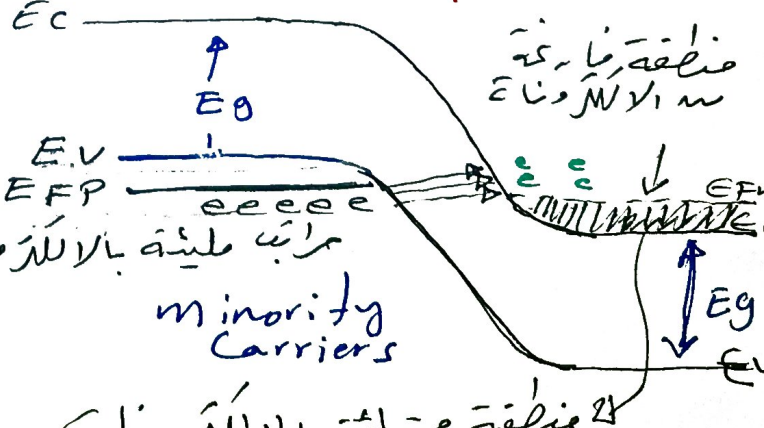
Reverse Biasing of Tunnel diode



V_F = فولتية امامية
V_r = فولتية عكسية

E_{Fn} ينزل
يصعد E_{FP}

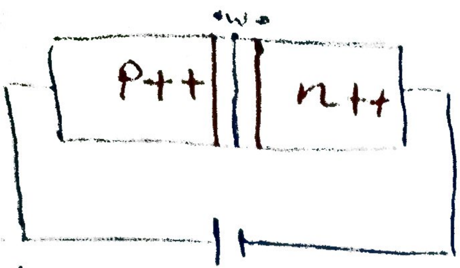




تيار النفق (الجور)
n++ و P++
مناطق ممتلئة بالـ e
مناطق خالية من e

تيار الانتشار

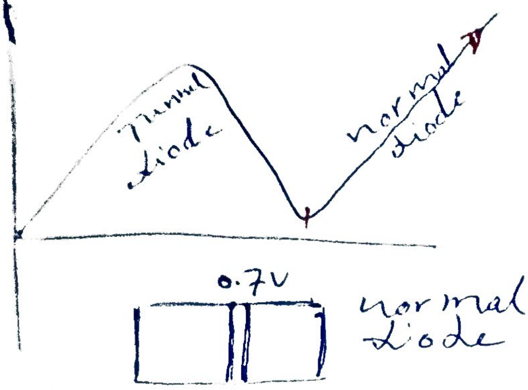
Tunnel Diode: pn junction — 1957 Esaki diode

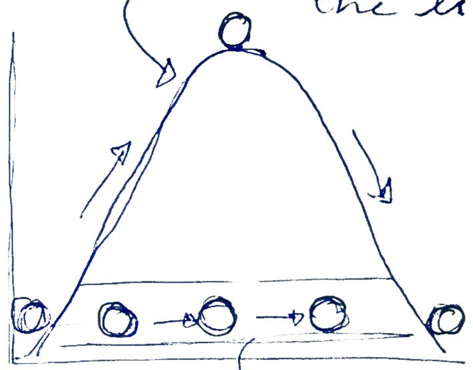


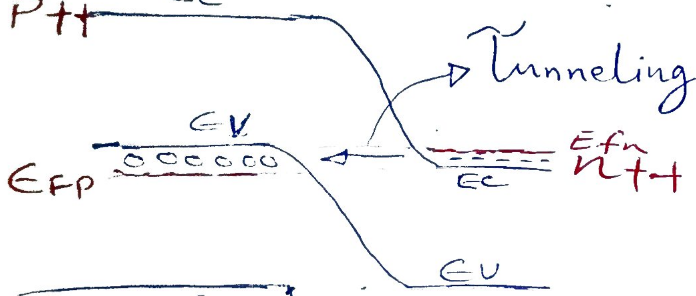
w = 50 – 150 A°

→ highly dopped
↓
→ large no. of impurity
↓
Degenerate semiconductors
more like a metal

P —▷|— n
Anode Cathod







$E_{fp} = E_{fn}$

$V_p = \frac{|E_v - E_{FP}|}{e}$

$V_N = \frac{|E_{fn} - E_c|}{e}$

p++ | n++

Efn - - - - -
Ec ——— Ec
Ev ——— Ev
EFP - - - - -

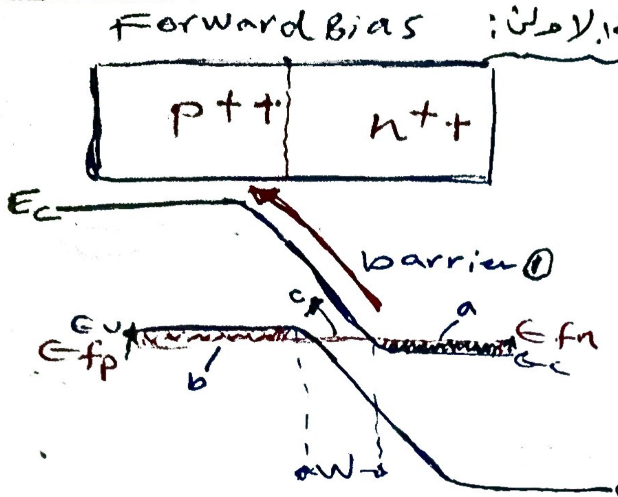
n++ ——— Efn
Ec ———
n+ ——— Efn
n ——— Efn

Ei ———

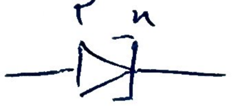
p ——— EFP
p+ ——— EFP
EV ———
p++ ——— EFP

إذا كان الدايود من نوع n فيكون مستوى
فيرمي قريب من الـ Ec ، وإذا كان مستوى
فيرمي قريب جداً فيسمى n+
وإذا كان فوق الـ Ec فيسمى n++
حيث يكون طاقة عالية degenerated

Forward Bias : الحالة الاولى

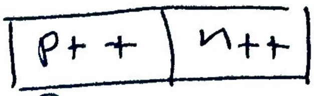


Forward - Bias

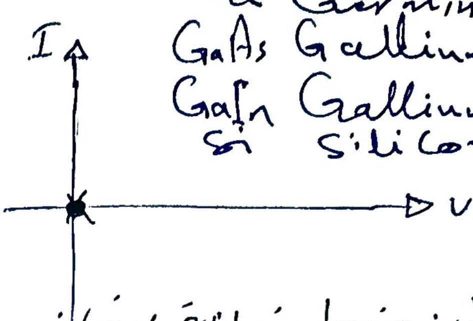


0V

المواد المصنعة من Tunnel diode



Ge Germanium
GaAs Gallium Arsenide
GaSb Gallium Antimonide
Si Silicon



في الحالة الاولى: عندما فولتية الانحياز الامامي للدايود النفقي = صفر نلاحظ ان Efn هو أعلى بقليل من Ec اي في n وان Efp هو أقل بقليل من Ev اي في p

لماذا ؟!

السبب هو نتيجة التطعيم العالي (الكبير) لمنطقة n ومنطقة p

وهذا الدايود مصنع بطريقة خاصة اي ان تطعيم n وتطعيم p كبير جداً، لذلك نتيجة التطعيم العالي يحدث ما يسمى بالتحلل او الانحلال يعني عندها سيصبح شبه الموصل متحلل

أي بمعنى سيصبح شبه الموصل معدن (تقريباً) = شبه معدن ويمتلك عندها ايصالية عالية جداً

(متحلل = خروج Efn من المكان الطبيعي لها وهو تحت Ec، خروجها الى أعلى Ec)

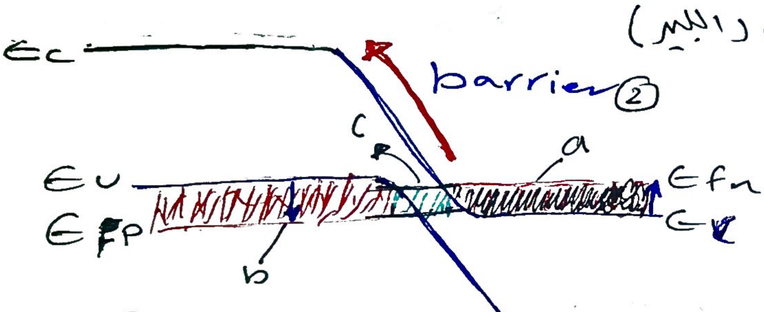
(متحلل = خروج Efp من المكان الطبيعي لها وهو فوق Ev، خروجها الى اسفل Ev)

منطقة a تكون ممتلئة بالـ e ⟵ Efn Ec

منطقة b تكون ممتلئة بالفجوات ⟵ Ev Efp

نلاحظ المنطقة c تفصل بين a و b ولا يوجد تقابل او تناظر بينهم، فولتية مسلطة = 0V

حالة الثانية :



FV = V1

يصعد Efn
ينزل Efp

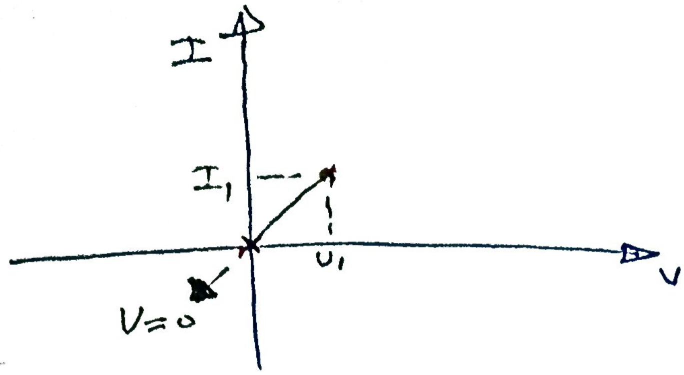
في الحالة الثانية: عند تسليط فولتية أمامية بمقدار معين V>0 أو نسميه V1 نلاحظ بأن Efn يرتفع قليلاً الى الأعلى وان Efp ينزل قليلاً الى الاسفل

عرض منطقة a حالة ثانية أكبر من عرض منطقة a حالة اولى

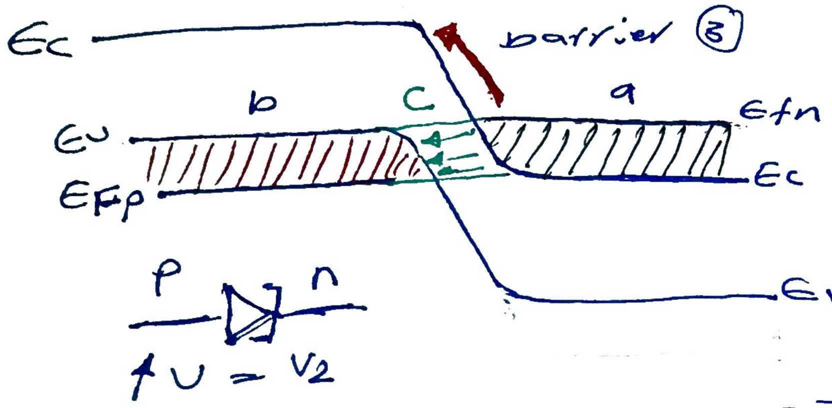
لماذا ارتفعت E_{fn} الى الأعلى
ولماذا انخفضت E_{fp} الى الأسفل
في حالة تسليط فولتية قليلة (V_1) ؟!
لأنه بتسليط الفولتية الأمامية
سوف يقل الجهد الحاجز
وبالتالي ترتفع a وتنخفض b
وأيضاً في هذه الحالة (الثانية)
سنلاحظ هناك تقابل أو تناظر قليل
بين منطقة a ومنطقة b

وعندها سيتشكل طريق او نفق
بين a و b عبر c
يسمح بعبور أو مرور
جزء من الالكترونات من المنطقة
n الى المنطقة p
وتعرف هذه العملية بالتنفيق
Tunneling

شروط عملية التنفيق Tunneling
1- يجب ان يكون عرض منطقة الاستنزاف قليل جداً.
2- يجب ان يكون هناك تناظر أو تقابل بين منطقة a و b (حتى ولو يكون جزئياً) لكي تتمكن من تنفيق الـ e من n ← p
وهذا التناظر يحدث عند تسليط فولتية بالاتجاه الأمامي
3- وجود مراتب من الطاقة مشغولة بالـ e عند الطرف n
وكذلك وجود مراتب من الطاقة مشغولة بالفجوات عند الطرف p.



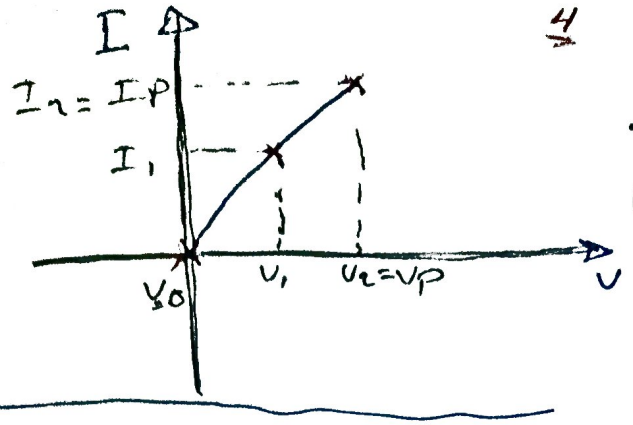
الحالة الثالثة :



barrier(1) > barrier(2) > barrier(3) > barrier(4)

في هذه الحالة (الثالثة) تقوم بزيادة الفولتية المسلطة بالاتجاه الأمامي بمقدار معين $V > V_1$ أو تسمى V_2
نلاحظ بأن E_{fn} ارتفع أكثر من الحالة السابقة (الثانية) أي ارتفع الى الأعلى
وكذلك فأن E_{fp} انخفض أكثر من الحالة السابقة (الثانية) أي انخفض الى الأسفل
عرض منطقة a و b أكبر من عرض منطقة a و b
بالحالة الثانية ← بالحالة الاولى
والسبب في ذلك معروف، لأننا قمنا بزيادة فولتية الانحياز الأمامي
وبالتالي فأن الجهد الحاجز سوف يقل أيضاً

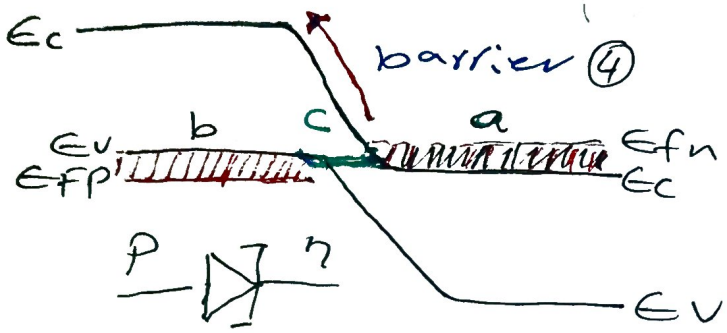
4



هنا نلاحظ في هذه الحالة (الثالثة) بأنه التقابل أو التناظر بين منطقة a ومنطقة b، (التناظر كامل وكبير)

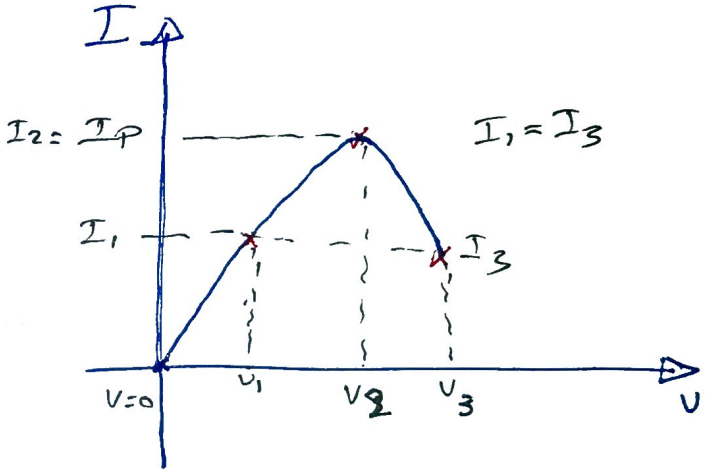
وعندها سوف يتم عملية تنشيط انتقال كامل للإلكترونات من المنطقة n إلى المنطقة p وبالتالي سوف تكون قيمة التيار أعلى ما يمكن I_{max} أو I_P

الحالة الرابعة:

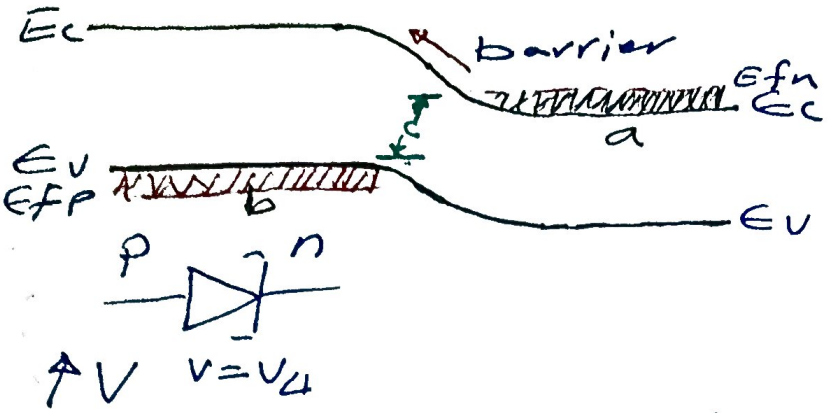


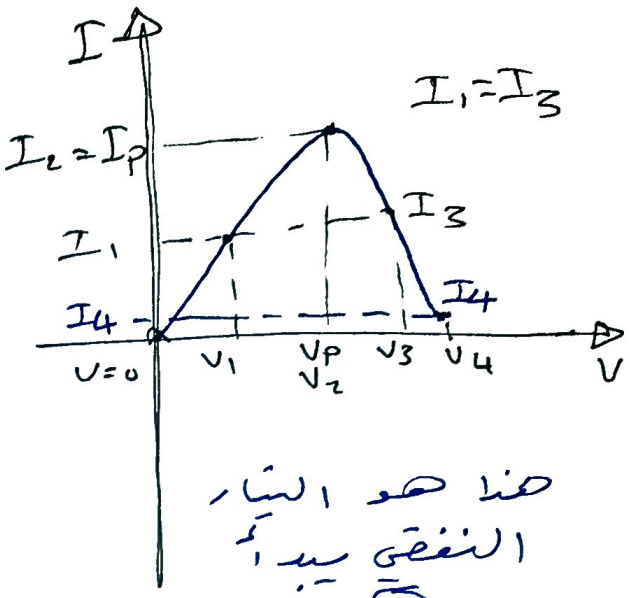
$U = V_3$

هنا في هذه الحالة (الرابعة) نتوقع زيادة الموصلية المطبقة بالاتجاه الأمامي بمقدار جهد $V > V_2$ أو حتى V_3 نلاحظ بأنه E_{fn} ارتفع أكثر من الحالة السابقة (الثالثة)، ارتفع الأعلى وكذلك نلاحظ بأن E_{fp} انخفض أكثر من الحالة السابقة (الثالثة) انخفض إلى الأسفل، وبالتالي فإن منطقة a ابتعدت عن منطقة b (ابتعدت بالتقابل) نتيجة زيادة الموصلية فإن الجهد الحاجز سوف يقل أيضاً وكذلك نلاحظ بأن التقابل بين a و b سوف يقل أو ينقص وبالتالي فإن التيار سوف يقل أيضاً لأن عملية التنشيط قلت عن السابق



المرحلة الخامسة





هذا هو التيار النفقي يبدأ من (V=0) إلى (V4)

هنا في هذه الحالة (الخامسة) تقوم بزيادة الفولتية المسلطة بالاتجاه الأمامي بمقدار معين $V > V_3$ أو حتى V_4، نلاحظ بأن E_{fn} ارتفعت أكثر من الحالة السابقة (1) الأعلى وكذلك فإن E_{FP} انخفضت أكثر من الحالة السابقة (انخفضت) الأسفل وبالتالي فإن منطقة a ابتعدت أكثر عن المنطقة b

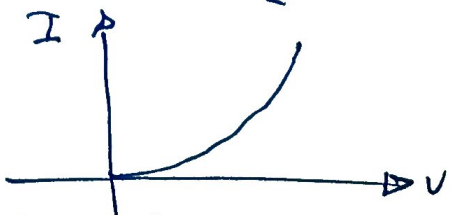
لا يوجد أي تقابل أو تناظر بينهما) وكذلك نتيجة زيادة الفولتية بالاتجاه الأمامي فإن الجهد الحاجز سوف يقل أكثر

وبالنتيجة فإن التيار سوف يقل أيضاً (أقل قيمة ممكنة

ولا يوجد أي وجود لعملية Tunneling

يحدث نتيجة تسليط فولتية على الثنائي النفقي بالاتجاه الأمامي وبنفس الوقت سوف تمر (تنفذ) الالكترونات من منطقة n (1) منطقة p بعد هذه المرحلة أو الحالة أو بعد هذه النقطة سيتصرف الثنائي النفقي مثل الثنائي الاعتيادي

أي يحدث خواص التيار الفولتية مثل الثنائي الاعتيادي



خواص الثنائي الاعتيادي

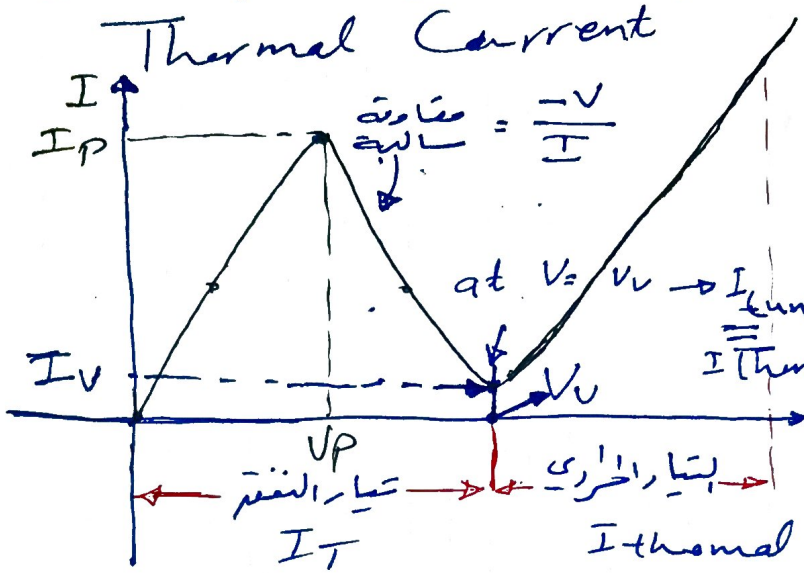
المرحلة الثانية

V $V = V_\gamma \cong 0.6$ أو 0.7 ← حتى في هذه الحالة

عندما: يبدأ التيار الحراري بالتناقص بالعكس

ممانعة الانهيار = ممانعة الحاجز للتيار

Thermal Current



$I_V = I_4$

I_V = Current Valley

تيار الوادي أو التعبير عن أقل قيمة تيار

$V_V = V_4$

V_V = Voltage Valley

الفولتية التي عندها يكون أقل قيمة للتيار (وأيضاً شكله شابه للوادي)

$\therefore I = I_{(tunnel} + I_{thermal)}$

لماذا المقاومة سالبة عند التيار النفقي ؟

لأنه التيار الاعتيادي أو التيار في حالة الثنائي العادي يكون شكله ↗ وهو أيضاً كما قلنا سابقاً

هذا التيار هو التيار الحراري (Thermal)

وهنا تكون المقاومة $\frac{V}{I}$ وهي موجبة

في حين في حالة التيار النفقي يكون معكوس ↘

في المنطقة التي يتناقص بها التيار بازدياد الفولتية (المقاومة سالبة) يستفاد من هذه المنطقة في عمل المذبذبات Oscillators, Amplifiers, switching device

at $V = V_V = I_{Tunnel} = I_{Thermal}$

Lectures of Electrical Engineering Department

Subject Title: Microelectronics

Class: 4th Electronic and Communications

Lecture Contents	**Lecture sequences:**	**First lecture**	**Instructor Name:**
	The major contents: **1- Basic Concepts** **2- Types of Solids (Conductivity)** **3- Types of Solids (Structures)** **4-**		
	The detailed contents: **1- Semiconductors Materials** **2- Atomic structure** **3- ENERGY BAND** **4- Diffusion Current Density**		

Basic Concepts

Types of Materials:

1- Solids.
2- Liquids.
3- Gases.

Types of Solids (Conductivity):

1- Insulators.
2- Semiconductors.
3- Conductors.

Types of Solids (Structures):

1- Amorphous.
2- Polycrystalline.
3- Single crystalline.

Semiconductors Materials:

The conductivity of a semiconductor is generally sensitive to temperature, illumination, magnetic field, and minute amounts of impurity atoms. This sensitivity in conductivity makes the semiconductor one of the most important materials for electronic applications.

Figure 1 shows the range of electrical conductivities $\sigma = S/cm$ and resistivities $\rho = 1/\sigma$

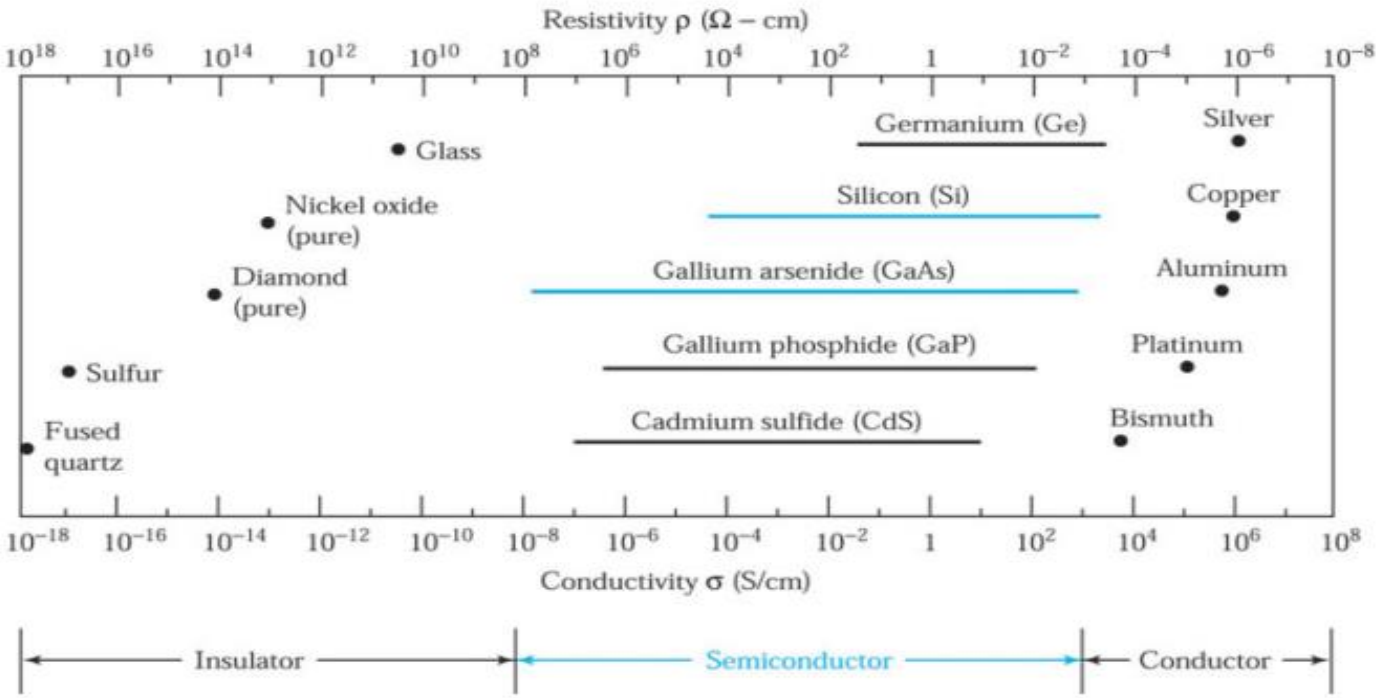


Fig. 1 Typical range of conductivities for insulators, semiconductors, and conductors.

$S = 1/\Omega$, $\rho = cm * \Omega$ $\rho =$ Rho , σ = Sigma , S = Siemens

Element Semiconductors

In the early 1950s, germanium was the major semiconductor material. Since the early 1960s silicon has become a practical substitute and has now virtually supplanted germanium as a semiconductor material. The main reasons we now use silicon are that silicon devices exhibit better properties at room temperature (teeny leakage current) and (high-quality silicon dioxide can be grown thermally).

Period	Column II	III	IV	V	VI
2		B Boron	C Carbon	N Nitrogen	O Oxygen
3	Mg Magnesium	Al Aluminum	Si Silicon	P Phosphorus	S Sulfur
4	Zn Zinc	Ga Gallium	Ge Germanium	As Arsenic	Se Selenium
5	Cd Cadmium	In Indium	Sn Tin	Sb Antimony	Te Tellurium
6	Hg Mercury		Pb Lead		

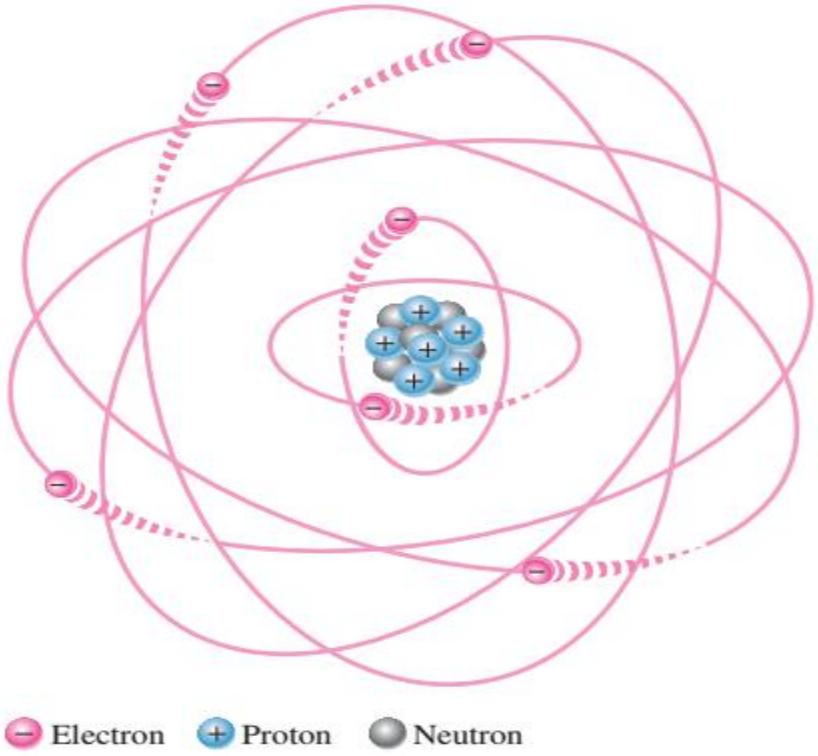
Compound Semiconductors

In recent years a number of compound semiconductors have found applications for various devices. A binary compound is a combination of two elements from the periodic table.

Many of the compound semiconductors have electrical and optical properties that are different from those of silicon. These semiconductors, especially GaAs, are used mainly for high-speed electronic , microwave and photonic applications.

Elemental	**IV compounds**	**Binary III–V compounds**	**Binary II–VI compounds**
Si	SiC	AlP	ZnS
Ge	SiGe	AlAs	ZnSe
		AlSb	ZnTe
		GaP	CdS
		GaAs	CdSe
		GaSb	CdTe

Atomic structure

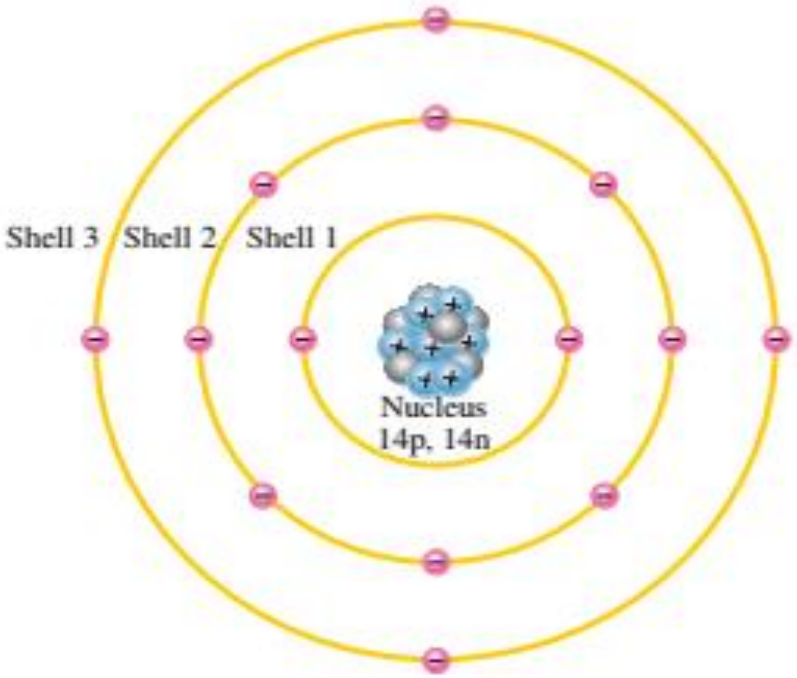


The Bohr model of an atom showing electrons in circular orbits around the nucleus. The "tails" on the electrons indicate they are moving.

Mass of (Neuton or Proton) = 1.66*$10^{-27} Kg$

Mass of Electron $<$ 1800 *time* of *proton mass*

$<$ 1800 *time* of *neutron mass*



Energy levels increase as the distance from the nucleus increases.

Electon Energy (E_H) = $\frac{-13.6}{n^2}\ ev$

An electron–volt is the energy of an electron that has been accelerated through a potential difference of 1 volt, and 1 eV = 1.6 × 10-19 joules.

Electron Shells and Orbits

Electrons orbit of an atom at certain distances from the nucleus. Electrons near the nucleus have less energy than those in more distant **orbits**.

Each orbit from the nucleus corresponds to a certain energy level . In an atom, the orbits are grouped into energy bands known as **shell**s.

Valence Electrons

Electrons that are in orbits farther from the nucleus have higher energy and are less tightly bound to the atom than those closer to the nucleus. Electrons with the highest energy levels exist in the outermost shell of an atom and are loosely bound to the atom. This outermost shell is known as the **valance** shell , and electrons in this shell are called **valence electrons**. The chemical activity of a material is determined primarily by the number of such electrons.

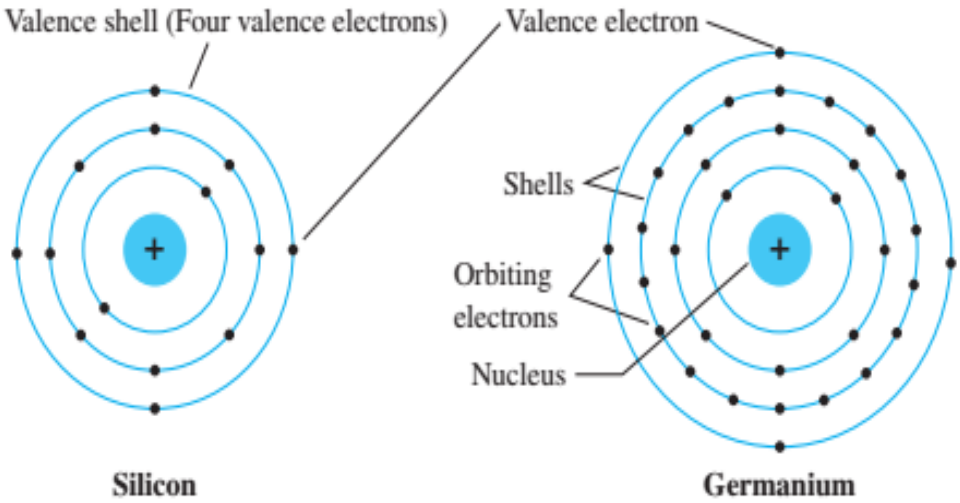
Free Electrons and Ions

If an electron absorbs a **photon** of sufficient energy, it escapes from the atom and becomes a **free electron** . Any time an atom or group of atoms acquires or loss the electron it is called an **ion**.

Conductors: are materials that allow current. They have a large number of free electrons and are characterized by one to three valence electrons in their structure. Most metals are good conductors. Silver is the best conductor, and copper is next.

Semiconductors: are classed below the conductors in their ability to carry current because they have fewer free electrons than do conductors. Semiconductors have four valence electrons in their atomic structures. Silicon (Si), germanium (Ge) and Gallium arsenide (GaAs) are common semiconductive materials.

Insulators: are nonmetallic materials that are poor conductors of electric current, they are used to prevent current where it is not wanted. Insulators have no free electrons in their structure. Insulators such as glass, and Teflon.



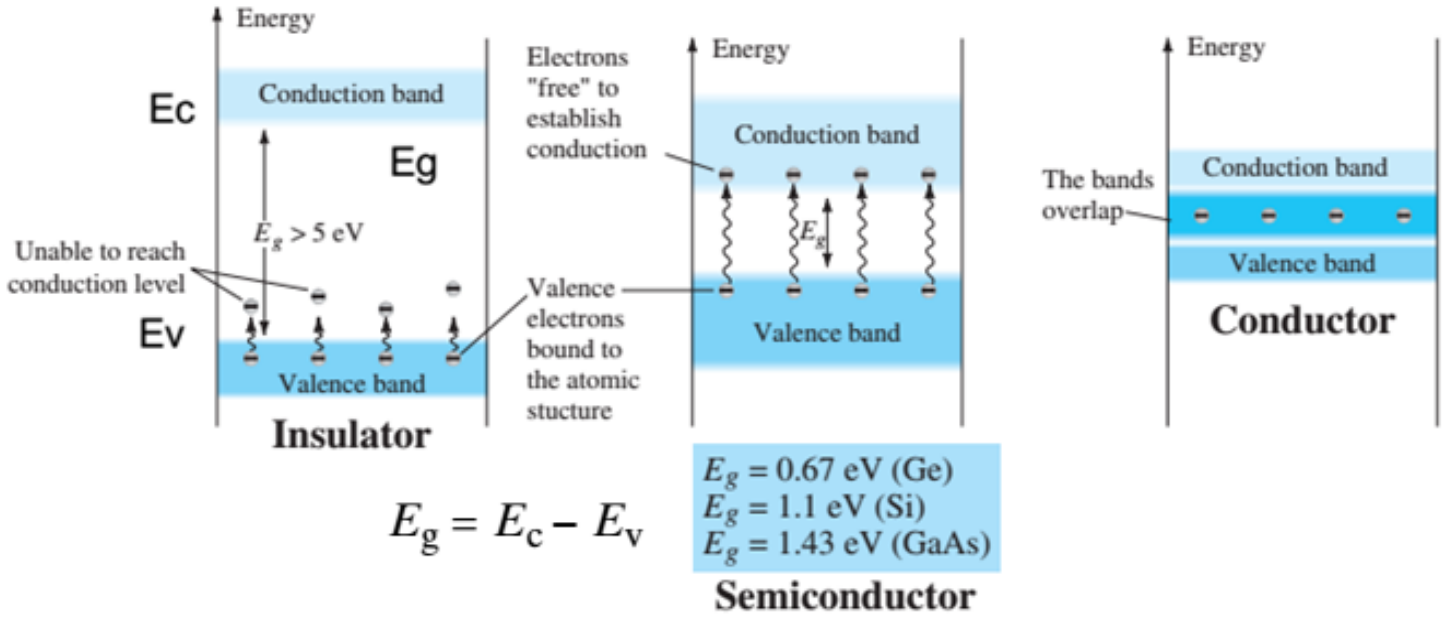
ENERGY BAND

Valance band (Ev): Is the band of electron orbitals that electrons can jump out of, moving into the conduction band when excited.The valance band is the outermost electron orbital of an atom.

Conduction band (Ec): Is the band of electron orbitals that electrons can jump up into from the valance band when excited. When the electrons are in these orbitals, they have enough energy to move freely in the material. This movement of electrons creates an electric current.

Band gap (Eg): The differnce in energy between the valance band and conduction band is called an energy gap or band gap,(Eg = Ec - Ev).

The region between these two energies is called the forbidden bandgap.



$$E_g = E_c - E_v$$

Materials that have large bandgap energies, in the range of 3 to 6 electron–volts (eV), are **insulators** because, at room temperature, essentially no free electrons exist in the conduction band.

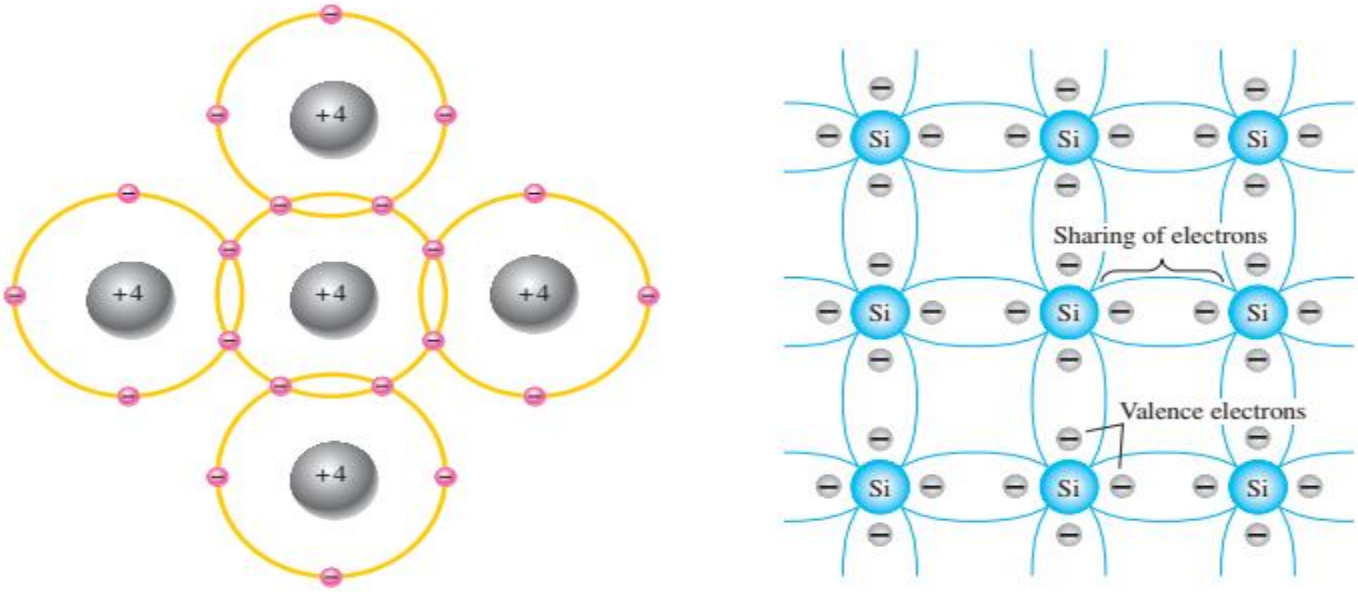
In contrast, materials that contain very large numbers of free electrons at room temperature are **conductors**.

In a **semiconductor,** the bandgap energy is on the order of 1 eV .

Covalent Bonds

In a pure silicon or germanium crystal the four valence electrons of one atom form a bonding arrangement with four adjoining atoms.

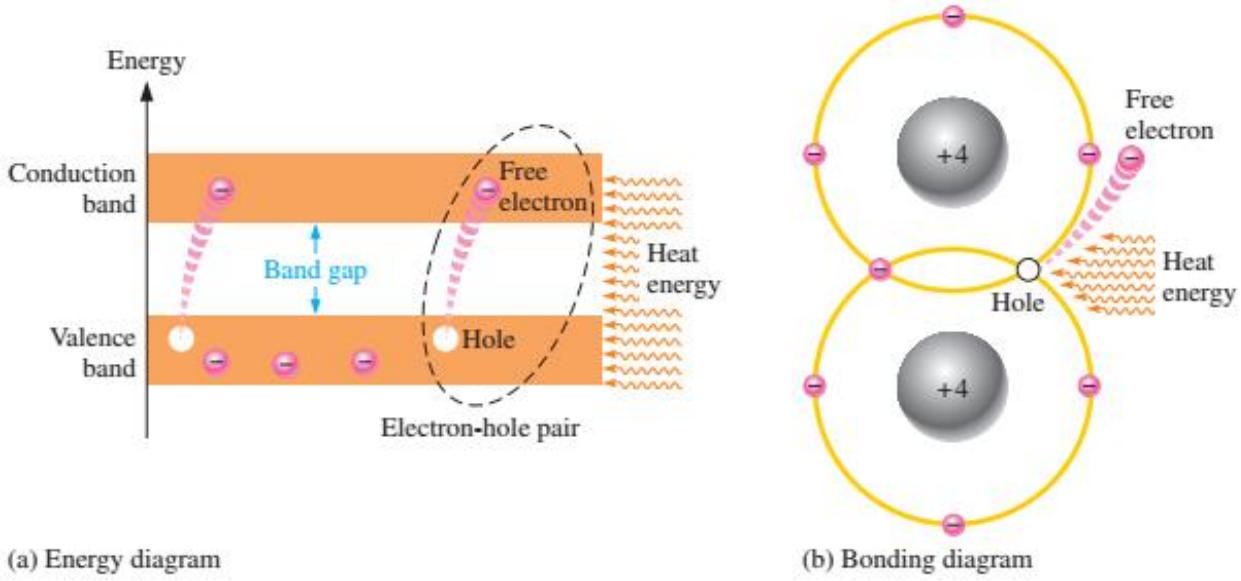
This bonding of atoms, strengthened by the sharing of electrons, is called covalent bonding.



Covalent bonds in silicon.

Conduction Electrons and Holes

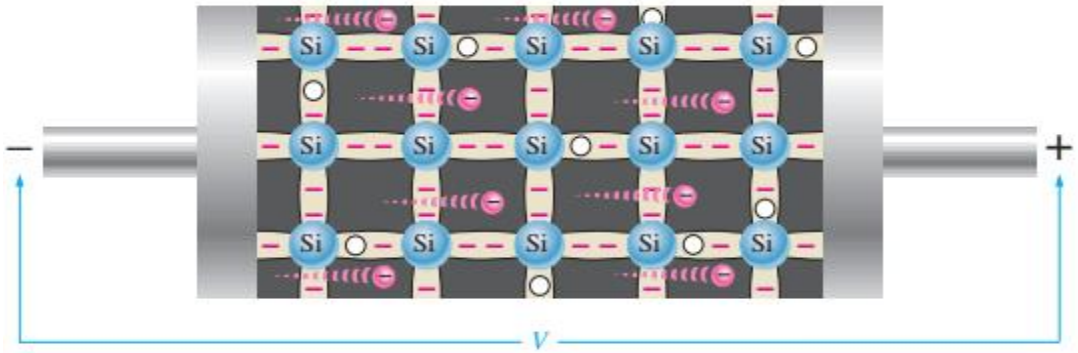
An intrinsic (pure) silicon crystal at room temperature has sufficient heat (thermal) energy for some valence electrons to jump the gap from the valence band into the conduction band, becoming free electrons. Free electrons are also called ***conduction electrons.***



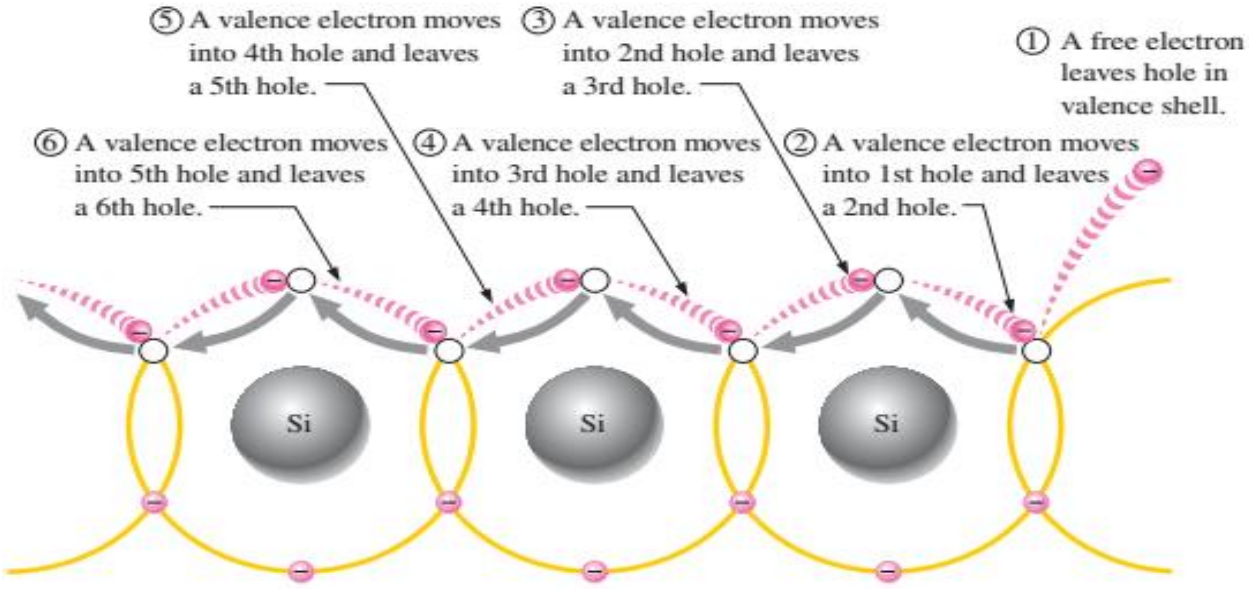
When an electron jumps to the conduction band, a vacancy is left in the valence band within the crystal. This vacancy is called a ***hole***. For every electron raised to the conduction band by external energy, there is one hole left in the valence band, creating what is called an **electron-hole pair.**

Electron and Hole Current

When a voltage is applied across a piece of intrinsic silicon, the thermally generated free electrons in the conduction band, which are free to move randomly in the crystal, are now easily attracted toward the positive end. This movement of free electrons is one type of current in a semiconductive material and is ***called electron current***.



Another type of current occurs in the valence band, where the holes created by the free electrons exist. Electrons remaining in the valence band are still attached to their atoms and are not free to move randomly in the crystal structure. The hole has moved from one place to another in the crystal structure. Although current in the valence band is produced by valence electrons, it is called ***hole current.***



When a valence electron moves left to right to fill a hole while leaving another hole behind, the hole has effectively moved from right to left. Gray arrows indicate effective movement of a hole.

Intrinsic Semiconductors

Is a single-crystal semiconductor material with no other types of atoms within the crystal. In an intrinsic semiconductor, the densities of electrons and holes are equal.

The notation n_i as the **intrinsic carrier concentration** for the concentration of the free electrons, as well as that of the holes. The equation for n_i is as follows:

$$n_i = BT^{3/2}\, e^{\left(\frac{-E_g}{2kT}\right)}$$

where *B* is a coefficient related to the specific semiconductor material, *Eg* is the bandgap energy (eV), T is the temperature (K), *k* is Boltzmann's constant = ($86 * 10^{-6}$ eV/K).

Material	*Eg* (eV)	*B* ($cm^{-3}\,K^{-3/2}$)
Silicon (Si)	1.1	5.23×10^{15}
Gallium arsenide (GaAs)	1.4	2.10×10^{14}
Germanium (Ge)	0.66	1.66×10^{15}

The values for B and Eg for several semiconductor materials are given

EXAMPLE: Calculate the intrinsic carrier concentration in silicon at T=300 K.

Solution:

$$n_i = BT^{3/2}\, e^{\left(\frac{-E_g}{2kT}\right)} \quad , \quad n_i = (5.23 * 10^{15})(300)^{3/2}\, e^{\left(\frac{-1.1}{2(86*10^{-6})(300)}\right)}$$

$$n_i = 1.5 * 10^{10}\ cm^{-3}$$

Comment: An intrinsic electron concentration of 1.5×10^{10} cm^{-3} may appear to be large, but it is relatively small compared to the concentration of silicon atoms, which is 5×10^{22} cm^{-3}.

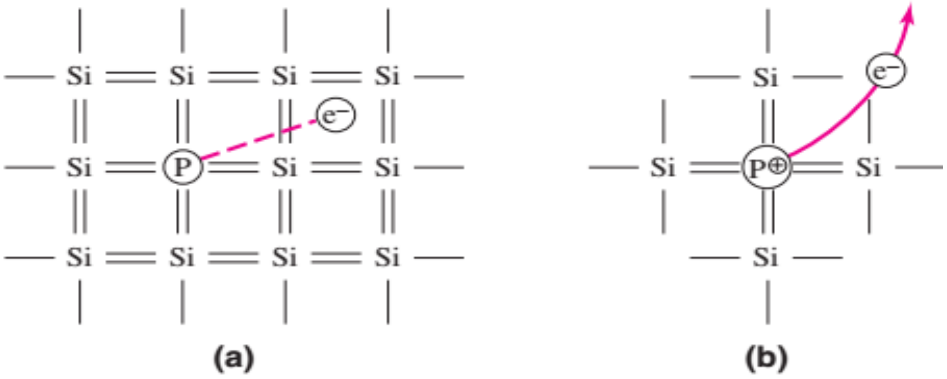
Intrinsic Carriers n_i

Semiconductor	Intrinsic Carriers (per cubic centimeter)
GaAs	1.7×10^{6}
Si	1.5×10^{10}
Ge	2.5×10^{13}

Extrinsic Semiconductors

Since the electron and hole concentrations in an intrinsic semiconductor are relatively small, only very small currents are possible. However, these concentrations can be greatly increased by adding controlled amounts of certain impurities.

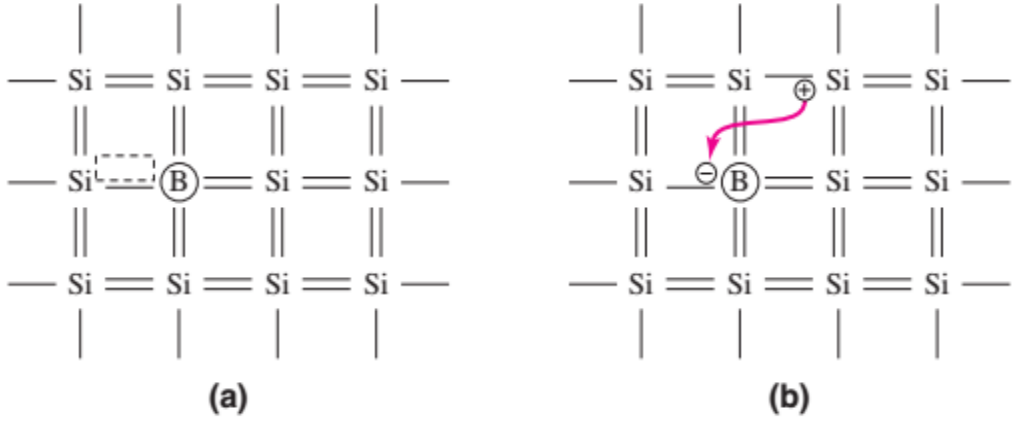
A desirable impurity is enters the crystal and replaces (i.e., substitutes for) one of the semiconductor atoms, even though the impurity atom does not have the same valence electron structure. For silicon, the desirable substitutional impurities are Boron (B) and Phosphorus (P) elements.



(a) silicon doped with a phosphorus atom showing the fifth phosphorus valence electron
(b) positively charged phosphorus ion after the fifth valence electron has moved into the conduction band

The phosphorus atom is called a **donor impurity,** since it donates an electron that is free to move. Although the remaining phosphorus atom has a net positive charge, the atom is immobile in the crystal and cannot contribute to the current.

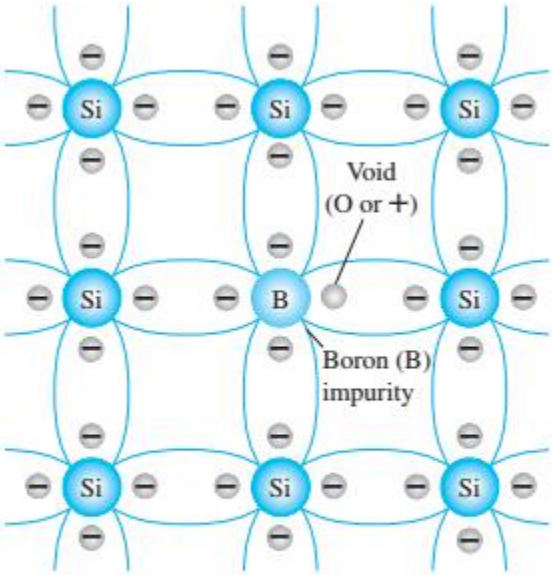
Therefore, when a donor impurity is added to a semiconductor, free electrons are created without generating holes. This process is called **doping,** and it allows us to control the concentration of free electrons in a semiconductor.



(a) silicon doped with a boron atom showing the vacant covalent bond position
(b) negatively charged boron ion after it has accepted an electron from the valence band.

When a boron atom replaces a silicon atom, its three valence electrons are used to satisfy the covalent bond requirements for three of the four nearest silicon atoms. This leaves one bond position open.

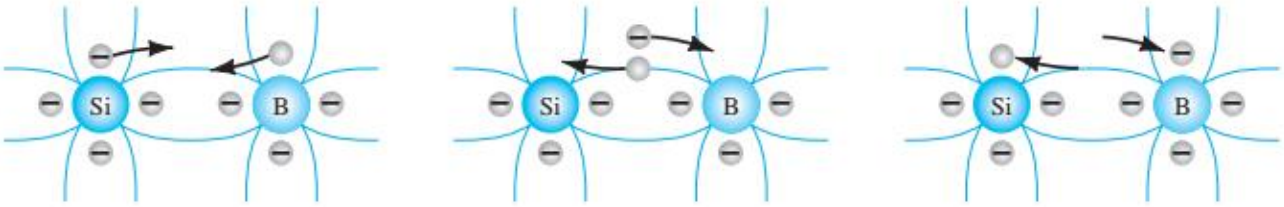
At room temperature, adjacent silicon valence electrons have sufficient thermal energy to move into this position, thereby creating a **hole**.



Boron impurity in p-type material.

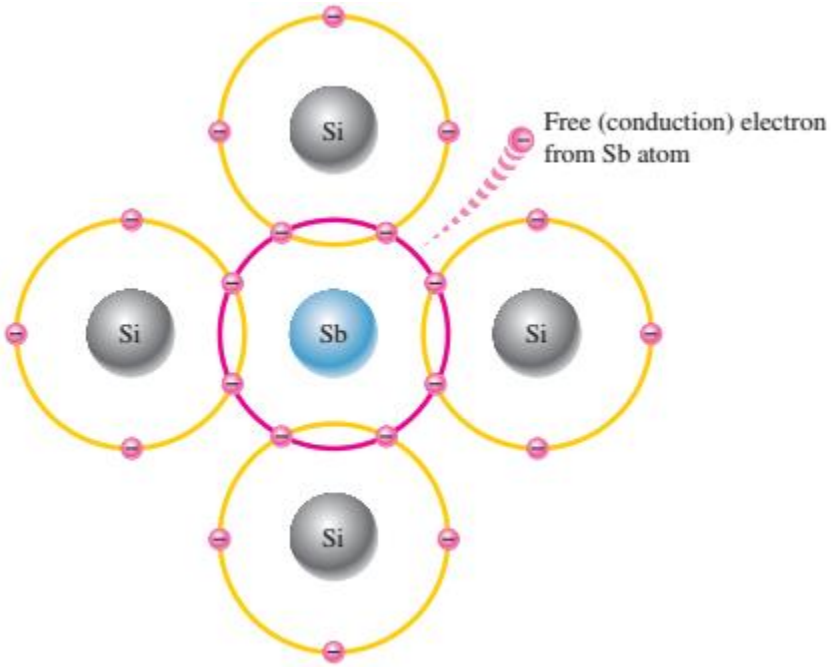
Because the boron atom has accepted a valence electron, the boron is therefore called an **acceptor impurity.**

Acceptor atoms lead to the creation of holes without electrons being generated. This process, also called **doping**, can be used to control the concentration of holes in a semiconductor.



n-type semiconductor

To increase the number of conduction-band electrons in intrinsic silicon, **pentavalent** impurity atoms are added. These are atoms with five valence electrons such as arsenic (As),phosphorus (P), and antimony (Sb).



A semiconductor that contains donor impurity atoms is called an **n-type semiconductor** (negatively charged electrons) and has a preponderance of electrons compared to holes.

The result is that at room temperature, there are a large number of carriers (electrons) in the conduction level, and the conductivity of the material increases significantly.

Majority and Minority Carriers **:**

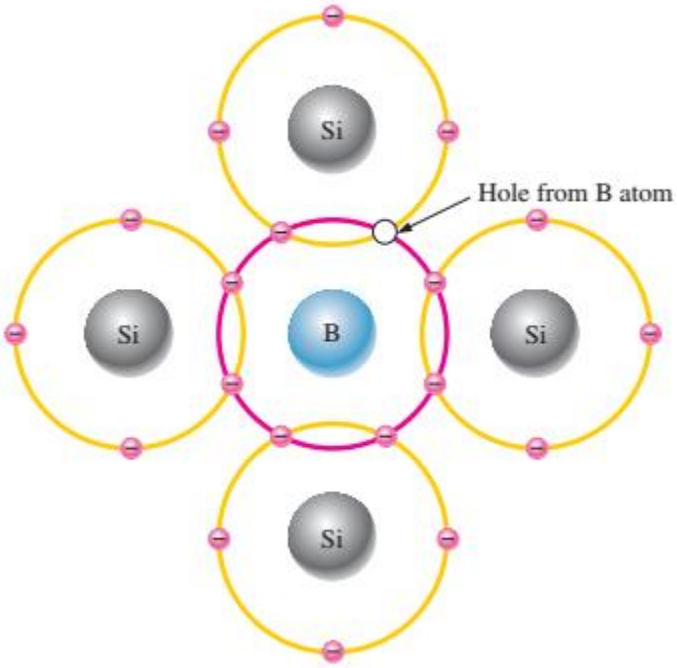
The electrons are called the **majority carriers** in *n*-type material. (the *n* stands for the negative charge on an electron).

Although the majority of current carriers in *n*-type material are electrons, there are also a few holes that are created when electron-hole pairs are thermally generated

These holes are **not** produced by the addition of the pentavalent impurity atoms. Holes in an n-type material are called **minority carriers**.

P-Type Semiconductor

To increase the number of holes in intrinsic silicon, **trivalent** impurity atoms are added. These are atoms with three valence electrons such as boron (B), indium (In), and gallium (Ga).



A semiconductor that contains acceptor impurity atoms is called a **p-type semiconductor** (positively charged holes created) and has a preponderance of holes compared to electrons.

Majority and Minority Carriers :

The holes are the **majority carriers** in ***p***-type material. Although the majority of current carriers in **p**-type material are holes, there are also a few conduction-band electrons that are created when electron-hole pairs are thermally generated. These conduction-band electrons are **not** produced by the addition of the trivalent impurity atoms. Conduction-band electrons in **p**-type material are the minority carriers.

Electron and hole concentrations

A fundamental relationship between the electron and hole concentrations in a semiconductor in **thermal equilibrium** is given by :

$$n_o\, p_o = n_i^2$$

- n_o is the thermal equilibrium concentration of free electrons.
- p_o is the thermal equilibrium concentration of holes.
- n_i is the intrinsic carrier concentration.

At room temperature (**T** = 300 K), each donor atom donates a free electron to the semiconductor. If the donor concentration **Nd** is much larger than the intrinsic concentration, we can approximate:

$n_o \cong N_d$, N_d is donor concentration

the hole concentration is:

$$p_o = \frac{n_i^2}{N_d}$$

If the acceptor concentration **Na** is much larger than the intrinsic concentration, we can approximate:

$p_o \cong N_a$, N_a is acceptor concentration

Then

$$n_o = \frac{n_i^2}{N_a}$$

Thermal equilibrium: the number of carriers in the conduction and valance band with no externally applied bias is called the equilibrium carrier concentration.

(Thermal equilibrium = zero bias voltage)

EXAMPLE: Calculate the thermal equilibrium electron and hole concentrations.

(a) Consider silicon at $T = 300$ K doped with phosphorus at a concentration of $N_d = 10^{16}\ \text{cm}^{-3}$. Recall from Example 1.1 that $n_i = 1.5 \times 10^{10}\ \text{cm}^{-3}$.

Solution: Since $N_d \gg n_i$, the electron concentration is

$$n_o \cong N_d = 10^{16}\,\text{cm}^{-3}$$

and the hole concentration is

$$p_o = \frac{n_i^2}{N_d} = \frac{(1.5 \times 10^{10})^2}{10^{16}} = 2.25 \times 10^4\,\text{cm}^{-3}$$

(b) Consider silicon at $T = 300$ K doped with boron at a concentration of $N_a = 5 \times 10^{16}\ \text{cm}^{-3}$.

Solution: Since $N_a \gg n_i$, the hole concentration is

$$p_o \cong N_a = 5 \times 10^{16}\,\text{cm}^{-3}$$

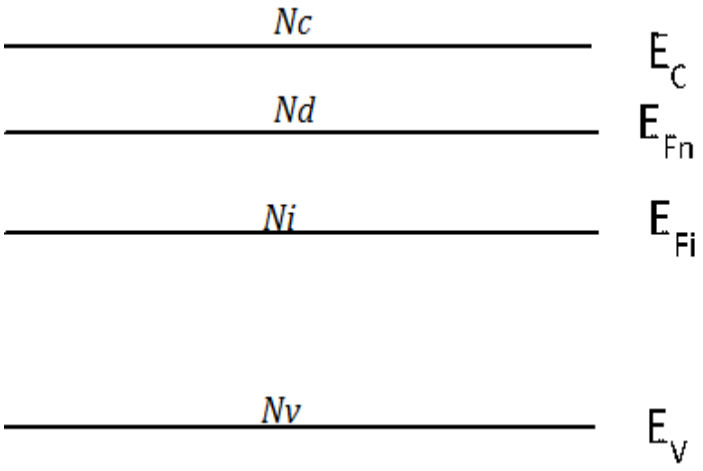
and the electron concentration is

$$n_o = \frac{n_i^2}{N_a} = \frac{(1.5 \times 10^{10})^2}{5 \times 10^{16}} = 4.5 \times 10^3\,\text{cm}^{-3}$$

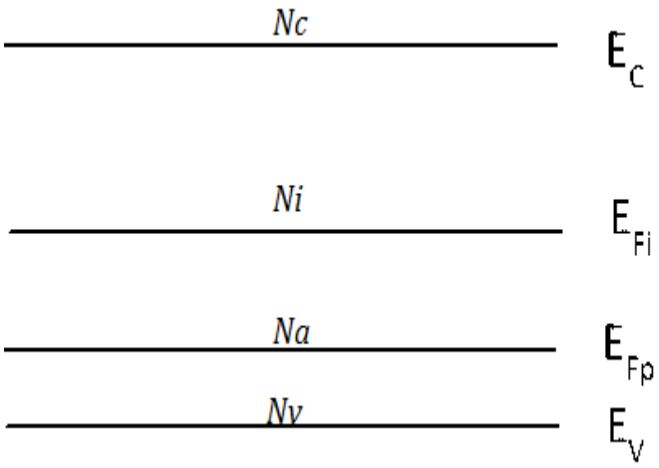
EXERCISE PROBLEM

(a) Calculate the majority and minority carrier concentrations in silicon at $T = 300$ K for (i) $N_d = 2 \times 10^{16}\ \text{cm}^{-3}$ and (ii) $N_a = 10^{15}\ \text{cm}^{-3}$. (b) Repeat part (a) for GaAs. (Ans. (a) (i) $n_o = 2 \times 10^{16}\ \text{cm}^{-3}$, $p_o = 1.125 \times 10^4\ \text{cm}^{-3}$; (ii) $p_o = 10^{15}\ \text{cm}^{-3}$, $n_o = 2.25 \times 10^5\ \text{cm}^{-3}$; (b) (i) $n_o = 2 \times 10^{16}\ \text{cm}^{-3}$, $p_o = 1.62 \times 10^{-4}\ \text{cm}^{-3}$; (ii) $p_o = 10^{15}\ \text{cm}^{-3}$, $n_o = 3.24 \times 10^{-3}\ \text{cm}^{-3}$).

N – type



p – type



$$Nc = ni \ exp \ \frac{+|Ec-Efi|}{KT}$$

$$Ni = Nc \ exp \ \frac{-|Ec-Efi|}{KT}$$

$$Nd = Ni \ exp \ \frac{+|Efn-Efi|}{KT}$$

$$Ni = Nd \ exp \ \frac{-|Efn-Efi|}{KT}$$

$$Nd = Nc \ exp \ \frac{-|Ec-Efn|}{KT}$$

$$Na = ni \ exp \ \frac{+|Efp-Efi|}{KT}$$

$$Nv = Na \ exp \ \frac{+|Ev-Efp|}{KT}$$

$$Na = Nv \ exp \ \frac{-|Ev-Efp|}{KT}$$

$$Nv = Ni \ exp \ \frac{+|Ev-Efi|}{KT}$$

$$Ni = Nv \ exp \ \frac{-|Ev-Efi|}{KT}$$

Nc = Conduction band concentration. *Ec = Energy of Conduction band.*

Ni = Intrinsic Fermi level concentration. *Efi = Energy of Internist Fermi level.*

Nd = Donor electron concentration. *Efn = Energy of Donor Fermi level.*

Na = Acceptor hole concentration. *Efp = Energy of Acceptor Fermi level.*

Nv = Valance band concentration. *Ev = Energy of Valance band.*

K = Boltzmann's constant *T = Temperature of semiconductor.*

The Fermi level is the energy at which the probability of occupation by an electron is exactly one-half {0.5} (lies midway between the two bands)

Drift and Diffusion Currents

❖ Two types of current exist in the semiconductors :

1. Drift Current Density
2. Diffusion Current Density

Drift Current Density:

To understand drift, assume an electric field is applied to a semiconductor. An electric field ***E*** applied in one direction produces a force on the electrons in the *opposite* direction, because of the electrons' negative charge. The electrons acquire a **drift velocity** v_{dn} (in cm/s) which can be written as:

$v_{dn} = -\mu_n E$ drift velocity

μ_n: **electron mobility** in $cm^2/V–s$ ⟶ (constant)

The negative sign in Equation indicates that the electron drift velocity is opposite to that of the applied electric field.

The electron drift produces a **drift current density** J_n (A/cm^2) given by:

$$J_n = -env_{dn} = -en(-\mu_n E) = +en\mu_n E$$

where **n** is the electron concentration (#/cm3) and **e**, is the magnitude of the electronic charge.

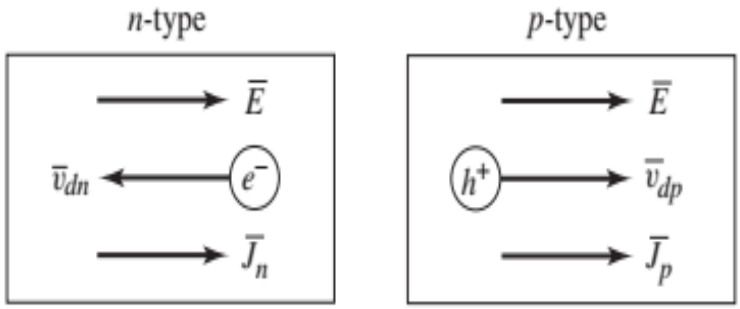
The conventional drift current (*Jn*) is in the opposite direction from the flow of negative charge (e^-), which means that the drift current in an n-type semiconductor is in the same direction as the applied electric field (*E*).

- Similarly (consider a p-type semiconductor)

An electric field ***E*** applied in one direction produces a force on the holes in the **same** direction, because of the positive charge on the holes.

$v_{dp} = +\mu_p E$ drift velocity

μ_p: **hole mobility** in $cm^2/V–s$ (constant)



The positive sign in Equation indicates that the hole drift velocity is in the same direction as the applied electric field.

The hole drift produces a **drift current density** J_p (A/cm^2) given by:

$$J_p = +epv_{dp} = +ep(+\mu_p E) = +ep\mu_p E$$

where **p** is the hole concentration (#/cm3) and **e** is again the magnitude of the electronic charge.

The conventional drift current (*Jp*) is in the same direction as the flow of positive charge (h^+), which means that the drift current in a p-type material is also in the same direction as the applied electric field (*E*)

Since a semiconductor contains both electrons and holes, the total drift current density is the sum of the electron and hole components. The total drift current density is then written as:

$$J = en\mu_n E + ep\mu_p E = \sigma E = \frac{1}{\rho} E$$

Where $\sigma = en\mu_n + ep\mu_p$

σ is the **conductivity** of the semiconductor in **(Ω–cm)**$^{-1}$

ρ is the **resistivity** of the semiconductor in **(Ω–cm)**

EXERCISE PROBLEM

Consider n-type GaAs at $T = 300$ K doped to a concentration of $N_d = 2 \times 10^{16}$ cm^{-3}. Assume mobility values of $\mu_n = 6800$ cm^2/V–s and $\mu_p = 300$ cm^2/V–s. (a) Determine the resistivity of the material. (b) Determine the applied electric field that will induce a drift current density of 175 A/cm^2. (Ans. (a) 0.0460 Ω–cm, (b) 8.04 V/cm).

EXAMPLE

Objective: Calculate the drift current density for a given semiconductor.

Consider silicon at $T = 300$ K doped with arsenic atoms at a concentration of $N_d = 8 \times 10^{15}$ cm^{-3}. Assume mobility values of $\mu_n = 1350$ cm^2/V–s and $\mu_p = 480$ cm^2/V–s. Assume the applied electric field is 100 V/cm.

Solution: The electron and hole concentrations are

$$n \cong N_d = 8 \times 10^{15}\,\text{cm}^{-3}$$

and

$$p = \frac{n_i^2}{N_d} = \frac{(1.5 \times 10^{10})^2}{8 \times 10^{15}} = 2.81 \times 10^4\,\text{cm}^{-3}$$

Because of the difference in magnitudes between the two concentrations, the conductivity is given by

$$\sigma = e\mu_n n + e\mu_p p \cong e\mu_n n$$

or

$$\sigma = (1.6 \times 10^{-19})(1350)(8 \times 10^{15}) = 1.73(\Omega\text{–cm})^{-1}$$

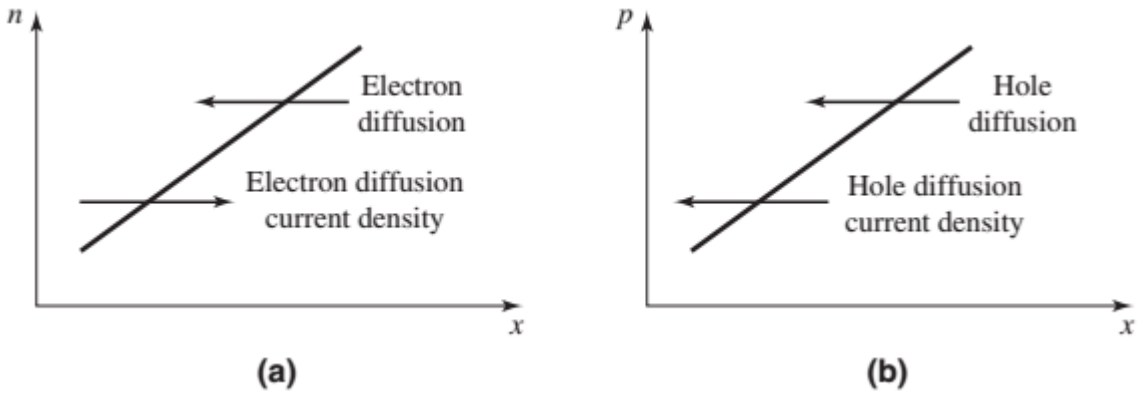
The drift current density is then

$$J = \sigma E = (1.73)(100) = 173\,\text{A/cm}^2$$

Comment: Since $n \gg p$, the conductivity is essentially a function of the electron concentration and mobility only. We may note that a current density of a few hundred amperes per square centimeter can be generated in a semiconductor.

Diffusion Current Density :

In the diffusion process, particles flow from a region of high concentration to a region of lower concentration.



For example, consider an electron concentration that varies as a function of distance **x**, as shown in Figure (a) .The diffusion of electrons from a high-concentration region to a low-concentration region produces a flow of electrons in the negative **x** direction. Since electrons are negatively charged, the conventional current direction is in the positive **x** direction.

- The diffusion current density due to the diffusion of electrons can be written as (for one dimension)

$$J_n = eD_n \frac{dn}{dx}$$

dn/dx is the gradient of the electron concentration

In Figure (b), the hole concentration is a function of distance. The diffusion of holes from a high-concentration region to a low-concentration region produces a flow of holes in the negative **x** direction. (Conventional current is in the direction of the flow of positive charge.)

- The diffusion current density due to the diffusion of holes can be written as (for one dimension)

$$J_p = -eD_p \frac{dp}{dx}$$

dp/dx is the gradient of the hole concentration

*Dn **is the** electron diffusion coefficient.*

*Dp **is the** hole diffusion coefficient.*

EXAMPLE

Objective: Calculate the diffusion current density for a given semiconductor.

Consider silicon at $T = 300$ K. Assume the electron concentration varies linearly from $n = 10^{12}$ cm^{-3} to $n = 10^{16}$ cm^{-3} over the distance from $x = 0$ to $x = 3$ μm. Assume $D_n = 35$ cm^2/s.

Solution: We have

$$J_n = eD_n\frac{dn}{dx} = eD_n\frac{\Delta n}{\Delta x} = (1.6 \times 10^{-19})(35)\left(\frac{10^{12} - 10^{16}}{0 - 3 \times 10^{-4}}\right)$$

Or

$$J_n = 187 \text{ A/cm}^2$$

Comment: Diffusion current densities on the order of a few hundred amperes per square centimeter can also be generated in a semiconductor.

EXERCISE PROBLEM

Consider silicon at $T = 300$ K. Assume the hole concentration is given by $p = 10^{16}e^{-x/L_p}$ (cm^{-3}), where $L_p = 10^{-3}$ cm. Calculate the hole diffusion current density at (a) $x = 0$ and (b) $x = 10^{-3}$cm. Assume $D_p = 10$ cm^2/s. (Ans. (a) 16 A/cm^2, (b) 5.89 A/cm^2)

The mobility values in the drift current equations and the diffusion coefficient values in the diffusion current equations are not independent quantities. They are related by the **Einstein relation,** which is:

$$\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = \frac{kT}{e} \cong 0.026 \text{ V}$$

At room temperature.

The **total** current density is the sum of the drift and diffusion components. Fortunately, in most cases only one component dominates the current at any one time in a given region of a semiconductor.

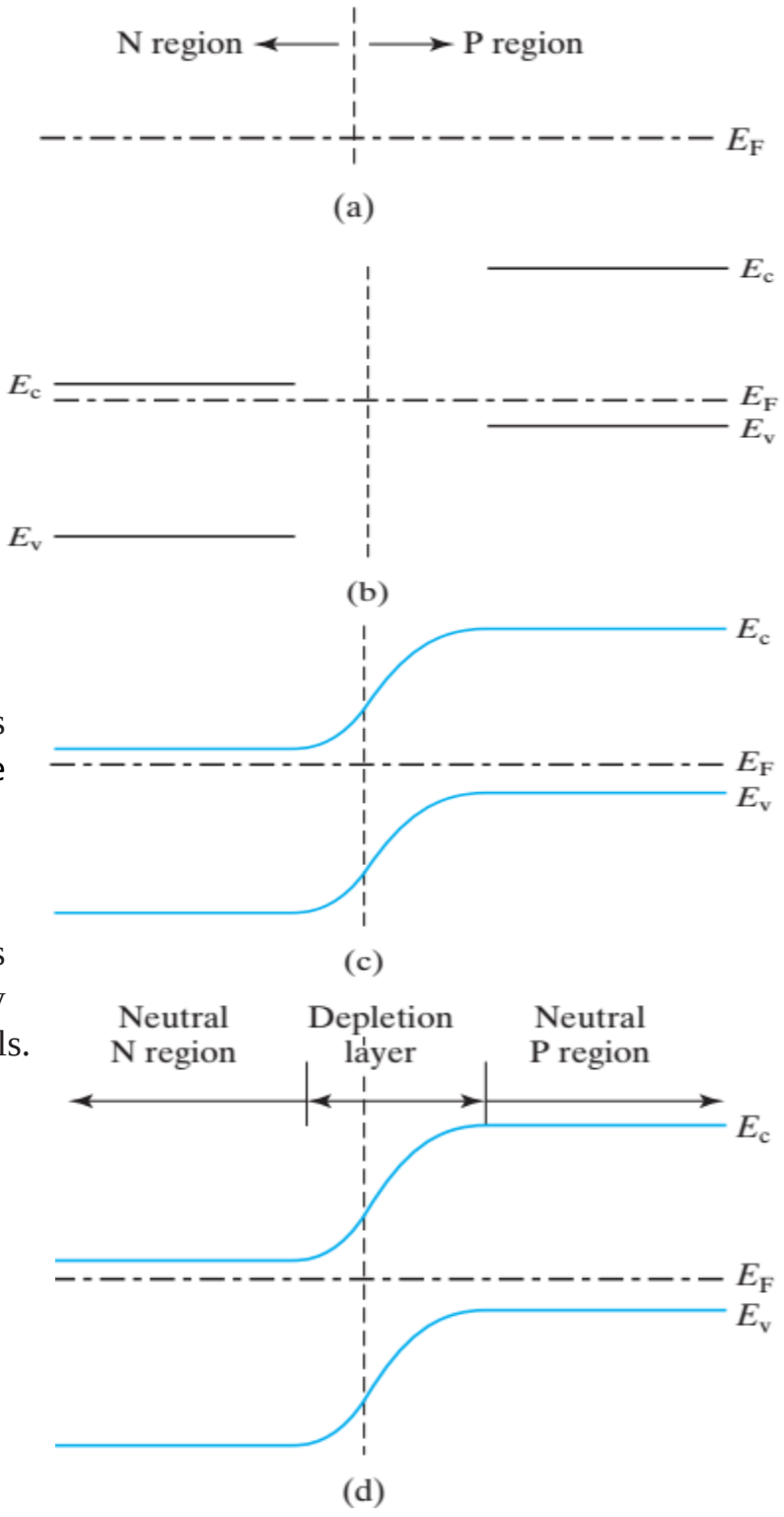
THE Equilibrium pn JUNCTION

P and N layers are uniformly doped at acceptor density **N**a, and donor density **N**d, respectively. This idealized PN junction is known as a *step junction*.

$n \approx 0$ and $p \approx 0$ in the depletion layer

The term **depletion layer** means that the layer is depleted of electrons and holes.

(No mobile electrons or holes).



Why the **n-type material** are lower than the **p-type material** ?

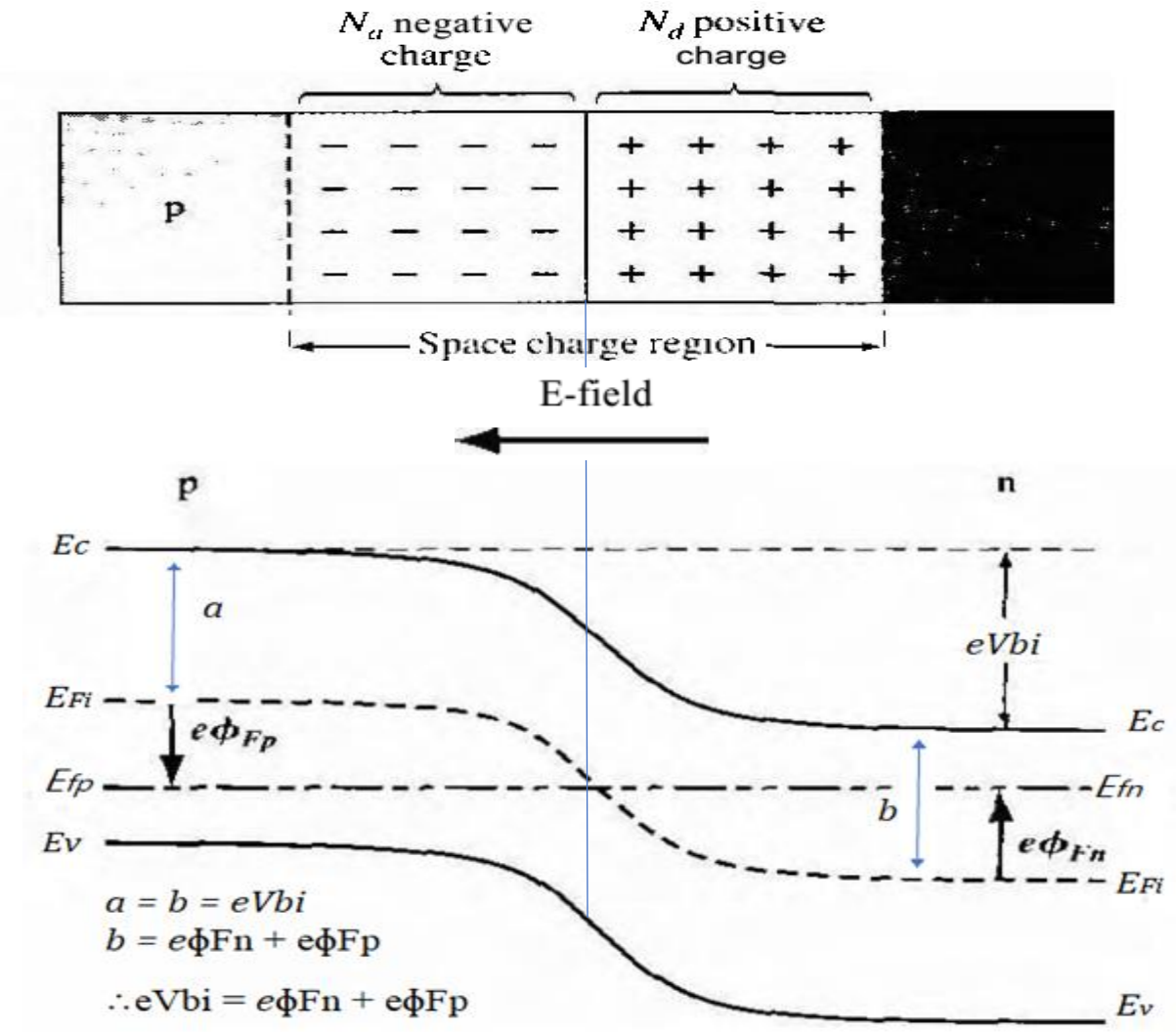
Because:

The trivalent impurities exert lower forces on the outer-shell electrons than the pentavalent impurities.

That is mean:

The lower forces in **p**-type materials means that the electron orbits have greater energy than the electron orbits in the **n**-type materials.

Depletion region = Space charge region

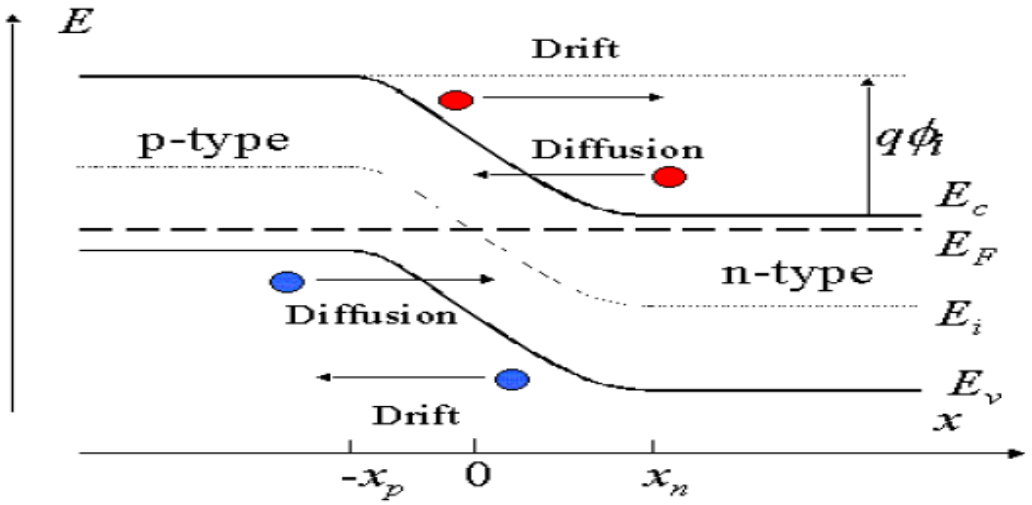


Energy - band diagram of a pn junction in thermal equilibrium

Vbi = built – in – potential barrier <u>*Or*</u> *built-in voltage (volts)*

ϕFn *= static potential for n type (volts).*

ϕFp *= static potential for p type (volts).*



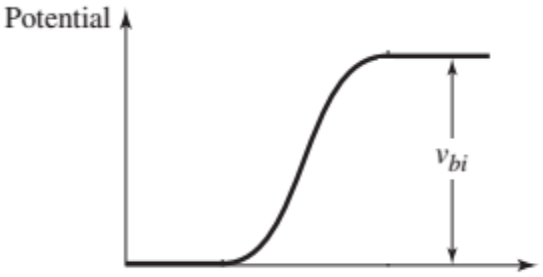
$$Nd = Ni \ exp \ \frac{+|Efn-Efi|}{KT} \quad , \quad e\phi Fn = Efi - Efn$$

$$Nd = Ni \ exp \ \frac{-(e\phi Fn)}{KT} \quad , \quad \phi Fn = \frac{Efi-Efn}{e}$$

$$\frac{Nd}{Ni} = exp \ \frac{-(e\phi Fn)}{KT} \longrightarrow \text{taking the lin of both sides}$$

$$\ln \frac{Nd}{Ni} = \frac{-(e\phi Fn)}{KT}$$

$$\therefore \phi Fn = -\frac{KT}{e} \ln \frac{Nd}{Ni}$$



Similarity , in the **P – region**

$$Na = ni \ exp \ \frac{+|Efi-Efp|}{KT} \quad , \quad e\phi Fp = Efi - Efp$$

$$\therefore \phi Fp = +\frac{KT}{e} \ln \frac{Na}{Ni} \quad , \quad \phi Fp = \frac{Efi-Efp}{e}$$

Finally , the built – in potential barrier for the pn junction is formed by :

$$\boxed{Vbi = \frac{KT}{e} \ln \frac{NaNd}{Ni^2}}$$

$where \ \frac{KT}{e}$ = vt (thermal voltage) vt = (25 – 26 mV)

EXAMPLE

Objective: Calculate the built-in potential barrier of a pn junction.

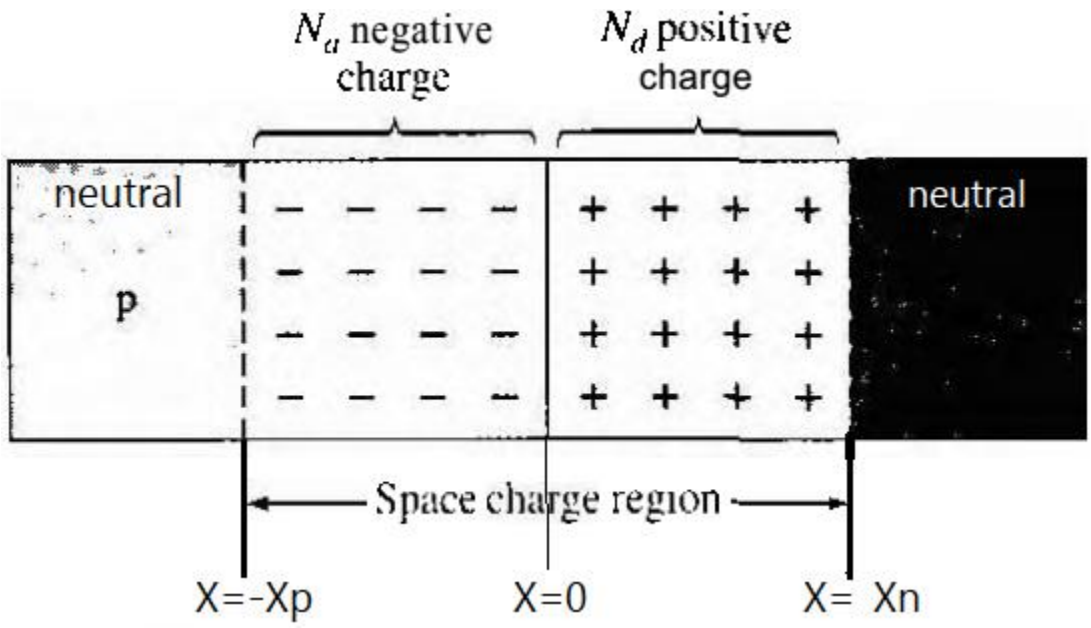
Consider a silicon pn junction at $T = 300$ K, doped at $N_a = 10^{16}$ cm^{-3} in the p-region and $N_d = 10^{17}$cm^{-3} in the n-region.

Solution: From the results of Example 1.1, we have $n_i = 1.5 \times 10^{10}$cm^{-3} for silicon at room temperature. We then find

$$V_{bi} = V_T \ln\left(\frac{N_a N_d}{n_i^2}\right) = (0.026) \ln\left[\frac{(10^{16})(10^{17})}{(1.5 \times 10^{10})^2}\right] = 0.757 \text{ V}$$

Electric Field of pn JUNCTION

An electric field is created in the depletion region by the separation of positive and negative space charge densities.



The electric field is determined from Poisson's equation which, for a one dimensional analysis, is

$$\frac{d^2\phi(x)}{dx^2} = \frac{-\rho(x)}{\varepsilon_s} = -\frac{dE(x)}{dx}$$

Where $\phi(x)$ is the electric potential{phi}, **E(x)** is the electric field , $\rho(x)$ is the volume charge density{Rho} and ε_s is the permittivity of the semiconductor{Epsilon}

$\varepsilon_s = \varepsilon_r * \varepsilon_o$ $\quad \varepsilon_r =$ Relative permittivity or dielectric constant = 11.7

$\varepsilon_o =$ Permittivity of free space = 8.85* 10^{-14} (farad/cm)

$\therefore\ \varepsilon_s = (11.7)\ (8.85* 10^{-14}) = 103.5$ (F/cm)

$\rho(x) = -eNa \quad , \quad -Xp \leq X \leq 0$

$\rho(x) = eNd \quad , \quad 0 \leq X \leq Xn$

The electric field in the p - region is found by integrating Equation:

$$-dE(x) = -\frac{\rho(x)}{\varepsilon_s}dx$$

$$\int dE(x) = \int \frac{\rho(x)}{\varepsilon_s}dx$$

$$E(x) = \int \frac{\rho(x)}{\varepsilon_s} dx = - \int \frac{eNa}{\varepsilon_s} dx$$

$$\therefore E(x) = \frac{-eNa}{\varepsilon_s} x + C_1$$ where $\mathbf{C_1}$ is a constant of integration

At $x = -xp$ ⟶ $E(x) = 0$

$$\therefore 0 = \frac{-eNa}{\varepsilon_s} - xp + C1 \longrightarrow \therefore C_1 = \frac{-eNa}{\varepsilon_s} xp$$

$$\therefore E = \frac{-eNa}{\varepsilon_s} x - \frac{eNa}{\varepsilon_s} xp$$

The electric field is assumed to be zero in the neutral p region for $X < -Xp$ since the currents are zero in thermal equilibrium.

$$\therefore E(x) = \frac{-eNa}{\varepsilon_s} (x + xp) \quad \text{at} \quad -Xp \leq X \leq 0$$

In the n region, the electric field is

$$E(x) = \int \frac{eNd}{\varepsilon_s} dx$$

$$E(x) = \frac{eNd}{\varepsilon_s} x + C_2$$ where $\mathbf{C_2}$ is a constant of integration

At $x = xn$ ⟶ $E(x) = 0$

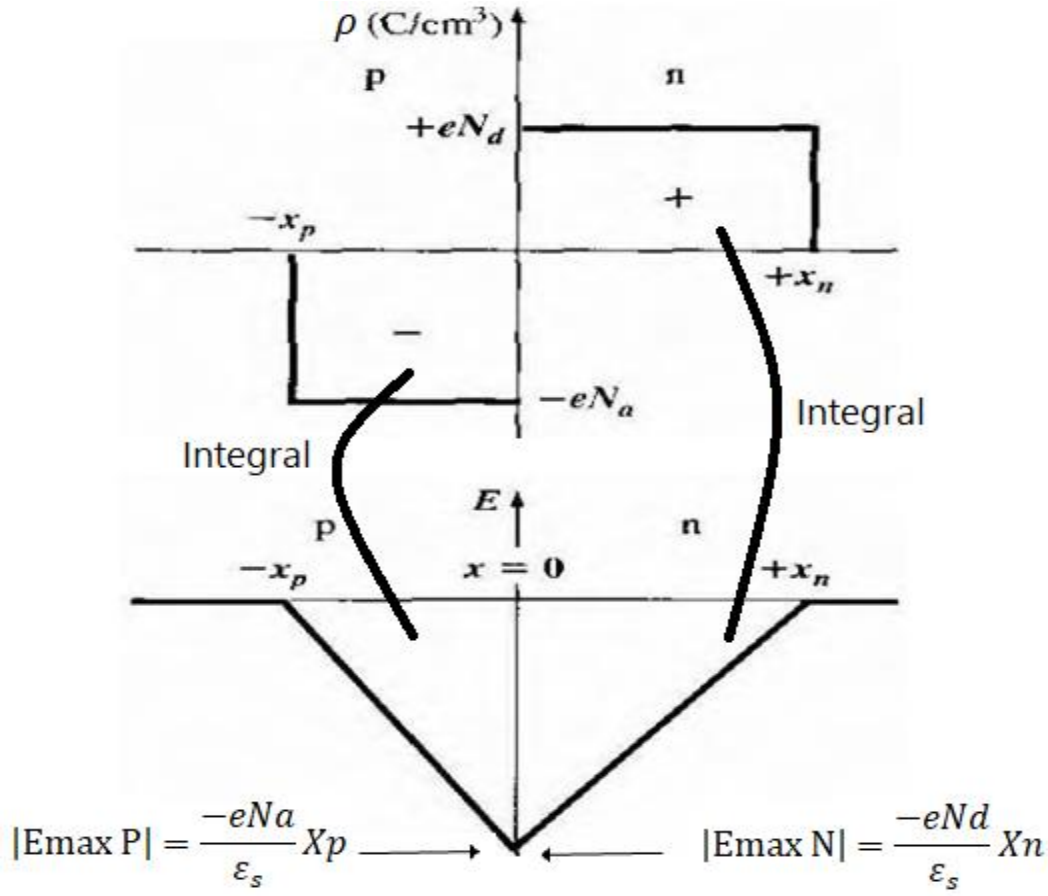
$$\therefore 0 = \frac{eNd}{\varepsilon_s} xn + C2 \longrightarrow \therefore C_2 = \frac{-eNd}{\varepsilon_s} xn$$

The electric field is assumed to be zero in the neutral n region for $X > Xn$ since the currents are zero in thermal equilibrium.

$$\therefore E(x) = \frac{-eNd}{\varepsilon_s} (xn - x) \quad \text{at} \quad 0 \leq X \leq Xn$$

or

$$\therefore E(x) = \frac{eNd}{\varepsilon_s} (x - xn) \quad \text{at} \quad 0 \leq X \leq Xn$$



∴ Max value of E(x) at x = 0

$$|Emax\ p| = |Emax\ n| \qquad \frac{-eNa}{\varepsilon_s} xp = \frac{-eNd}{\varepsilon_s} xn$$

$$NaXp = NdXn$$

- That is mean the number of negative charges per unit area in the p-region is equal to the number of positive charges per unit area in the n-region.
- An electric field exists in the depletion region even when no voltage is applied between the p-and n- regions.

Now another way to **determine *vbi***

The potential in the junction is found by integrating the electric field.

in the p-region.

$$\frac{d^2\phi}{dx^2} = -\frac{dE(x)}{dx} \quad , \quad E(x) = -\frac{d\phi(x)}{dx}$$

$$\int d\phi(x) = -\int E(x)dx$$

$$\phi(x) = -\int \frac{-eNa}{\varepsilon_s}(x + xp)\,dx$$

$$\phi(x) = \frac{eNa}{\varepsilon_s}\left(\frac{x^2}{2} + xp\,.x\right) + \bar{C}_1$$ where $\bar{C}_1$ is a constant of integration

The potential is assumed to be zero at $X = -Xp$. ⟶ $\phi(x) = 0$

$$\therefore 0 = \frac{-eNa}{\varepsilon_s}\left(\frac{xp^2}{2}\right) + \bar{C}_1 \longrightarrow \bar{C}_1 = \frac{eNa}{2\varepsilon_s}\,xp^2 \text{ or } \bar{C}_1 = \frac{eNa}{\varepsilon_s}\,\frac{xp^2}{2}$$

$$\therefore \phi(x) = \frac{eNa}{\varepsilon_s}\left(\frac{x^2}{2} + xp\,.x\right) + \frac{eNa}{\varepsilon_s}\,\frac{xp^2}{2}$$

$$\phi(x) = \frac{eNa}{\varepsilon_s}\left\{\left(\frac{x^2}{2} + xp\,.x\right) + \frac{xp^2}{2}\right\} \longrightarrow * 2$$

$$2\phi(x) = \frac{eNa}{\varepsilon_s}\left\{\left(x^2 + 2xp\,.x\right) + xp^2\right\}$$

$$2\phi(x) = \frac{eNa}{\varepsilon_s}(x + xp)^2 \longrightarrow /2$$

$$\boxed{\phi(x) = \frac{eNa}{2\varepsilon_s}(x + xp)^2 \qquad -Xp \le X \le 0}$$

In the n region, the potential is

$$\phi(x) = \int \frac{eNd}{\varepsilon_s}(xn - x)\,dx$$

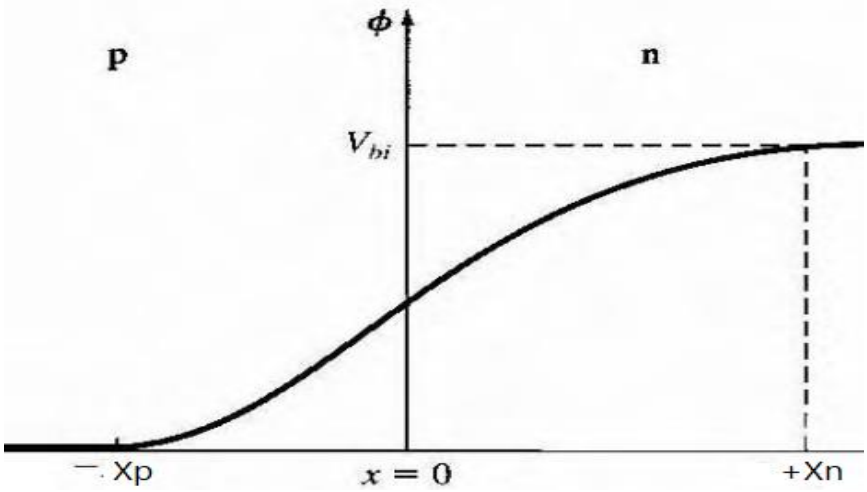
$$\phi(x) = \frac{eNd}{\varepsilon_s}\left(xn\,.x - \frac{x^2}{2}\right) + \bar{C}_2$$ where $\bar{C}_2$ is a constant of integration

$$\bar{C}_2 = \frac{eNa}{2\varepsilon_s}xp^2$$

In the n-region. The potential is not to be zero at $X = Xn$

$$\boxed{\phi(x) = \frac{eNd}{\varepsilon_s}\left(xn\,.x - \frac{x^2}{2}\right) + \frac{eNa}{2\varepsilon_s}xp^2 \qquad 0 \le X \le Xn}$$

Figure below is a plot of the potential through the junction. The magnitude of the potential at $X = Xn$ is equal to the built-in potential barrier.

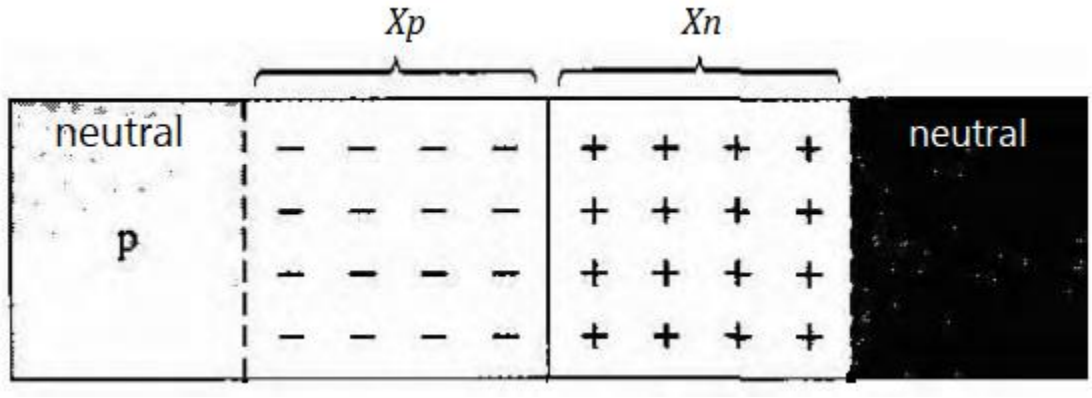


Electric potential through the space charge of a uniformly doped pn junction.

$$\therefore Vbi = |\phi(X = Xn)| = \frac{e}{2\varepsilon_s}(NdX^2n + NaX^2p) \quad \text{-------a}$$

Space charge width

We can determine the distance that the space charge region extends into the p and n regions from the junction. This distance is known as the space charge width



$$NaXp = NdXn$$

$$Xp = \frac{NdXn}{Na} \quad ----b$$ substituting equation ***b*** into equation ***a*** and solving for Xn

$$Vbi = \frac{e}{2\varepsilon_s}(NdX^2n + Na\frac{Nd^2Xn^2}{Na^2})$$

$$Vbi = \frac{e}{2\varepsilon_s}(NdX^2n + \frac{Nd^2Xn^2}{Na})$$

$$Vbi = \frac{e}{2\varepsilon_s}\{X^2n(Nd + \frac{Nd^2}{Na})\} \quad , \quad X^2n\left(Nd + \frac{Nd^2}{Na}\right) = \frac{2vbi\varepsilon_s}{e}$$

$$\therefore X^2n = \frac{2vbi\varepsilon_s}{e} * \frac{1}{Nd + \frac{Nd^2}{Na}} \quad , \quad \therefore X^2n = \frac{2vbi\varepsilon_s}{e} * \frac{Na}{NaNd + Nd^2}$$

$$\therefore \ Xn \ = \sqrt{\frac{2vbi\varepsilon_s}{e} * \frac{Na}{Nd}\left[\frac{1}{Na + Nd}\right]}$$

The width of the depletion region , *Xn* extending into the n-type region for the case of zero applied voltage.

Similarly, if we solve for Xp

$$\therefore \ Xp \ = \sqrt{\frac{2vbi\varepsilon_s}{e} * \frac{Nd}{Na}\left[\frac{1}{Na + Nd}\right]}$$

The width of the depletion region , *Xp* extending into the p-type region for the case of zero applied voltage.

The total depletion or space charge width *W* is the sum of the two components, or

W = Xn + Xp

$$\therefore \ W \ = \sqrt{\frac{2vbi\varepsilon_s}{e} * \left[\frac{Na + Nd}{NaNd}\right]}$$

∴ *Wmax* is achieved when Na = Nd

EXAMPLE

Calculate the space charge width (*W*) and electric field (*E*) in a pn junction. Consider a silicon at T = 300^0 K with doping of *Na* = 10^{16} cm^{-3} and *Nd* = 10^{15} cm^{-3} and *Xn = 0.864 μm.*

Solution:

$$Vbi = \frac{KT}{e} \ln \frac{NaNd}{Ni^2}$$

$$Vbi = (0.0259) \ln \frac{(10^{16})(10^{15})}{(1.5*10^{10})^2}$$

∴ *Vbi = 0.635 volt*

$$W = \left\{ \frac{2\epsilon_s V_{bi}}{e} \left[\frac{N_a + N_d}{N_a N_d} \right] \right\}^{1/2}$$

$$= \left\{ \frac{2(11.7)(8.85 \times 10^{-14})(0.635)}{1.6 \times 10^{-19}} \left[\frac{10^{16} + 10^{15}}{(10^{16})(10^{15})} \right] \right\}^{1/2}$$

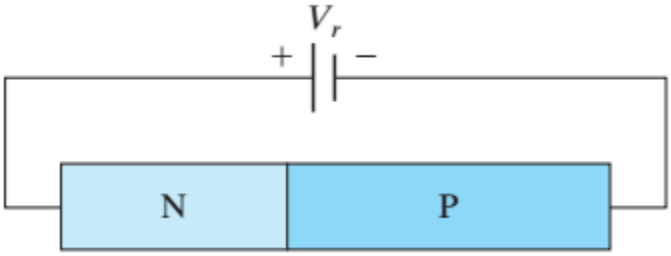
$$= 0.951 \times 10^{-4} \text{ cm} = 0.951\ \mu\text{m}$$

$$E_{max} = \frac{-eN_d x_n}{\epsilon_s} = \frac{-(1.6 \times 10^{-19})(10^{15})(0.864 \times 10^{-4})}{(11.7)(8.85 \times 10^{-14})}$$

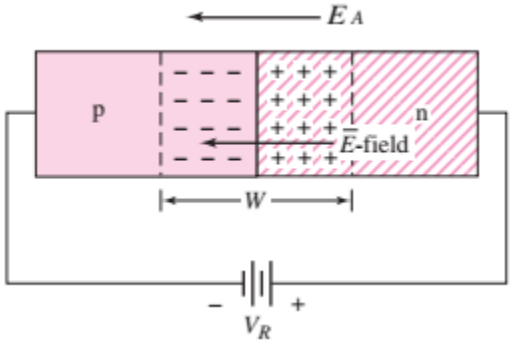
$$= 1.34 \times 10^{4} \text{ V/cm}$$

Reverse -Biased pn Junction

When a positive voltage is applied to the N region and negative voltage is applied to the P region, the PN junction is said to be **reverse-biased**.



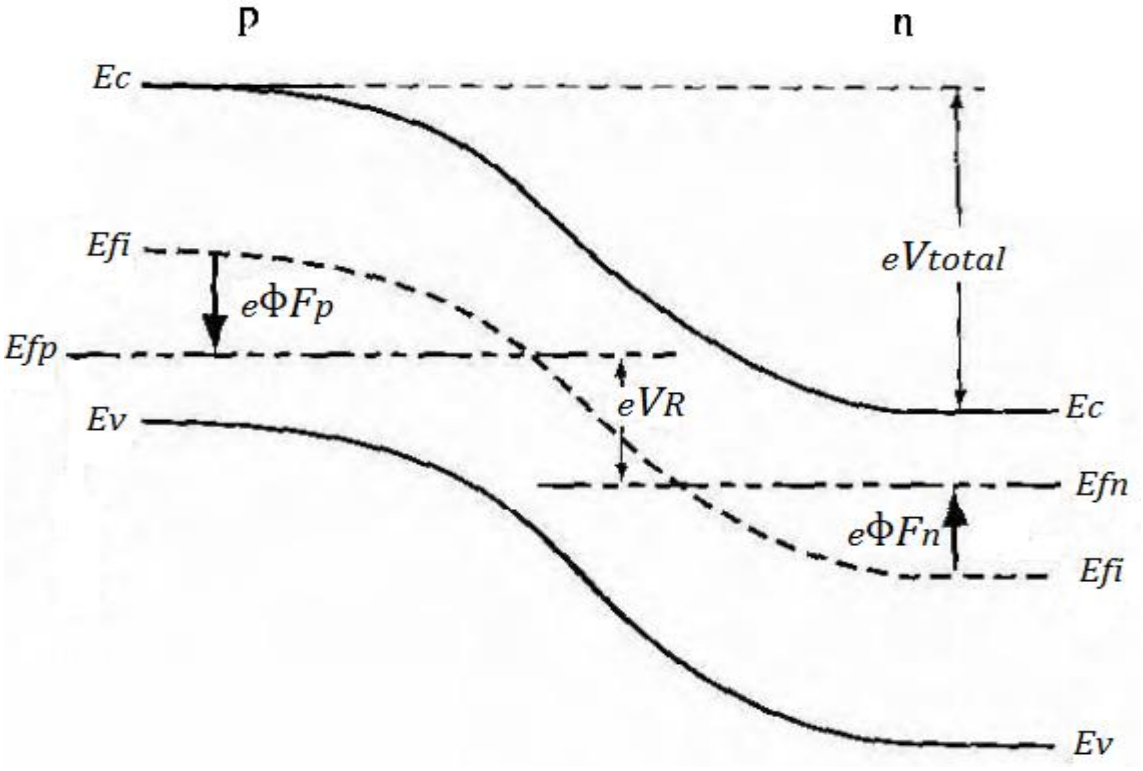
The applied voltage **VR** induces an applied electric field, $\mathbf{E_A}$, in the semiconductor. The direction of this applied field is the same as that of the **E**-field in the space-charge region. The magnitude of the electric field in the space charge region must increase above the thermal-equilibrium value due to the applied voltage.



There is no current across the pn junction.

The electric field ($\mathbf{E_A}$) originates positive and negative charges; this means that the number of positive and negative charges must increase if the electric field increases, Then the space charge width (**W**) increases.

In the reverse biased the Fermi energy level will not be constant through the system. Figure below shows the energy-band diagram of the pn junction



The total potential barrier, indicated by V_{total} has increased. This applied potential is the reverse – bias condition.

$V_{total} = |\phi Fn| + |\phi Fp| + V_R$

$$V_{total} = V_{bi} + V_R$$

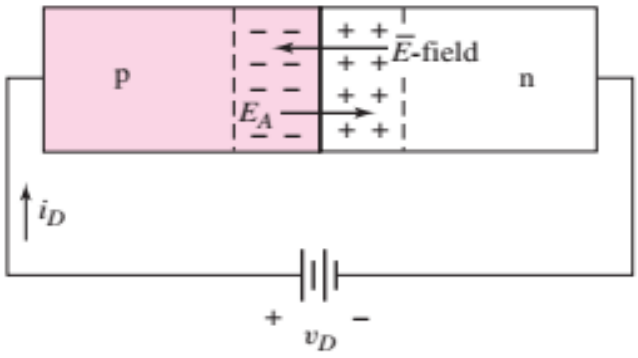
The total space charge width can he written as:

$$\therefore W = \sqrt{\frac{2\varepsilon_s(vbi + VR)}{e} * \left[\frac{Na + Nd}{NaNd}\right]}$$

$$Vbias = VR$$

Forward -Biased pn Junction

When a positive voltage is applied to the P region and negative voltage is applied to the N region, the PN junction is said to be **forward-biased**.



If a positive voltage $\mathbf{V}_D$ is applied to the p-region, the potential barrier decreases. The applied electric field, EA, induced by the applied voltage is in the opposite direction from that of the thermal equilibrium space-charge E-field.

There are current across the pn junction.

The total potential barrier, indicated by V_{total} has decreased. This applied potential is the forward – bias condition.

$$V_{total} = |\phi Fn| + |\phi Fp| - V_D$$

$$\boxed{V_{total} = V_{bi} - V_D}$$

The total space charge width can he written as:

$$\therefore W = \sqrt{\frac{2\varepsilon_s(vbi\_VD)}{e} * \left[\frac{Na + Nd}{NaNd}\right]}$$

$$Vbias = V_D$$

$$Vtotal = Vbi - V_D$$

EXAMPLE

Calculate the width of the space charge region in a pn junction when a reverse-biased voltage is applied.

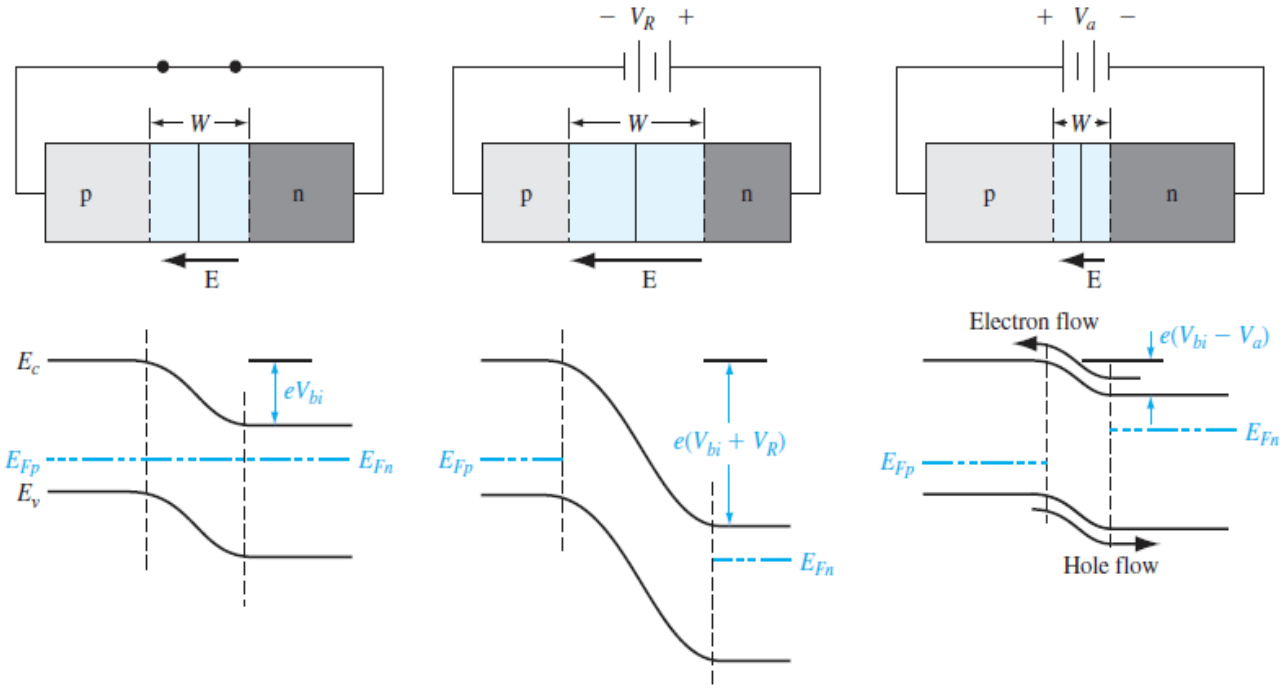
Again consider a silicon pn junction at $T = 300$ K with doping concentrations of $N_a = 10^{16}$ cm^{-3} and $N_d = 10^{15}$ cm^{-3}. Assume that $n_i = 1.5 \times 10^{10}$ cm^{-3} and $V_R = 5$ V.

Solution:

$$Vbi = (0.0259)\ln\frac{(10^{16})(10^{15})}{(1.5*10^{10})^2} \qquad \therefore Vbi = 0.635\ volt$$

$$W = \left\{\frac{2(11.7)(8.85\times10^{-14})(0.635+5)}{1.6\times10^{-19}}\left[\frac{10^{16}+10^{15}}{(10^{16})(10^{15})}\right]\right\}^{1/2}$$

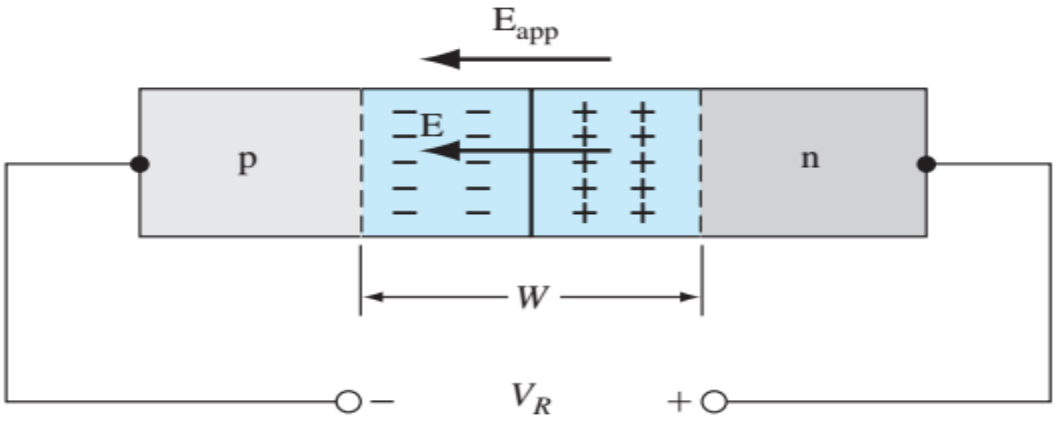
$$W = 2.83\times10^{-4}\ \text{cm} = 2.83\ \mu\text{m}$$



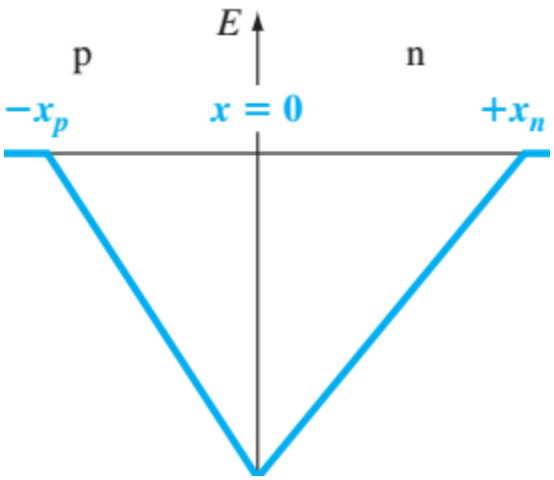
Zero bias | Reverse Bias | Forward bias

Electric Field For Reverse -Biased pn Junction

The magnitude of the electric field in the depletion region increases with an applied reverse-biased voltage.



Since ***Xn*** and ***Xp*** increase with reverse-biased voltage, the magnitude of the electric field also increases.



The maximum electric field still occurs at $X = 0$.

The electric field is given by Equations :

$$\mathrm{E_{max}} = \frac{-eN_d x_n}{\epsilon_s} = \frac{-eN_a x_p}{\epsilon_s}$$

Substitutive on *Xn*

$$Emax = \frac{-eNd}{\varepsilon_S} * \sqrt{\frac{2\varepsilon_S(vbi+VR)}{e} * \frac{Na}{Nd}\left[\frac{1}{Na+Nd}\right]}$$

Square both sides

$$Emax^2 = \frac{e^2Nd^2}{{\varepsilon_S}^2}\frac{2\varepsilon_S(vbi+VR)}{e} * \frac{Na}{Nd}\left[\frac{1}{Na+Nd}\right]$$

$$\mathrm{E_{max}} = -\left\{\frac{2e(V_{bi}+V_R)}{\epsilon_s}\left(\frac{N_a N_d}{N_a+N_d}\right)\right\}^{1/2}$$

We can show that the maximum electric field in the pn junction can also be written as

$$\mathrm{E_{max}} = \frac{-2(V_{bi}+V_R)}{W}$$

EXAMPLE

A silicon pn junction at $T = 300^0$ K with $Nd = 5*10^{15}cm^{-3}$ and $Na = 5*10^{16}cm^{-3}$. Assume $ni = 1.5*10^{10}cm^{-3}$. Calculate the reverse-voltage that will produce a maximum electric field of $|Emax| = 1.25*10^5$ V/ cm.

Solution:

$$E_{max} = -\left\{\frac{2e(V_{bi}+V_R)}{\epsilon_s}\left(\frac{N_aN_d}{N_a+N_d}\right)\right\}^{1/2}$$

$$Vbi + V_R = \frac{\varepsilon_S\, Emax^2}{2e}\left(\frac{Na+Nd}{NaNd}\right)$$

$$= \frac{(11.7)(8.85*10^{-14})(1.25*10^5)^2}{2(1.6*10^{-19})}\left[\frac{5*10^{16}+5*10^{15}}{(5*10^{16})(5*10^{15})}\right] = 11.1 \text{ V}$$

The built – in potential barrier , $\boxed{Vbi} = \frac{KT}{e}\ln\frac{NaNd}{Ni^2}$

$$Vbi = (0.0259)\ln\frac{(5*10^{16})(5*10^{15})}{(1.5*10^{10})^2}$$

$$Vbi = 0.718 \text{ V}$$

$$V_R = 11.1 - 0.718 = 10.4 \text{ V}$$

Junction Capacitance For Reverse -Biased pn Junction

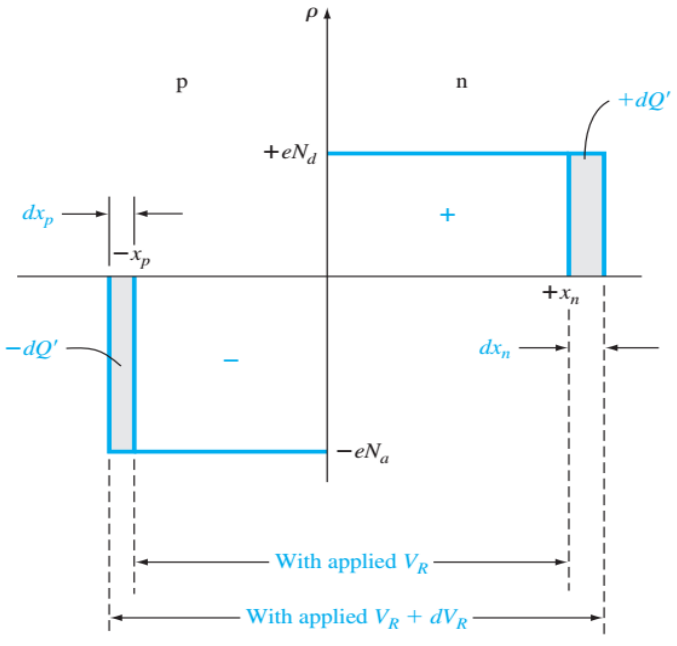
Since we have a separation of positive and negative charges in the depletion region, a capacitance is associated with the pn junction.

An increase in the reverse-biased voltage **dVR** will uncover additional positive charges in the n region and additional negative charges in the p region. The junction capacitance is defined as:

$$C' = \frac{dQ'}{dV_R}$$

$$dQ' = eN_d\,dx_n = eN_a\,dx_p$$

The differential charge **dQ** is in units of Coul/cm^2 so that the capacitance **C** is in the units (F/cm^2)



$$C' = \frac{dQ'}{dV_R} = eN_d \frac{dx_n}{dV_R}$$

$$x_n = \left\{ \frac{2\epsilon_s(V_{bi} + V_R)}{e} \left[\frac{N_a}{N_d} \right] \left[\frac{1}{N_a + N_d} \right] \right\}^{1/2}$$

$$C' = \left\{ \frac{e\epsilon_s N_a N_d}{2(V_{bi} + V_R)(N_a + N_d)} \right\}^{1/2}$$

EXAMPLE

To calculate the junction capacitance of a pn junction. Consider

Again consider a silicon pn junction at $T = 300$ K with doping concentrations of $N_a = 10^{16}$ cm^{-3} and $N_d = 10^{15}$ cm^{-3}. Assume that $n_i = 1.5 \times 10^{10}$ cm^{-3} and $V_R = 5$ V.

Solution

$$C' = \left\{ \frac{(1.6 \times 10^{-19})(11.7)(8.85 \times 10^{-14})(10^{16})(10^{15})}{2(0.635 + 5)(10^{16} + 10^{15})} \right\}^{1/2}$$

$$C' = 3.66 \times 10^{-9} \text{ F/cm}^2$$

If the cross-sectional area of the pn junction is, for example, $A = 10^{-4}$ cm^2, then the total junction capacitance is

$$C = C' \cdot A = 0.366 \times 10^{-12} \text{ F} = 0.366 \text{ pF}$$

Another expression for the junction capacitance that is:

$$C' = \frac{\epsilon_s}{W}$$

EXERCISE PROBLEM

Consider a GaAs pn junction at $T = 300$ K doped to $N_a = 5 \times 10^{15}$ cm^{-3} and $N_d = 2 \times 10^{16}$ cm^{-3}. (a) Calculate V_{bi}. (b) Determine the junction capacitance C' for $V_R =$ 4V

One-Sided Junctions (Na >> Nd)

Consider a special pn junction called the one-sided junction. for example, Na >> Nd this junction is referred to as a p^+ n junction. ($Xn >> Xp$)

$$x_n = \left\{\frac{2\epsilon_s(V_{bi} + V_R)}{e}\left[\frac{N_a}{N_d}\right]\left[\frac{1}{N_a + N_d}\right]\right\}^{1/2}$$

يهمل لان قيمته صغيرة جدا

$$\therefore Xn = \left\{\frac{2\varepsilon s(Vbi+VR)}{eNd}\right\}^{1/2}$$

$$\therefore Xp = \left\{\frac{2\varepsilon s(Vbi+VR)Nd}{eNa^2}\right\}^{1/2} \cong 0$$

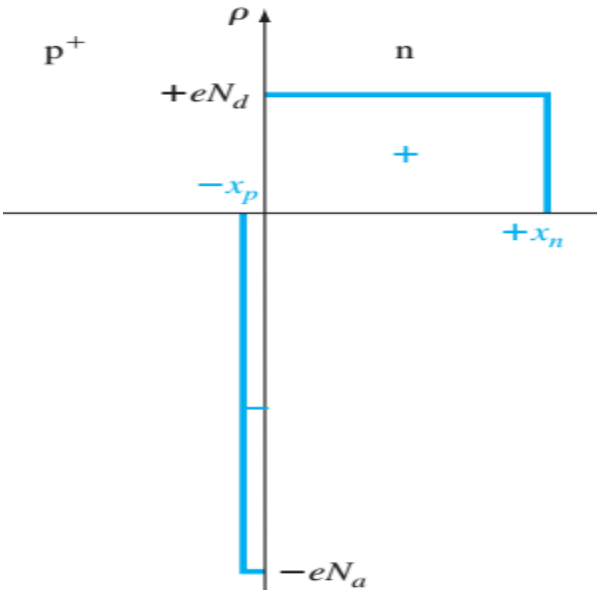
لان Na كمية كبيرة وهي في المقام وتربيع ايضا

∴The total space charge width is :

$$W \approx \left\{\frac{2\epsilon_s(V_{bi} + V_R)}{eN_d}\right\}^{1/2} \quad \text{(One-Sided)} \quad Xn >> Xp \quad W \approx Xn$$

The junction capacitance of the p^+ n junction reduces to

$$C' \approx \left\{\frac{e\epsilon_s N_d}{2(V_{bi} + V_R)}\right\}^{1/2} \qquad C' = \frac{\epsilon_s}{W}$$

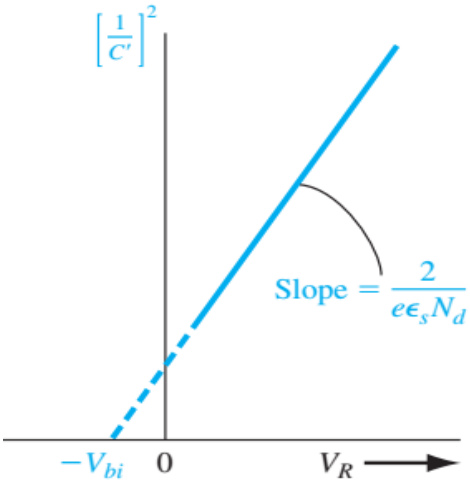


The depletion layer capacitance of a one-sided junction is a function of the doping concentration in the low-doped region (*Nd*).

The equation of capacitance can be weitten as:

$$\left(\frac{1}{C'}\right)^2 = \frac{2(V_{bi} + V_R)}{e\epsilon_s N_d}$$

which shows that the inverse capacitance squared is a linear function of applied reverse-biased voltage.



EXAMPLE

Determine the impurity doping (*Na* and *Nd*) in a p^+ n Si-junction for parameters $T = 300\ ^0$K , $ni = 1.5 * 10^{10}\ cm^{-3}$, $Vbi = 0.72$V and slope = $6.15*10^{15}(F/cm^2)^{-2}.V^{-1}$

Solution:

$$N_d = \frac{2}{e\,\epsilon_s} \cdot \frac{1}{slope} = \frac{2}{(1.6 \times 10^{-19})(11.7)(8.85 \times 10^{-14})(6.15 \times 10^{15})}$$

$$N_d = 1.96 \times 10^{15}\ \text{cm}^{-3}$$

$$V_{bi} = V_t \ln\left(\frac{N_a N_d}{n_i^2}\right)$$

$$N_a = \frac{n_i^2}{N_d} \exp\left(\frac{V_{bi}}{V_t}\right) = \frac{(1.5 \times 10^{10})^2}{1.963 \times 10^{15}} \exp\left(\frac{0.725}{0.0259}\right)$$

$$N_a = 1.64 \times 10^{17}\ \text{cm}^{-3}$$

Comment

The results of this example show that $N_a \gg N_d$; therefore the assumption of a one-sided junction was valid.

EXERCISE PROBLEM

The experimentally measured junction capacitance of a one-sided silicon n^+p junction biased at $V_R = 3$ V and at $T = 300$ K is $C = 0.105$ pF. The built-in potential barrier is found to be $V_{bi} = 0.765$ V. The cross-sectional area is $A = 10^{-5}$ cm^2. Find the doping concentrations.

Ideal Current–Voltage Relationship

$$I = I_s\left[\exp\left(\frac{eV_a}{nkT}\right) - 1\right] \qquad I = I_s\left[\exp\left(\frac{V_a}{nVt}\right) - 1\right]$$

The parameter ***IS*** is the ***reverse-bias saturation current*** . For silicon pn junctions, typical values of ***IS*** are in the range of 10^{-18} to 10^{-20} A.

The actual value depends on the doping concentrations and is also proportional to the cross-sectional area of the junction.

VT = *0.026 V at room temperature.*

The parameter **n** is usually called the emission coefficient or ideality factor, and its value is in the range $1 \leq \mathbf{n} \leq 2$.

The emission coefficient **n** takes into account any recombination of electrons and holes in the space-charge region.

EXAMPLE

Objective: Determine the current in a pn junction diode.

Consider a pn junction at $T = 300$ K in which $I_S = 10^{-14}$ A and $n = 1$. Find the diode current for $v_D = +0.70$ V and $v_D = -0.70$ V.

Solution: For $v_D = +0.70$ V, the pn junction is forward-biased and we find

$$i_D = I_S\left[e^{\left(\frac{v_D}{V_T}\right)} - 1\right] = (10^{-14})\left[e^{\left(\frac{+0.70}{0.026}\right)} - 1\right] \Rightarrow 4.93\,\text{mA}$$

For $v_D = -0.70$ V, the pn junction is reverse-biased and we find

$$i_D = I_S\left[e^{\left(\frac{v_D}{V_T}\right)} - 1\right] = (10^{-14})\left[e^{\left(\frac{-0.70}{0.026}\right)} - 1\right] \cong -10^{-14}\,\text{A}$$

Semiconductor devices

1. Microwaves devices

That works at frequencies band of microwaves (1Ghz to 3000Ghz) (300 to 0.01 cm)

a. Tunnel diode.
b. Back –word diode.
c. IMPATT diode (Impact ionization Avalanche Transition Time).
d. Baritt Diode.
e. Gunn Diode.

2. Photonic devices

Photonic devices are devices in which the basic particle of light—the photon—plays a major role

a. Light detection devices
   - photo detector devices
   - Solar cell

b. Light source devices
   - LED (light Emitting Diode)
   - LAESR (Light Amplification by stimulated Emission Radiation)

Designation	Frequency range (GHz)	Wavelength (cm)
VHF	0.1– 0.3	300.00–100.00
UHF	0.3–1.0	100.00–30.00
L band	1.0–2.0	30.00–15.00
S band	2.0–4.0	15.00–7.50
C band	4.0–8.0	7.50–3.75
X band	8.0–13.0	3.75–2.31
Ku band	13.0–18.0	2.31–1.67
K band	18.0–28.0	1.67–1.07
Ka band	28.0–40.0	1.07–0.75
Millimeter	30.0–300.0	1.00–0.10
Submillimeter	300.0–3000.0	0.10–0.01

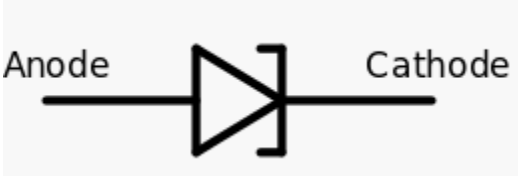
Tunnel diode

Definition of tunnel diode:

- A Tunnel diode is a heavily doped p-n junction diode in which the electric current decreases as the voltage increases and have very narrow depletion region.
- In tunnel diode, electric current is caused by "Tunneling".
- The tunnel diode is used as a very fast switching device in computers. It is also used in high-frequency oscillators and amplifiers.
- Leo Esaki observed that if a semiconductor diode is heavily doped with impurities, it will exhibit negative resistance.

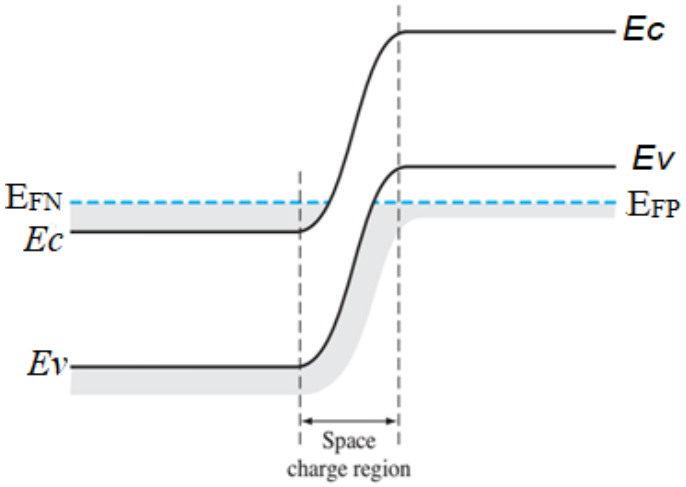
Applications of tunnel diodes:

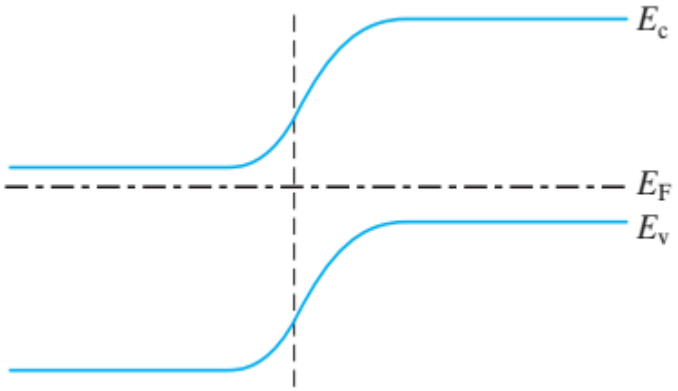
1. Tunnel diodes are used as logic memory storage devices.
2. Tunnel diodes are used in relaxation oscillator circuits.
3. Tunnel diode is used as an ultra high-speed switch.
4. Tunnel diodes are used in FM receivers.
5. Low voltage high frequency switching applications



Basic of tunnel diode:

- ✓ The fermi level is constant throughout the junction. we notice that E_{FP} lies below the valence band edge on the p-region and E_{FN} is above the conduction band edge on the n-region.
- ✓ Thus the bands must overlap on the energy in order for E_F to be constant.
- ✓ It means that with a small forward or reverse bias, a filled state and empty state appear opposite each other, separated by the width of the depletion region.





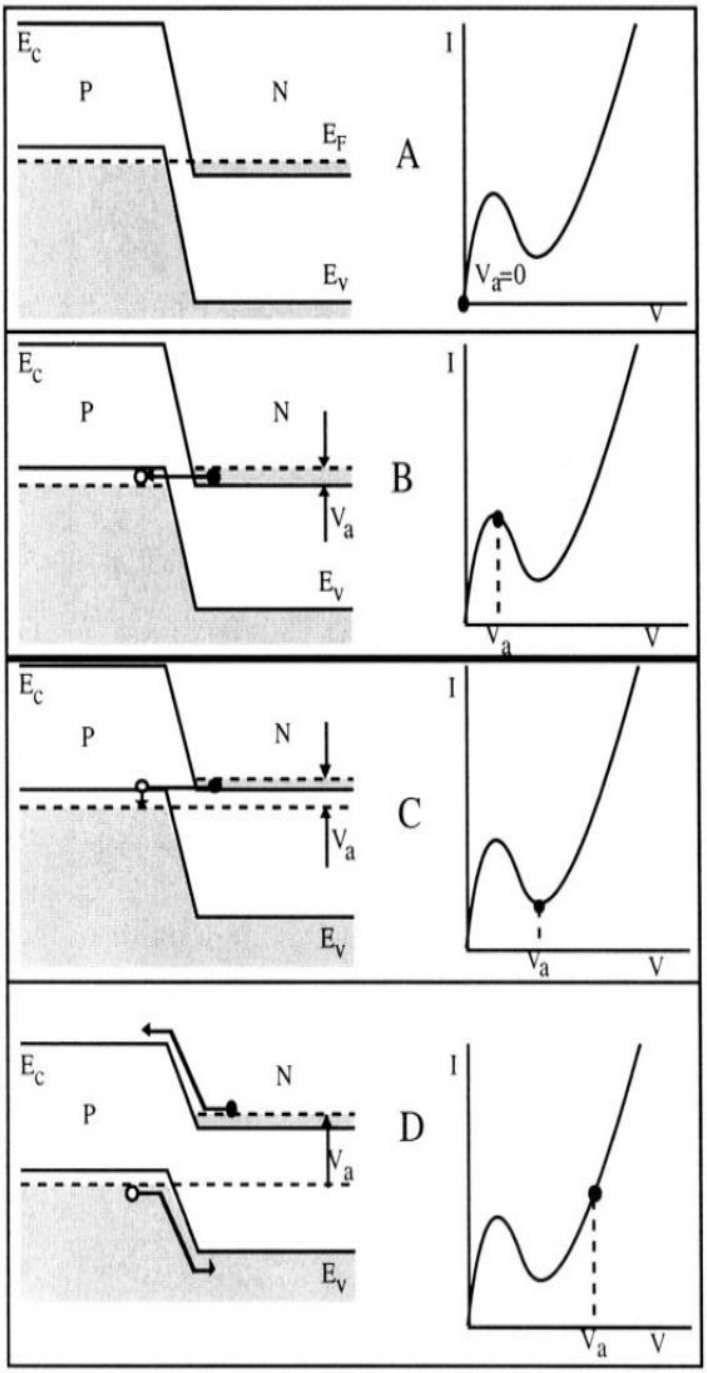
Basic of tunnel diode: (Forward bias)

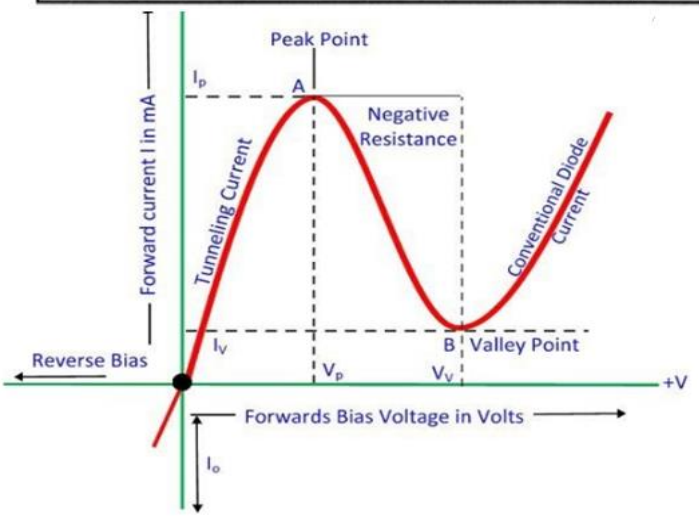
A. When no voltage is applied to the tunnel diode, the conduction band electrons at n-side and the valence band holes at p-side are nearly at the same energy level.
   But no electrons tunneling from n to p region. thus the net tunneling currents at zero applied voltage is zero

B. When a small voltage is applied to the tunnel diode which is less than the built-in voltage of the depletion layer, no forward current flows through the junction. However, a small number of electrons in the conduction band of the n-region will tunnel to the empty states of the valence band in p-region. This will create a small forward bias tunnel current. Thus, tunnel current starts flowing with a small application of voltage.

C. If the applied voltage is largely increased, the tunneling current drops to zero. At this point, the conduction band and valence band no longer overlap and the tunnel diode operates in the same manner as a normal p-n junction diode.

D. If the applied voltage continues to increase largely, there are no electrons on the n side directly opposite to empty states on the p side.
   For this forward- bias voltage, the tunneling current will be zero and the normal thermal current will exist in the device as shown in the I–V characteristics.

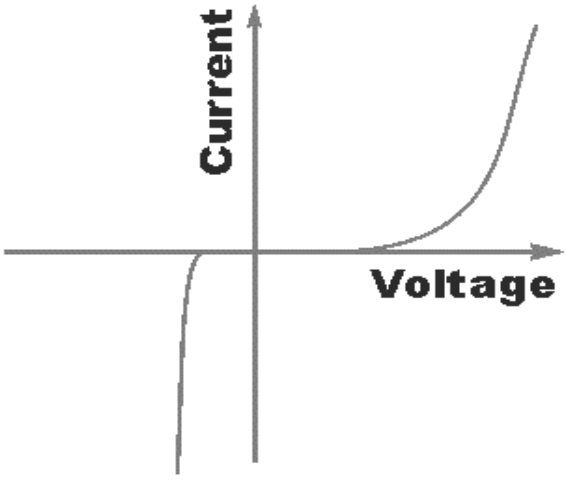




Back – word diode

Definition of back-ward diode:

- A backward diode is a form of tunnel diode where one side of the junction is less heavily doped than the other.
- This doping profile results in a diode that shares a number of characteristics with the tunnel diode, but modifies others. It means that in the reverse direction, the tunneling effect means that the diode has a characteristic similar to a normal forward biased PN junction diode.
- In the forward direction the tunneling effect is much reduced and it follows virtually the same characteristic as a normal PN junction diode.



Backward diode IV characteristic

Applications of Backward diode:

1. **Detector :** The backward diode provides a linear detection characteristic for small signals. Additionally the fact that there is no charge storage in its mode of operation means that it can be used for signals with frequencies extending to 50 GHz and more.

2. **Rectifier:** The diode is suitable for rectifying signals with peak voltages between about 0.1 and 0.6 volts

3. **Switch:** In view of its speed of operation, the diode is sometimes used for very high speed switching applications. It can be used as a switch within an RF mixer or multiplier where it provides excellent signal performance at microwave frequencies.

Lectures of Electrical Engineering Department

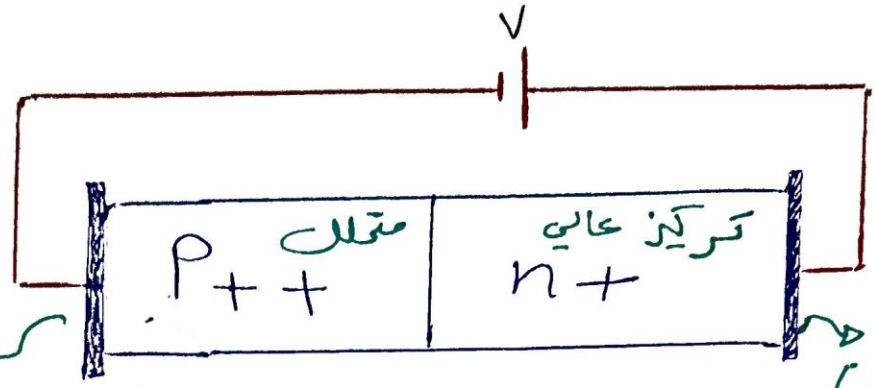
Subject Title: Microelectronics

Class: 4th Electronic and Communications

Lecture Contents	**Lecture sequences:**	**First lecture**	**Instructor Name:**
	The major contents: **1- Backward Diode** **2-** **3-** **4-**		
	The detailed contents: **1- Working principle** **2- Characteristics** **3- Applications**		

f.h.aldabbagh@uomosul.edu.iq عنوان البريد الاليكتروني F.H. Aldabbagh & Firas :اسم التدريسي

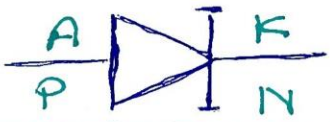
Backward diode — الثنائي العكسي



لماذا سُمّي بالثنائي العكسي ؟
لأنه يعمل بالانحياز العكسي.

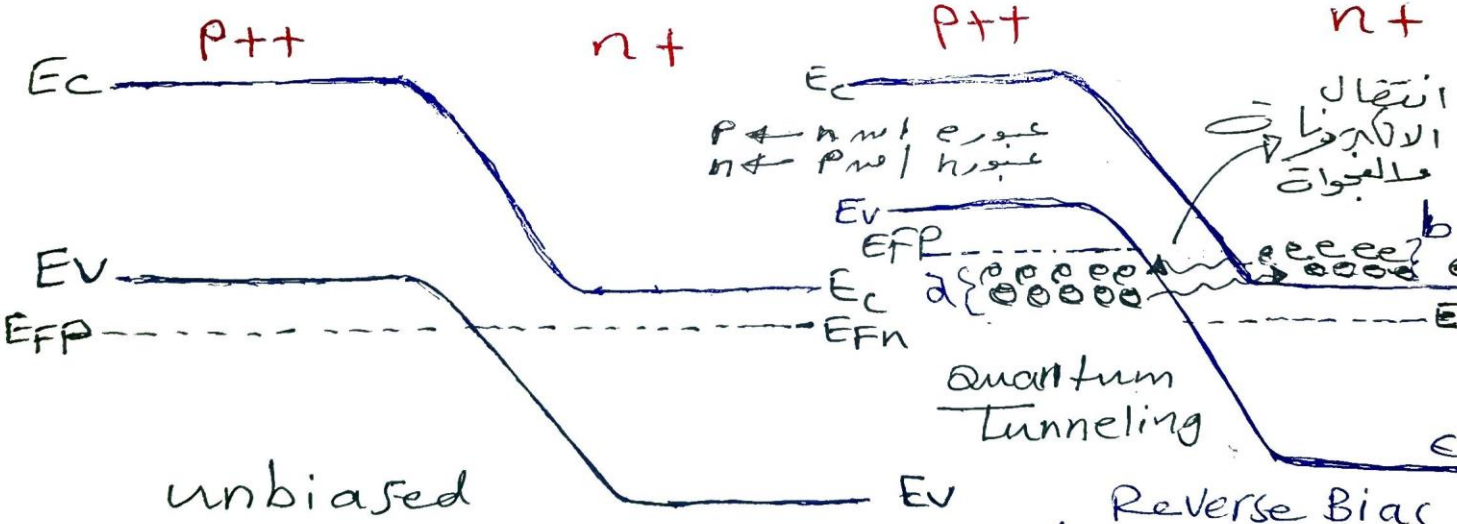
استخدامات هذا الثنائي :-
1- Rectifier
2- Switch
3- Detectors

رمز الثنائي :-



رمز الثنائي العكسي

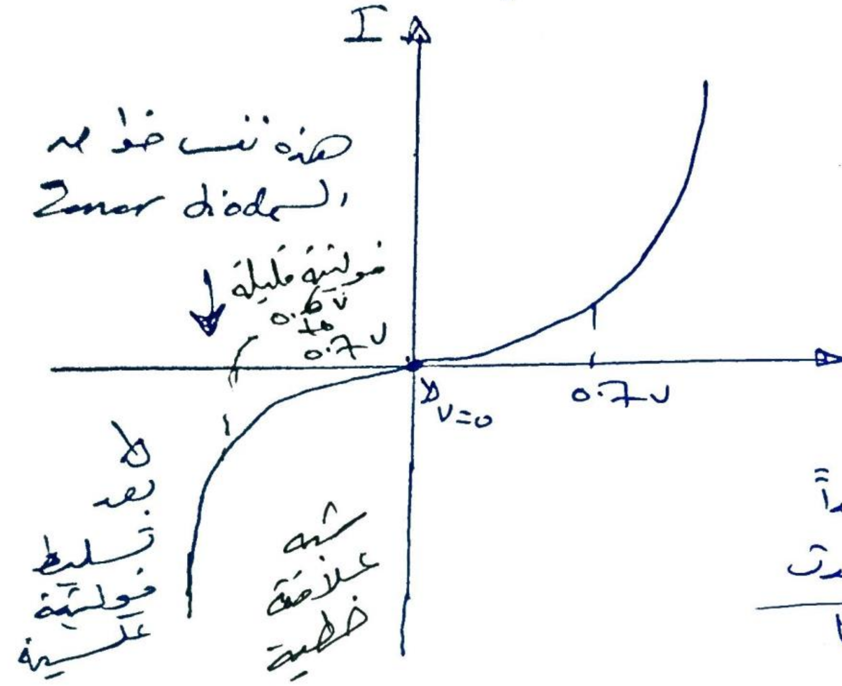
Band diagram of backward diode.



نلاحظ هنا ان EFP هي اسفل Ev عند الطرف P ؛ لأنه الطرف P مُطعّم بصورة كبيرة جداً (P++) وما أدنى إلى إخلاله ، أما الـ EFn فهو أسفل الـ Ec بقليل عند الطرف n ؛ لأنه الطرف n مُطعّم بصورة عالية (n+) ، ولم يحل

هنا نلاحظ الانحياز العكسي أرتفعت Ev للطرف P إلى الاعلى ، وأنخفضت Ec للطرف n بسبب الفولتية العكسية وما أدنى ما تقابل a مع b وبالتالي عبور e من n الى P وعبور h من P الى n

backward diode (also called back diode) having a better conduction for small reverse biases (for example -0.1 to -0.6V) than for forward bias voltage



الـ backward diode هو بالأساس شكل من أشكال الـ Tunneling diode كيف؟
لأن أحد المناطق (P++) المصنوع منها الـ Backword هي مطعمة بصورة عالية جداً (يعني فاسدة)، وبالتالي تحدث عملية النفق Tunneling

إذا سلطنا فولتية امامية على هذا الدايود (backward)
فإن ظاهرة النفق (Tunneling) سوف تقل بصورة كبيرة جداً
وسيسلك عندها هذا الثنائي (أي في حالة الانحياز بالاتجاه الامامي)
يسلك سلوك الثنائي الاعتيادي.

بينما في حالة الانحياز العكسي، نلاحظ تأثير ظاهرة النفق
Tunneling بصورة واضحة نتيجة تقابل أو تناظر المنطقتين
a و b كما في الرسم في صفحة 1
(عبور الالكترونات من منطقة n إلى منطقة P)
وبالنتيجة فإن خواص التيار - الفولتية لهذا
الثنائي في حالة الانحياز العكسي هي مشابهة لخواص
الـ Zenor diode

الرمز الـ backward

Lectures of Electrical Engineering Department

Subject Title: Microelectronics

Class: 4th Electronic and Communications

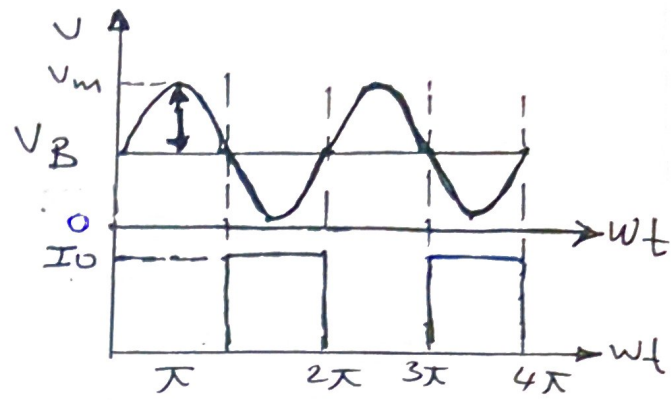
Lecture Contents	**Lecture sequences:**	**First lecture**	**Instructor Name:**
	The major contents: **1- IMPATT Diode** **2-** **3-** **4-**		
	The detailed contents: **1- Working principle** **2- Characteristics** **3- Applications**		

اسم التدريسي: F.H. Aldabbagh & Firas عنوان البريد الاليكتروني f.h.aldabbagh@uomosul.edu.iq

Efficiency : η :

كفاءة تحويل القدرة من dc إلى ac

$$\eta = \frac{\text{ac o/p power}}{\text{dc i/p power}}$$



$$\text{dc i/p power} = V_B * \frac{I_o}{2}$$

لماذا مقسوم على 2 : لأنه موجود خلال نصف الدورة (السالبة) فقط

ac o/p power

$$= \frac{1}{T}\int_0^T V_{ac} I \, d\theta = \frac{1}{2\pi}\left[\int_0^{\pi} V_m \sin wt + \int_{\pi}^{2\pi} I_o V_m \sin wt\right]$$

$= 0$ لأن التيار = صفر

$$\therefore \text{Ac o/p} = \frac{1}{2\pi}\left[I_o(-\cos wt)V_m\right]_{\pi}^{2\pi}$$

$$= -\frac{I_o V_m}{2\pi}\left[\overbrace{1-(-1)}^{2}\right]$$

$\cos 180 = -1$
$\cos 360 = 1$

الإشارة السالبة بالأقواس تدل:
على أن الدايود مولد للقدرة
لو كانت الإشارة + معناها
الدايود يستهلك القدرة

$$\text{Ac o/p power} = -\frac{I_o V_m}{\pi}$$

$$\therefore \eta = \frac{I_o V_m/\pi}{I_o V_B/2}$$

$$\boxed{\eta = \frac{2V_m}{\pi V_B} * 100\%}$$ قانون ثابت

عادة لا توضح الإشارة السالبة في قانون الكفاءة (التحمل).

نحن نفرضها دائماً $V_m(max)$

$$V_m(max) = \frac{3}{4} V_B$$

$$\therefore \text{output power}_{AC} = \frac{3}{4\pi} I_o * V_B$$

Induced External Current:-

The work done on the positive charge is:

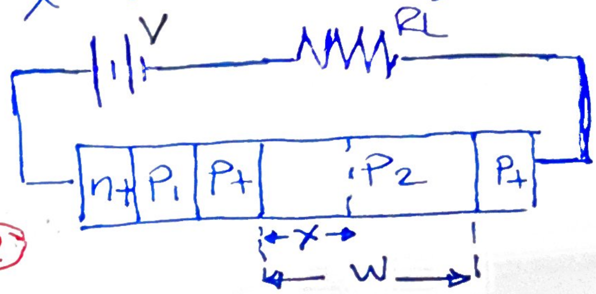
مسافة تحرك * قوة

$$W_h = F * X \longrightarrow (1)$$

مسافة تحرك = هي المسافة التي تقطعها الفجوات خلال المنطقة X

له الشغل للفجوات

الشغل اللازم لنقل الـ holes لمسافة x (منطقة P)



Where The Force F =

$$F = Q^{+} * E_o \longrightarrow (2)$$

له مقدار الشحنة الموجبة

مجال

معادلة (2) حسب قانون lenz law

and The Electric field =

$$E_o = \frac{V_o}{W} \longrightarrow (3)$$

المجال = فولتية / مسافة

لأنه حسب قانون الفولتية والذي يساوي المسافة * المجال = فولتية

$\because V = E * b$

$\therefore E = \frac{V}{b}$

The dc power supply does work in transferring the charge Q' through the external circuit which is given by:

external

$$W_e = V_o * Q' \longrightarrow (4)$$

له الشغل للمصدر

الشحنة المنقولة إلى الدائرة الخارجية

We = الشغل المنجز في المصدر

يساوي الشغل المنجز في نقل الفجوات داخل المنطقة (Wh)

معادلة (4) حسب قانون الفولتية

$V = \frac{J}{C}$

J = شغل = W

C = شحنة = Q

That's mean $W_e = W_h$

$W_e = W_h$ ⟶ ① عدد الجسيمات = ④ عدد الجسيمات

$$Q^+ E_0 \chi = V \bar{Q}$$

$$Q^+ \frac{V}{w} \chi = V \bar{Q}$$

$$\therefore Q^+ \frac{\chi}{w} = \bar{Q}$$

$$\bar{Q} = \frac{Q^+}{w} \chi$$

كمية الشحنة المنقولة

I_e = external current

I_o = output current

$I_e = I_o$

نشتق الطرفين بالنسبة للزمن

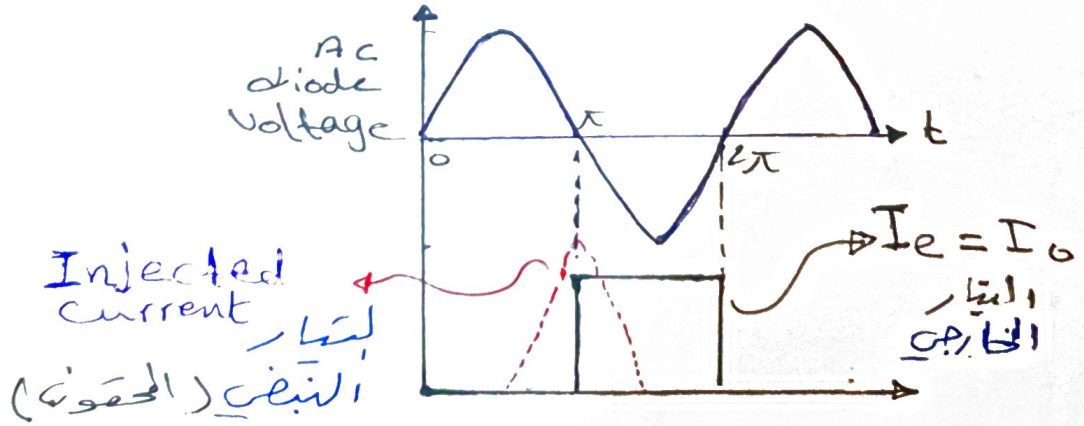
$$\frac{d\bar{Q}}{dt} = \frac{Q^+}{w} \frac{d\chi}{dt}$$

$$\frac{d\bar{Q}}{dt} = I_e : I_o$$

سرعة $= \frac{d\chi}{dt} = V_s$ سرعة الإشباع للإلكترون $= 10^7 \frac{cm}{sec}$

$$\therefore I_o = I_e = \frac{Q^+}{w} V_s$$

$I_o = I_e$ = The current in the External circuit.



Example: Consider a Read diode with $W = 5\,\mu m$, $v_s = 10^7 \frac{cm}{sec}$ and a Valanche-generated Number of holes $= 6 \times 10^7$ holes or (charge). determined the induced external current and the frequency.

Solution:-

The total +ve charge generated by the avalanche multiplication process is:

$$Q^+ = 6 \times 10^7 \times 1.6 \times 10^{-19}$$
$$= 9.6 \times 10^{-12} \text{ Coul} \quad .(c) \quad \text{كولوم}$$

التيار الخارجي المستحث

$$I_0 = I_e = \frac{Q^+}{W} v_s$$

$$I_0 = I_e = \frac{9.6 \times 10^{-12}}{5 \times 10^{-4}} \times 10^{+7}$$

$$I_0 \therefore I_e = 192 \text{ mA}$$ التيار الخارجي

$$f = \frac{v_s}{2W}$$

$$f = \frac{10^7}{2 \times 5 \times 10^{-4}}$$

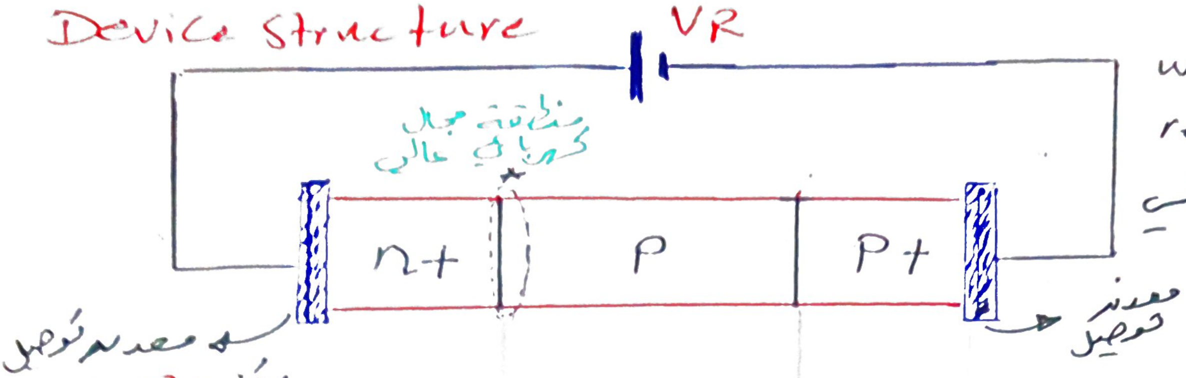
$$\therefore f = 10 \text{ GHz}$$

IMPATT diode :-

Impact ionization avalanche transit time

ثنائي زمن العبور الانهياري بالتأين الإصطدامي

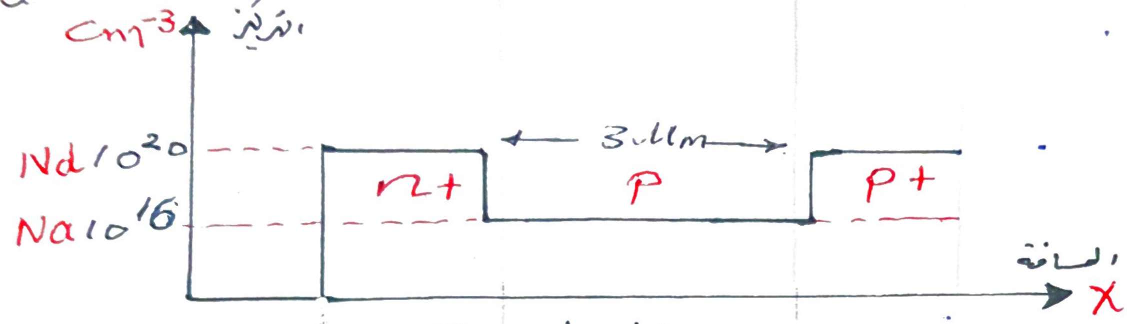
Device Structure



works only in reverse bias

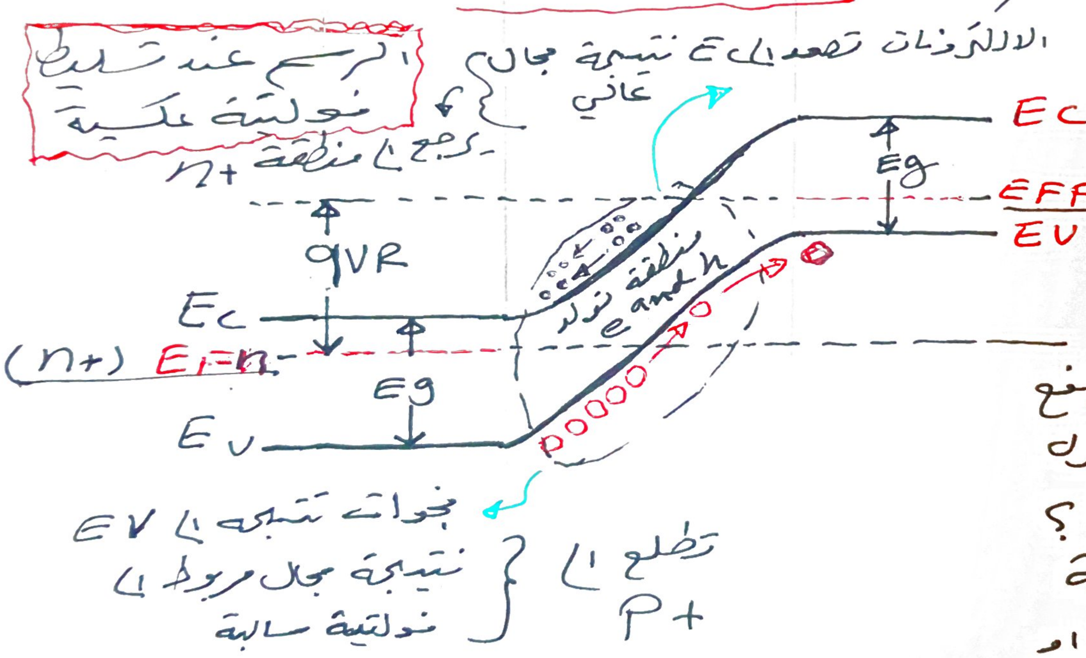
يعمل في الانحياز العكسي فقط

استخداماته :- يستخدم في توليد الموجات الدقيقة



مخطط الطاقة

Band diagram



منطقة مجال عالي

* منطقة تأين هي المنطقة التي يتولد فيها أزواج من الالكترونات والفجوات.

عند تسليط فولتية عكسية، طرف P يرتفع الى الأعلى وطرف n ينزل الى الأسفل لماذا؟ لأن الشوائب الثلاثية B مثل بورون من P تبدي ام تمارس قوة جذب أقل (قليلة) على الالكترونات الفلات الخارجي مقارنة مع الشوائب الخماسية. راجع حص 21 Ev

ما معنى n+ : مستوى فيرمي قريب جداً Ec ، P+ : مستوى فيرمي قريب جداً

ما معنى n++ : مستوى فيرمي فوق الـ Ec ← Degenerated

Operation Mechanism: الخواص الميكانيكية

في منطقة المجال الكهربائي العالي ، والتي تكون قريبة من القطب الموجب لفولتية الانهيار : يعني منطقة $n^+ p$

يحصل انهيار للذرات حيث ينفصل الالكترون عن الفجوة مولداً زوجاً من (e+h) ، وتكون طاقة هذا الالكترون أو الفجوة عالية وعندما تصطدم هذه (e+h) بالذرات الأخرى ، يتسبب انهيار للذرة ، مولداً هذا الانهيار زوجاً آخر من (e+h) وهكذا يتوالى التوالد أو التولد والانهيار (التتالي) للذرات حسباً تضاعف التيار العكسي (تضاعف الحاملات h-e)

تسمى هذه العملية : بالتضاعف التيهوري يعني تضاعف انهياري ، وتكون هذه العملية (التضاعف التيهوري) تكون بشكل خوائي

من ايجابيات هذه العملية : —

١- قدرة عالية
٢- تردد عالي بحدود 30GHZ
٣- كفاءة عالية

من سلبيات هذه العملية :—

- زيادة الضوضاء في الاشارة المايكروية المتولدة

الفولتية العكسية اللازمة لهذا الدايود : هي الفولتية التي يحدث عندها الانهيار للذرات حيث تنفصل elec عن الهول (ما يؤدي) الانهيار التيهوري ، وتسمى هذه الفولتية بـ فولتية الانهيار VB = VBreak Down Voltage

كذلك تسمى فولتية الانهيار Break Down Voltage
تسمى أيضاً بفولتية التأين Ionization Voltage

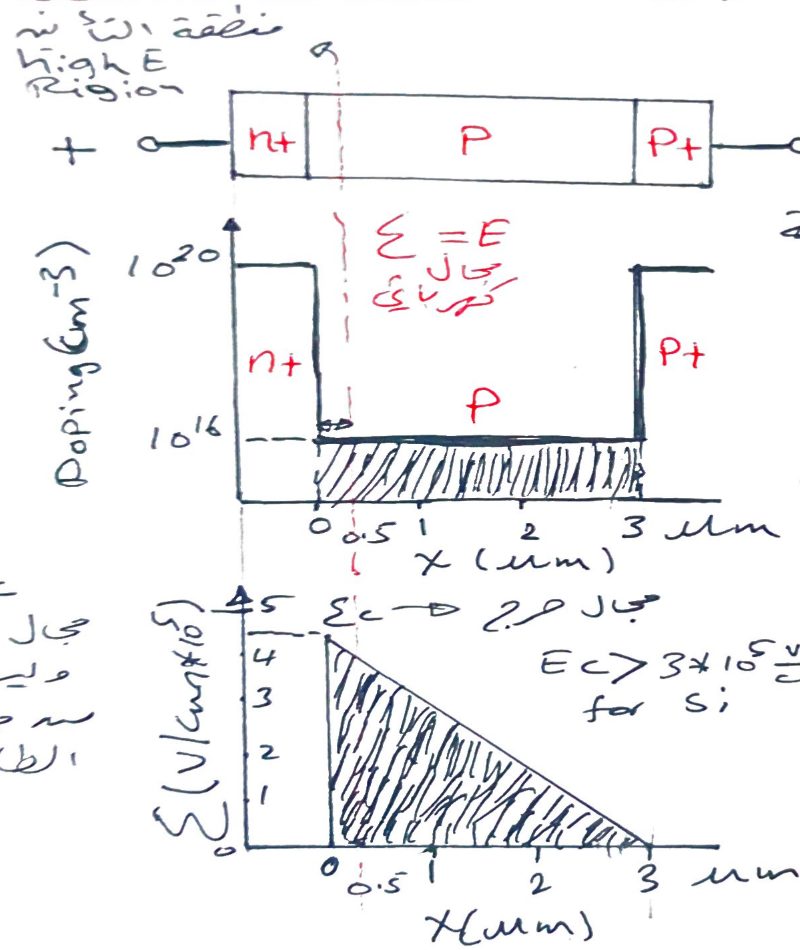
ملاحظة:
لماذا يكون عندنا في هذه العملية لـ الثنائي التيهوري يكون ضوضاء عالية ← High noises
لأنه تحدث بشكل عشوائي

ملاحظة: عند تسليط فولتية عكسية ← يتولد شدة عالية من تيار عالي (ثابت)

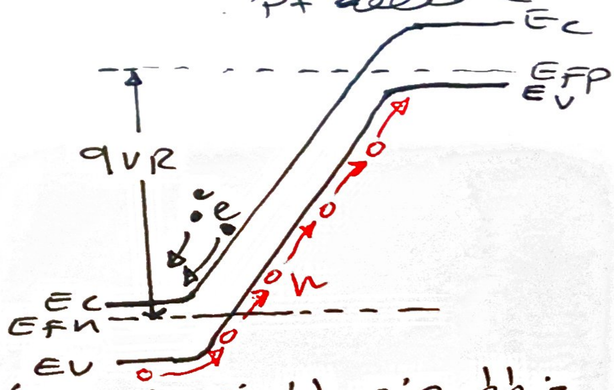
Electric field

ملاحظة: التأين يعتمد بشكل كبير على المجال الكهربائي

إن معظم الأزواج (e − h) تتولد في منطقة المجال الكهربائي العالي، أي في المنطقة $0 \leq X < 0.5\,\mu m$ حيث أن المجال الكهربائي $\mathcal{E}$
$\mathcal{E} > 3*10^5\ V/cm$
فالالكترونات المتولدة تنتقل فوراً إلى منطقة $n+$ أما الثقوب المتولدة فإنها تنجرف عبر منطقة P إلى منطقة $P+$



Ec مجال حرج وليس من مخطط الطاقة



مخطط حزم الطاقة عند الانهيار

qVR (EFP − EFn)

إن الوقت المستغرق لحين وصول الثقوب إلى منطقة $P+$ القادمة من منطقة التأين عبر P يسمى أو يؤلف تأخر زمن العبور

يسمى زمن تأخر العبور بـ Transit time delay

ملاحظة: مسافة الانهيار بحدود 0.5 μm والواقعة ضمن منطقة P يسمى المجال الكهربائي بالمجال الحرج Ec Critical Electric Field.

ويجب ان يكون $Ec \geqslant 3\times10^5 \frac{V}{cm}$ لغرض التأين

ملاحظة: إن الفجوات المتولدة في منطقة الانهيار تحتاج الى زمن لعبور منطقة P والوصول الى منطقة P+

وكلما قلّ زمن العبور كلما زادّ التردد للإشارة المتولدة ويعتمد الزمن على الفولتية المسلطة بحيث يتناسب تناسب عكسي مع الفولتية المسلطة

إذاً يتناسب تردد الإشارة المتولدة طردياً مع الفولتية المسلطة (العكسية)

ملاحظة: أخذنا بنظر الاعتبار زمن العبور للفجوات فقط عبور الفجوات من منطقة الانهيار (التأيين) الى منطقة P+ عبر P.

ثم تأخذ بنظر الاعتبار زمن عبور e ؟!

لان الالكترونات ما تحتاج زمن للعبور هي (electrons) متولدة في منطقة الانهيار ومباشرة تتجه الى منطقة n+ القريبة منها جداً

ملاحظة: عندما يصبح المجال الكهربائي E مساوياً للصفر عندها (at 3μm) سوف تقل سرعة الحاملات (الفجوات)

وحل هذه المشكلة: تم تطوير وتحسين بنية الدايود ليصبح بالشكل الآتي

والشكل الجديد للديود (المقترح) يسمى ب Read Diode

كان العالم Read: أول من قدم المقترح الاصلي لتصميم نبيطة موجات دقيقة من فصيلة Impatt يكون امجال الكهربائي لهذه النبيطة الجديدة $\vec{E}$ ثابتاً في منطقة الاستنزاف وسمي هذا الديود ب Impatt Read diod

هذه النبيطة الجديدة أو الديود الجديد مؤلف من

$$n^+ - p - \pi - p^+ \quad \text{أو} \quad n^+ - p - i - p^+$$

i = Intrinsic متعادل الشحنات (h عدد = e عدد)

π = معناها تركيز الفجوات أعلى من حالة Intrinsic ⟸ π = قريب من شبه موصل نقي (أغلبية فجوات)

ومن ثم قام هذا العالم بتقسيم المنطقة الوسطية P الى منطقتين الأولى P_1 ذات التطعيم العالي نسبياً وبعرض $(0 \leq x \leq b) = 0.5\mu m$ وهي المنطقة التي يحدث فيها الانهيار ديودي (التضاعف التيهوري) ويكون المجال الكهربائي متغيراً. (مجال عالي)

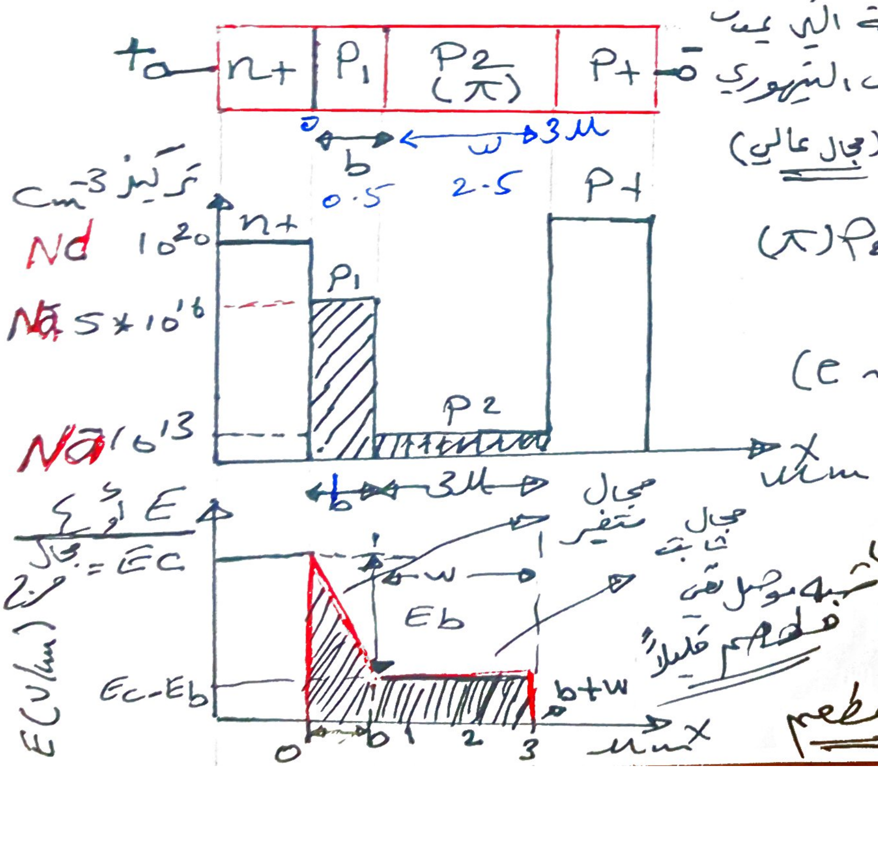
أما المنطقة الثانية: هي منطقة $P_2(\pi)$ ذات التطعيم الجوهري تقريباً شبه موصل نقي (فجوات أكثر من e) وذات المجال الكهربائي الثابت

منطقة P_1 = منطقة توليد (e+h)

منطقة P_2 = عرضها $W = 2.5\mu m$

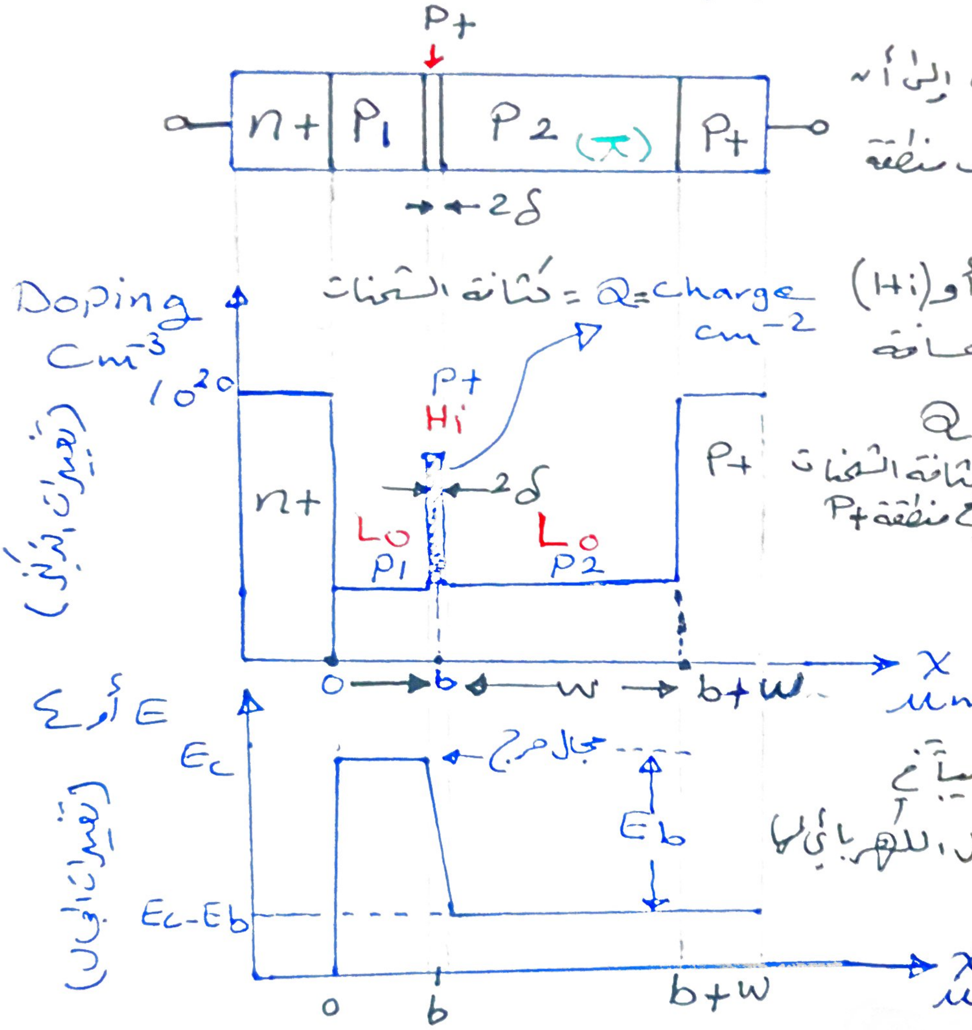
ملاحظة: $1 \times 10^{13}\ cm^{-3}$

شبه موصل نقي غير مطعم $1.5 \times 10^{10}\ cm^{-3}$



Modified Read diode Lo-Hi-Lo

هو عبارة عن ثنائي محوّر Read ، يسمى بـ تركيبة واطئ عالي - واطئ (Lo-Hi-Lo). حيث كمية كبيرة من الشحنات Q موجودة عند $x=b$ ، والتطعيم في P_1 و P_2 قريب من الحالة الجوهرية



ملاحظة: يجب الانتباه إلى أن نقطة b على محور x هي منتصف منطقة (Hi) P+.

عرض أو مسافة P+ أو (Hi) هو 2δ ، حيث δ = مسافة

$$Q = 2\delta \, Na(P+)$$

كثافة الشحنات في منطقة P+ = مسافة * تركيز منطقة P+

$$2\delta \cong 0$$

لأن منطقة ضيقة جداً لذلك يهمل

ملاحظة: منطقة P_1 تقريباً في الحالة الجوهرية، فإن المجال الكهربائي لها يبقى ثابتاً ما بين $x=0$ و $x=b$ وعند $x=b$ فإن كمية الشحنات الكبيرة أو الكثيرة تسبب انخفاضاً بالمجال الكهربائي بمقدار E_b وفي منطقة $b \leq x \leq b+w$ فإن المجال الكهربائي يبقى ثابتاً.

ملاحظة: $10^{20}\,cm^{-3}$ معناها $\frac{Charge}{cm^{3}}$

شحنة * تركيز = $\frac{charge}{cm^{3}}$

charge → coulomb

المجال الكهربائي = $\frac{\text{كمية الشحنة}}{\epsilon_s}$ ، ϵ_s = سماحية العازل

معادلة -1-: $E_b = \frac{qQ}{\epsilon_s}$ (شرط أن الشحنة بالمساحة)

V_B = المساحة تحت المجال = فولتية الانهيار

معادلة -2-: $V_B = E_c b + w[E_c - E_b]$

معادلة -3-: $V_B = E_c b + w\left[E_c - \left|\frac{qQ}{\epsilon_s}\right|\right]$

q هي نفسها $e = 1.6 \times 10^{-19}\,C$

$$V_B = E_c\, b + W\left[E_c - \left|\frac{e(2\delta) N_a (P+)}{\epsilon_s}\right|\right]$$

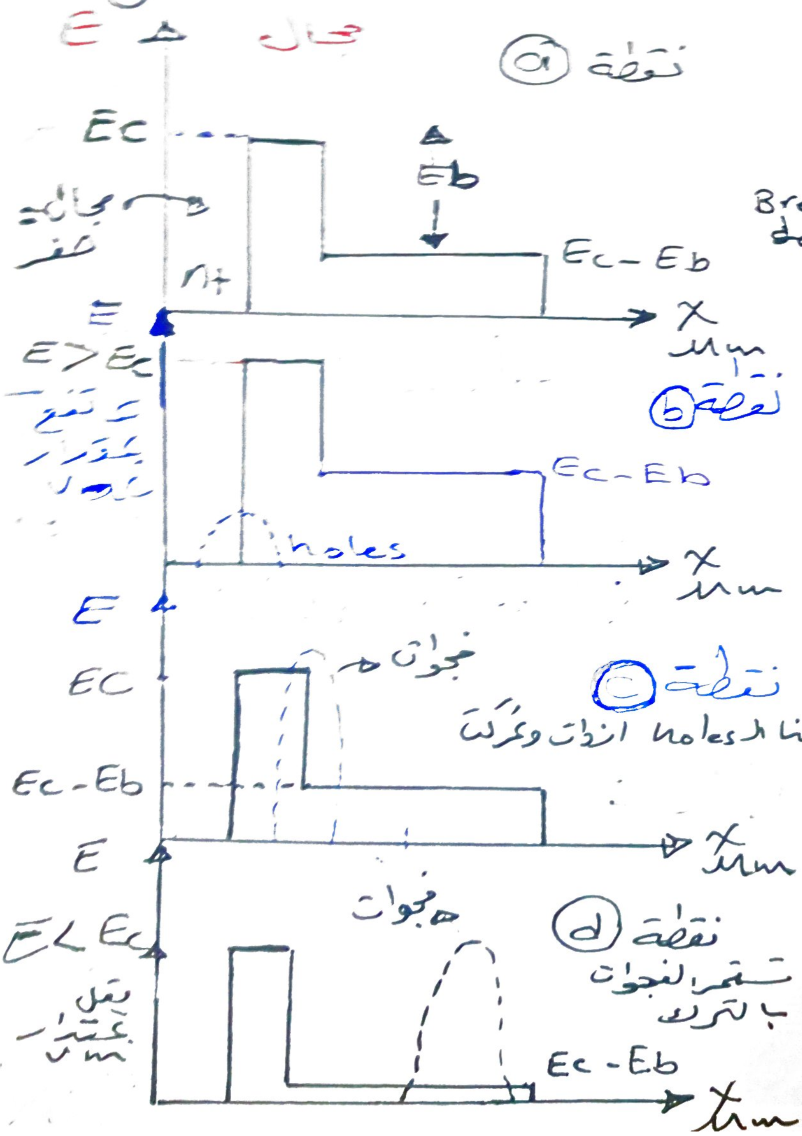
لأن $Q = 2\delta N_a (P+)$ = تركيز الشحنات

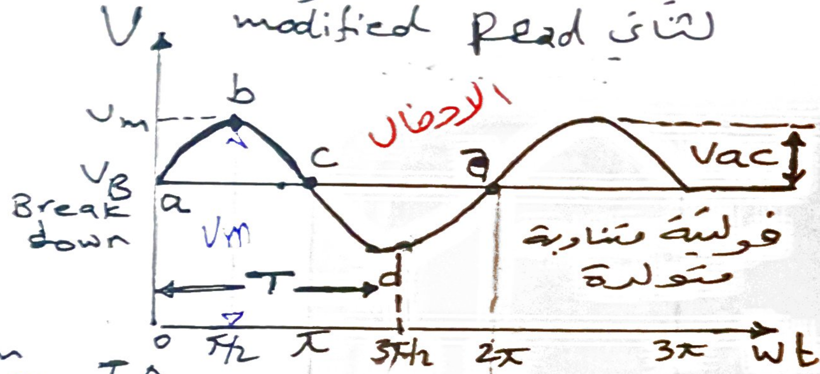
$q = e = 1.6 \times 10^{-19}$ الوحدة الشحنة

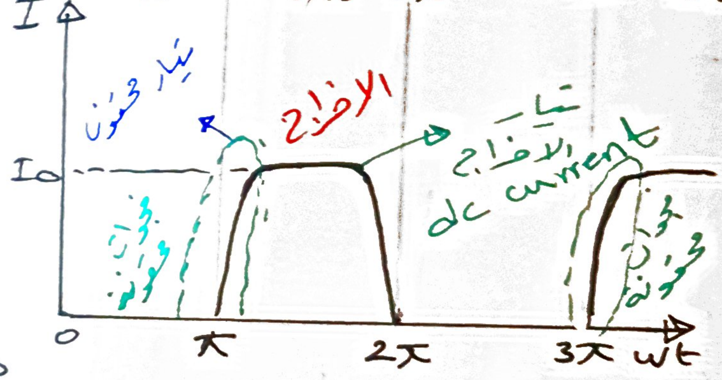
ϵ_s = سماحية العازل $= F/cm$

ملاحظة: بسبب منطقة المجال الكهربائي العالي المنتظم تقريباً $0 \leq x \leq c$ يمكن إبقاء قيمة المجال الحرج E_c ودرجة حرارة التشغيل أوطأ مما هي عليه في ثنائي Read . (هذه هي فائدة modified Read)

Dynamic Characteristic المميزات الداينميكية لثنائي modified Read







نقطة b = حدث تأين بالذات

تيار الانجراف = dc current

$V_{ac} + V_B = V_m$

V_B = فولتية مستمرة مسلطة بصورة عكسية على الدايود

ملاحظة :-
الفولتية المتناوبة (الادخال) هي نتيجة وجود ثنائي زينر (العمل) في دائرة لموجات دقيقة ، يعني هذه الفولتية المتناوبة المركبة فوق الفولتية المستمرة (VB) هي من مولدة الدائرة المربوط بها الثنائي.

ملاحظة :- في منطقة الانهيار (الزينري) تتولد فجوات والكترونات في نفس الوقت ، لاحظ الرسم في صفحة 7- نقطة b.

نلاحظ تولد فجوات وهذه الفجوات سوف تتحرك وتبقى منطقة الأنجراف متجهة نحو الطرف p+

أما الالكترونات المتولدة في منطقة التأين لم نقم بدراستها وأن هذه الالكترونات المتولدة في منطقة الانهيار (الزينري) سوف تتجه نحو الطرف n+.

ملاحظة :-
عندما تهبط الفولتية المتناوبة موجبة ، تضاف اذاد جديدة من الثقوب المتولدة في منطقة (الانهيار أو الزينري) ، وكما مبين بالخطوط المنقطة في صفحة 7- (نقطة b)
وتستمر الثقوب بالزيادة طالما المجال الكهربائي أعلى من Ec وبذلك فأن الثقوب تصل الى الذروة ليس عند $\pi/2$ حيث الفولتية عند القيمة القصوى بل عند π راجع صفحة 7- نقطة c

ملاحظة :- نستنتج من الرسم في صفحة 7 ، أن هناك فرق طور بين الادخال والاخراج - ونلاحظ من الرسم أنه كلما قلت الفولتية زاد التيار وهذا يعني ان المقاومة سالبة وبذلك يكون هنالك توليد للقدرة ، و نتيجة لـ التقلبات العشوائية في عملية التضاعف الزينري تكون الضوضاء عالية

ملاحظة: إن الحاملات المحمولة (النجوات) تقطع المسافة W وهي طول منطقة الاستنزاف خلال النصف السالب للذبذبة (ولهذا السبب يظهر في النصف السالب من الموجة)

$T = \frac{1}{f}$ ، $t_r = \frac{1}{2} T$ زمن العبور

$t_r = \frac{1}{2} \frac{1}{f}$ W = مسافة

V_s = سرعة النجوات

أو $t_r = \frac{W}{V_s}$ سرعة النجوات = سرعة الانسياق

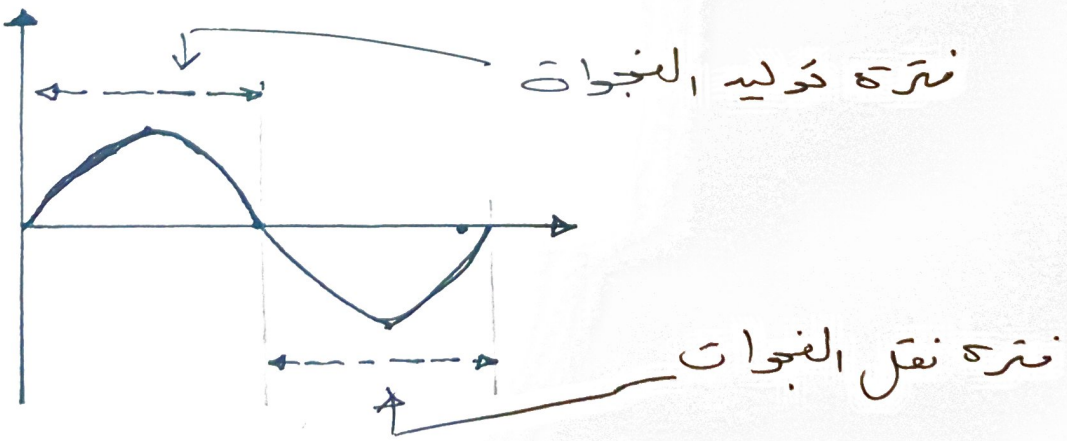
V_s = سرعة الانسياق

سرعة = $\frac{\text{مسافة}}{\text{زمن}}$ $V_s = 10^7 \frac{cm}{sec}$ for Si

$\text{زمن} = \frac{\text{مسافة}}{\text{سرعة}} = \frac{W}{V_s}$

$\frac{W}{V_s} = \frac{1}{2f}$ ، $2f W = V_s$

$$\therefore f = \frac{V_s}{2W}$$



ملاحظة: المقاومة السالبة، يعني توليد (للقدرة).

Example :- أحسب التردد الناتج من ثنائي IMPATT
إذا علمت أن سرعة انسياق الفجوات $10^7 \frac{cm}{sec}$
وطول منطقة الانزلاق $W = 2\,\mu m$

$$F = \frac{V_s}{2W}$$

الحل:

$$f = \frac{10^7 \frac{cm}{sec}}{2 * 2 * 10^{-4} cm} = \frac{10^{11}}{4}$$

cm إلى μm حولنا

$$f = \frac{\frac{cm}{sec}}{cm}$$

$$f = \frac{cm}{sec} \cdot \frac{1}{cm} = \frac{1}{sec}$$

دائماً بالـ $W = cm$

∴ التردد المتولد $f = 25\ GHZ$

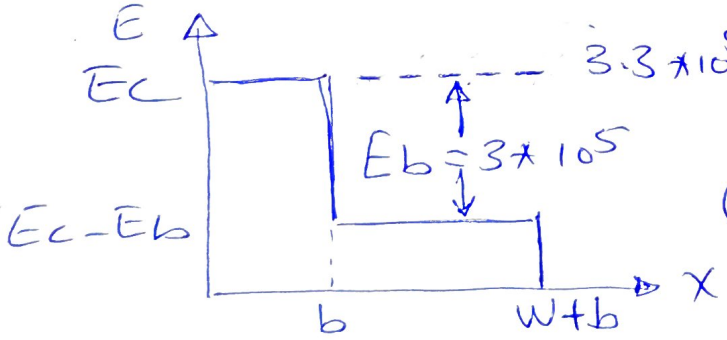
Example: في بنية سيليكون ذات التركيب Lo-Hi-Lo

$b = 1\,\mu m$ $(P_2 = \pi)$
$W = 5\,\mu m$ $(P_1 = P)$

$n+ - P - p + \pi - p+$
Lo Hi Lo

فإذا كانت $Q = 2 * 10^{12} \frac{charg}{cm^2}$ ما هي الفولتية اللازمة للانهيار (V_B)
لعمل هذه البنية وما تردد الثنائي إذا علمت أن منطقة التيار منتظمة بطول 1 μm تتبعها فولتية dc وقدرها 33 V للانهيار / $(\epsilon r = 11.7)$.

الحل:



$Ec - Eb$
$(3.3 - 3) * 10^5$
$= 0.3 * 10^5 \frac{V}{cm}$

الحجل = الفولتية قبل الانهيار

$$Ec = \frac{V}{b} = \frac{33V}{1 * 10^{-4}} = 3.3 * 10^5\ V/cm$$

$$V_B = Ecb + \left[Ec - \frac{qQ}{\epsilon_s}\right] W \quad \text{(Eb)}$$

$$V_B = 33 + \left[3.3 * 10^5 - \frac{1.6 * 10^{-19} * 2 * 10^{12}}{11.7 * 8.85 * 10^{-14}}\right] 5 * 10^{-4}$$

$$V_B = 33 + 13 \cong 44V$$

$$f = \frac{V_s}{2W} = \frac{10^7 cm/sec}{2 * 5 * 10^{-4}} = 10^{10} Hz = 10\ GHz$$

Lectures of Electrical Engineering Department

Subject Title: Microelectronics

Class: 4th Electronic and Communications

Lecture Contents	**Lecture sequences:**	**First lecture**	**Instructor Name:**
	The major contents: **1- BARITT DIODE** **2-** **3-** **4-**		
	The detailed contents: **1- Working principle** **2- Characteristics** **3- Applications**		

اسم التدريسي: F.H. Aldabbagh & Firas عنوان البريد الاليكتروني f.h.aldabbagh@uomosul.edu.iq

BARITT Diode:

BARrier Injection Transit Time Diode

ثنائي زمن العبور عند الحقن خلال الحاجز.

*** يعمل على توليد موجات دقيقة

** الآلية الأساسية عند نقل الحاملات (holes) في هذا الثنائي تعتمد على ① الحقن الترموايوني (ايونات متولدة بالحرارة)

② وانتشار الحاملات وهي الفجوات، يكون: عند حاجز جهد أمامي (جهد حاجز)، ومن خلال منطقة الإنجراف (منطقة عبور الحاملات) ③ وعلى الرغم في عبور هذه الحاملات

** نظراً لعدم وجود التضاعف الانهياري (التيفوري) فإن ① الضوضاء تكون قليلة، وبالمقابل ② تكون القدرة قليلة، وبالتالي ③ تكون الكفاءة أقل مما هي في حالة الـ IMPATT.

** إن الجهود الأدنى للضوضاء (مقارنة مع Impatt) والاستقرارية العالية لهذا الثنائي، يجعله مناسباً في التطبيقات ذات القدرة الواطئة

(كالمذبذبات المحلية Local oscillators)

و (كاشف دوبلر Doppler detectors)

ملاحظة: تكون القدرة قليلة، يعني القدرة الخارجة قليلة

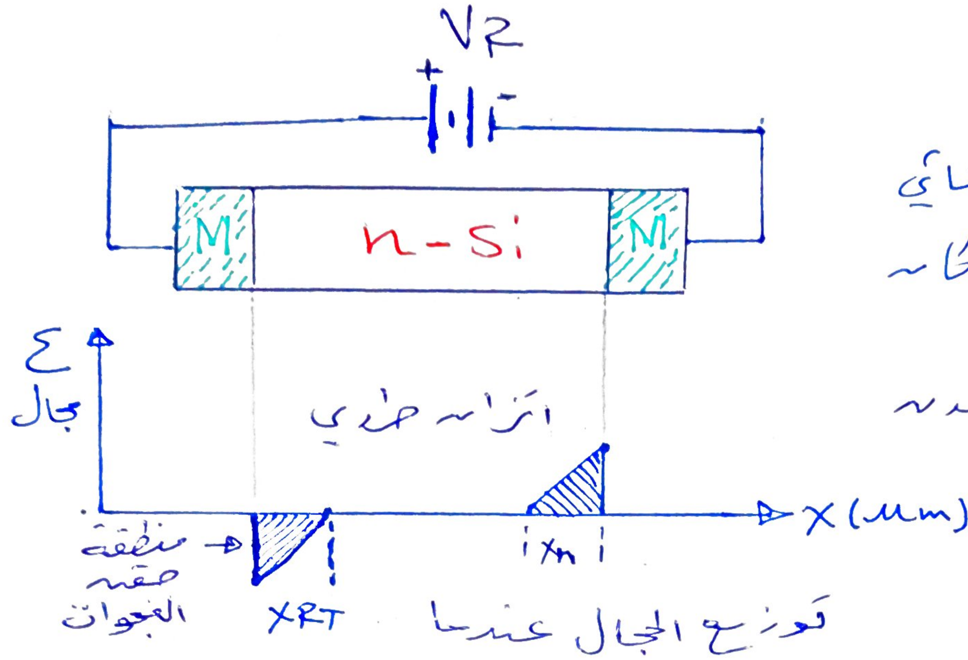
ملاحظة: تكون الضوضاء أقل في عملية الحقن الترموايوني مقارنة مع الضوضاء في عملية التأين الاصطدامي.

(ضوضاء) BARITT < IMPATT (ضوضاء)

Device Structure :- بناء النبيطة ②

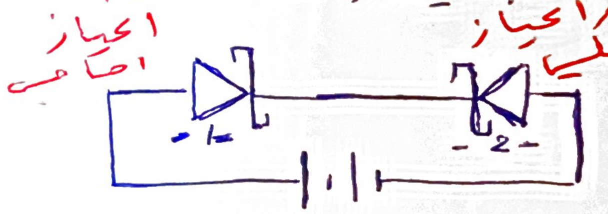
M = Metal معدن
n-si = n-type silicon

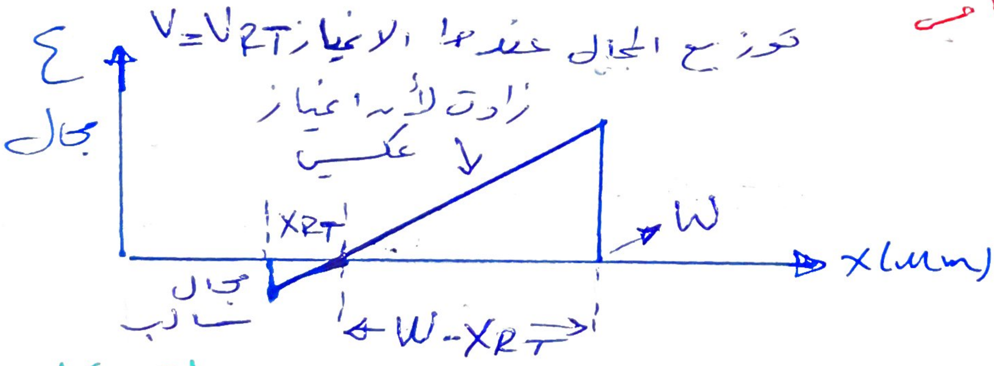
أمكن الحصول على أول ثنائي يعمل بصيغة كـ BARITT باستخدام التركيب معدن - شبه موصل - معدن
M Si - M
وهذا الثنائي هو بالأساس عبارة عن ثنائيين من نوع شوتكي دايود مربوطين بالتعاكس



توزيع المجال عندما الانحياز = صفر ← VR = 0

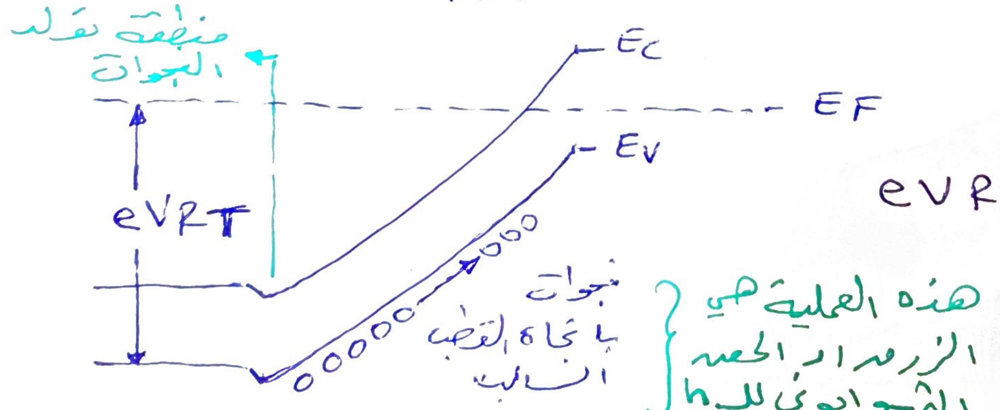
XRT = منطقة حقن الفجوات





عند تسليط انحياز كافٍ على النبيطة فإن المجال الكهربائي يغطي كل النبيطة

eVRT = فولتية الانحياز المسلطة التي تسبب الحقن



هذه العملية هي الازدياد الحقن الانهياري للـn

نقطة الحقن للفجوات

Energy Band diagram.

عند زيادة VR يزداد الحقن

ملاحظة: يكون انتشار الحاملات (الفجوات) عبر الجهد الحاجز بانحياز امامي وليس عكسي، لان شوتكي دايود رقم -1- فيه انحياز امامي

ملاحظة: منطقة التولد (الحقن) للفجوات هي المنطقة التي يبدأ عندها المجال الكهربائي بالإزدياد (XRT)

ملاحظة: عندما سلطنا فولتية على الثنائي وكانت قيمتها $V = V_{RT}$، معنى ذلك: سلطنا فولتية بحيث تشابك أو تعاكس المجال السالب مع المجال الموجب صفحة ③ [رسم المجال الكهربائي].

∴ عملية تشابك المجالين ضرورية لحدوث الحقن الإنحيازي وذلك سمي الفولتية المسلطة لأجل التشابك بـ V_{RT}

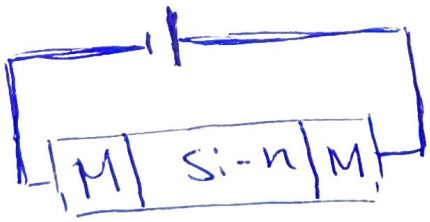
VReach Through
Forward and Reverse field are Interleaved.

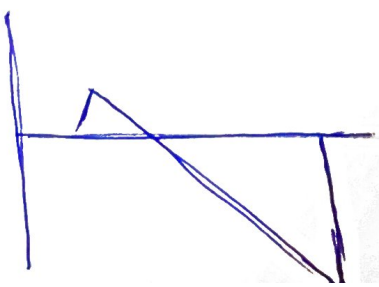
ملاحظة: عند زيادة V_{RT} ← يزداد الحقن ← يزداد التردد

ملاحظة: سرعة الإنجراف للفجوات في منطقة الحقن (XRT) تكون قليلة ؟ لماذا ؟!

لأنه المجال الكهربائي في منطقة الحقن ليكون واطئ وهي أقل من سرعة الإشباع V_s

ملاحظة: اذا سلطنا فولتية عكس الفولتية المسلطة صفحة ③ يكون شكل المجال الكهربائي أيضاً بالعكس (صفحة ①)



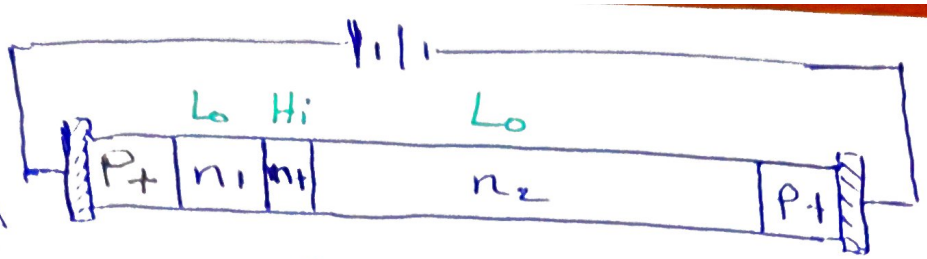


ملاحظة: تقطع الثقوب الحقونة منطقة الانجراف XPT وهي تلامس المعدن شبه الموصل على البعيد ويشار إلى الزمن المستغرق للوصول إلى التلامس المعدني ببناء زمن العبور transit delay time.

لأجل تقليل الفولتية المطلقة على الثنائي (البنيطة) إلى الحد الأدنى مع الإبقاء على مجال كهربائي كافي في منطقة الانجراف للحصول على سرعة الانسياق تم تصنيع ثنائي جديد يمثل البنية الثانية لثنائي BARITT، حيث تلاحظ (مجموعة او مجموعات) من الشحنات توجد عند نقطة الحقن، ويجب ان تكون كمية الشحنة وموقعها محدد (مختار) بشكل مناسب لغاية تقليل الفولتية المطلقة الى حد معين يضمن الحصول على المجال الكهربائي الكافي في منطقة الانجراف والحصول على سرعة انسياق و

البنية الأولى لتركيبة BARITT

ان المبدأ الاساسي لعمل هذا الدايود مشابة لمبدأ عمل ثنائي IMPATT، ولكن هناك فرقاً اساسياً واحداً وهو في ثنائي BARITT ليس هناك تأثير تيهوري (انهيار) لأن الحاملات الحقونة هي فقط ايونياً وتكون بنفس الطور مع الفولتية المتناوبة.

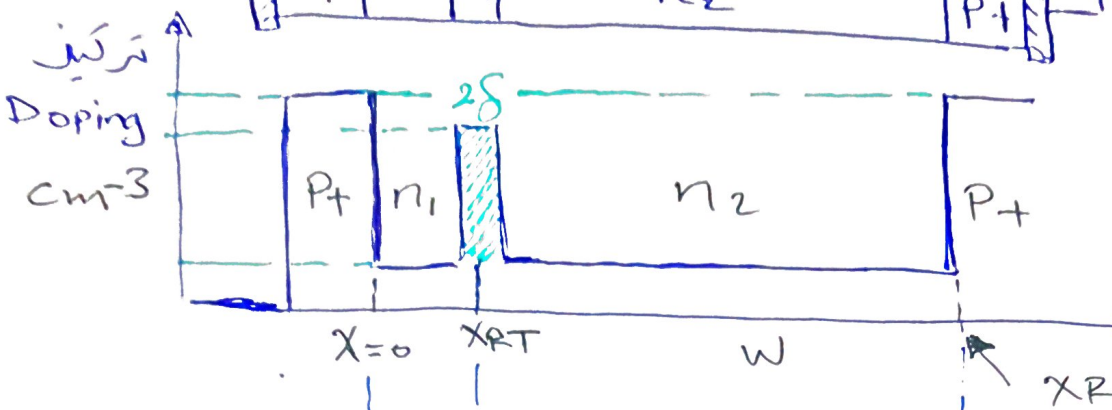


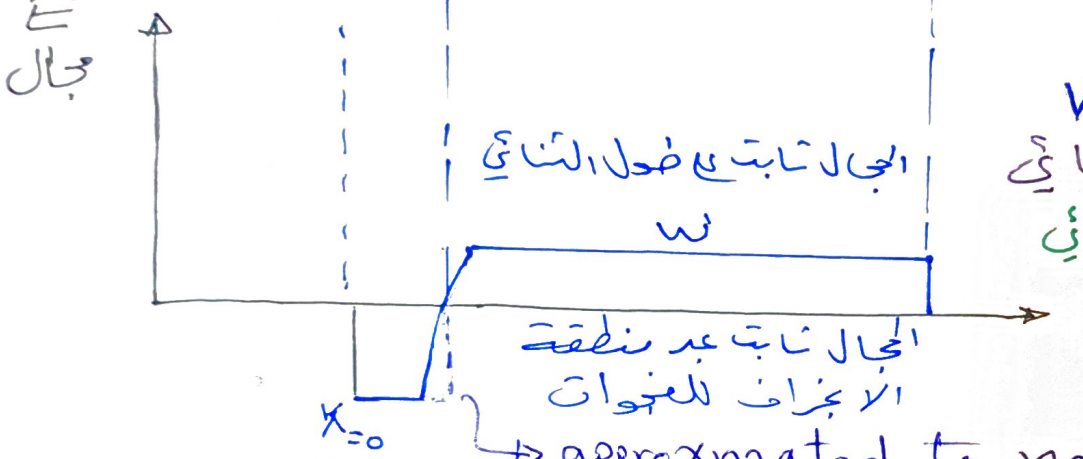
⑤

تركيبة ثنائي

$2\delta = n+$ حيث

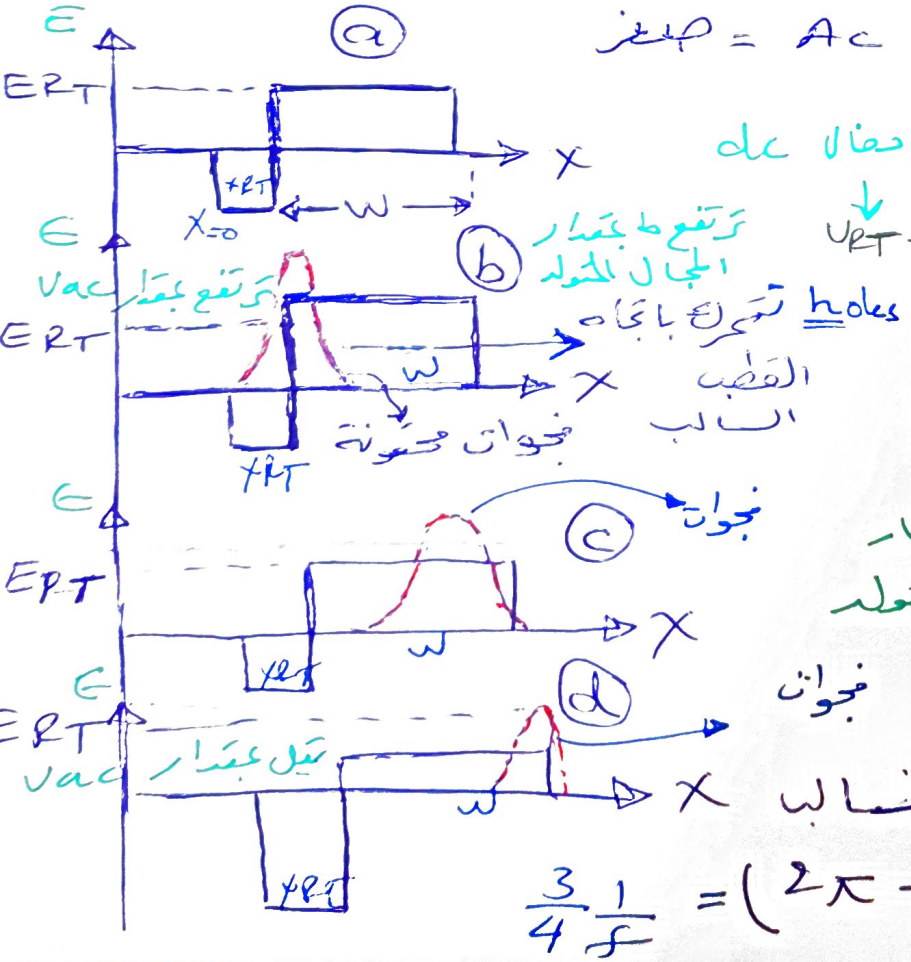
$X=0 \longrightarrow X_{RT} = X_{RT}$



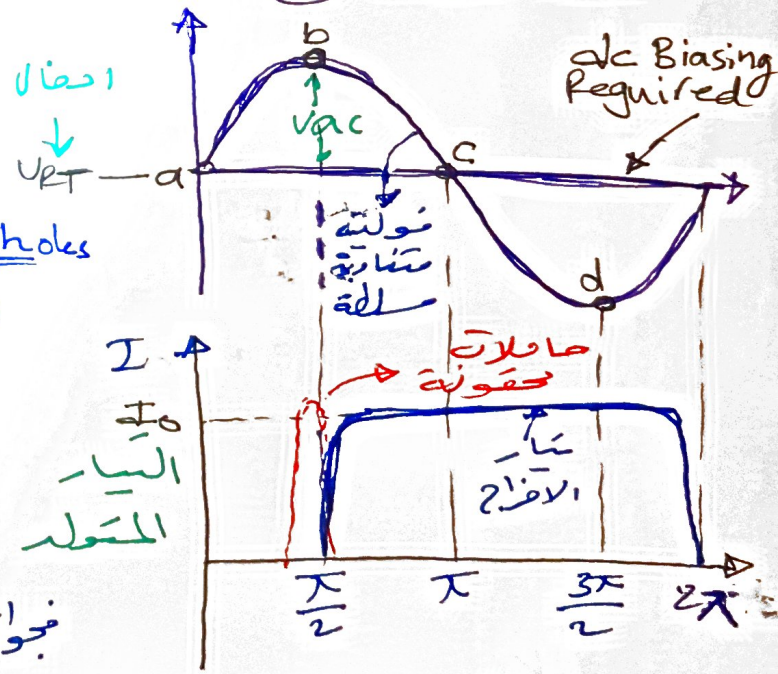


V_{RT} = فولتية عكسية على الثنائي يلوم المجال الكهربائي $\in_{RT}$ نتيجة الفولتية V_{RT}

الخواص الديناميكية لثنائي BARITT (البنية المثلى)



عند نقطة ⓐ ← A_c = صفر



فجوات

الفجوات لكي تصل الى القطب السالب تحتاج زمناً مقدارهُ $\left(2\pi - \frac{\pi}{2}\right)$ = $\frac{3}{4}\frac{1}{f}$

نلاحظ (صفحة ٥) عندما الفولتية تزيد نحو الموجب (نقطة a→b)، فإن النقوب الحرة تزداد بإزدياد الفولتية المتناوبة، ونحصل على الذروة في عدد النقوب الحرة عندما تصل الفولتية الى قيمتها القصوى.

ملاحظة: نلاحظ (صفحة ٥) ايضاً إن الحاملات الحرة تكون بنفس الاتجاه مع الفولتية المتناوبة

ملاحظة: إن الفجوات لكي تصل إلى الطرف السالب تحتاج زمن قدره $\left(\frac{3}{4}\right)$ من زمن الدورة الكامل، والمسافة التي تقطعها الفجوات هي W، وبسرعة مساوية لسرعة الانجراف V_s

$$\frac{\text{مسافة}}{\text{سرعة}} = \frac{W}{V_s} = \frac{3}{4} * \frac{1}{f}$$

$$t_r = \frac{W}{V_s} \qquad \therefore f = \frac{3}{4}\frac{V_s}{W}$$

ولذلك فقط $\frac{3}{4}$ من الدورة هناك تيار الكسب هو ربع دورة

$$\boxed{\text{dc power} = \frac{3}{4} I_o V_{RT}}$$

$$\text{ac power} = \frac{1}{2\pi}\int_0^{2\pi} \frac{V_{RT}}{2} I_o \sin W_t \, d(wt)$$

$$V_m = \frac{V_{RT}}{2} \rightarrow \frac{1}{2} V_{RT}$$

$$\text{ac power} = \frac{1}{2\pi}\left[\int_{\pi/2}^{\pi} \frac{I_o V_{RT}}{2} \sin wt \, dwt + \int_{\pi}^{2\pi} \frac{I_o V_{RT}}{2} \sin wt \, dwt\right]$$

$$= \frac{I_o V_{RT}}{4\pi} \left[\left| -\cos wt \right|_{\pi/2}^{\pi} + \left| -\cos wt \right|_{\pi}^{2\pi} \right] \quad (V)$$

$$\therefore \text{ac Power} = -\frac{I_o V_{RT}}{4\pi}$$

إشارة (-) تدل على القدرة المستهلكة

$$\eta \text{ الكفاءة} = \frac{\text{a.c Power}}{\text{d.c power}} = \frac{V_{RT} I_o / 4\pi}{3 I_o V_{RT}/4}$$

$$\therefore \eta = \frac{1}{3\pi} \text{ at } V_m = \frac{V_{RT}}{2}$$

$$\eta = \frac{1}{3\pi} * 100\,\% = 10.6\,\%$$

if $V_m = \frac{V_{RT}}{2}$

$$\therefore V_{RT} = 2V_m$$

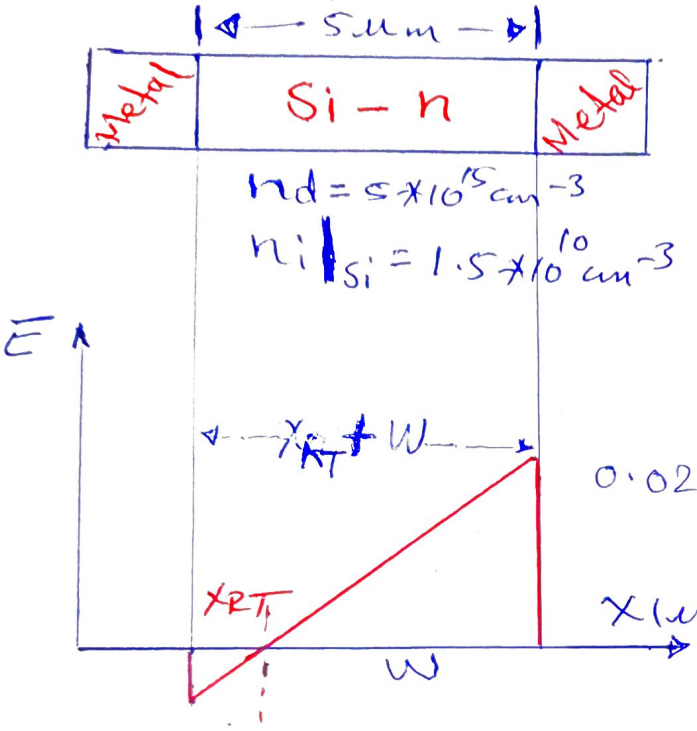
$$\text{ac power} = \frac{-I_o V_{RT}}{4\pi}$$

$$\therefore \text{ac power} = \frac{-I_o 2V_m}{4\pi}$$

$$\therefore \text{ac power} = \frac{-V_m I_o}{2\pi}$$

مثال:- في ثنائي BARITT المبين بالشكل، إذا كان فولتية الانهيار Voltage Reach-Through (V_{RT}) وكذلك أوجد تردد العمل الأعلى وأوجد كفاءة التوليد للثنائي عندما تتراوح $V_m = \frac{3}{7} V_{RT}$.

$X_{RT} + W = 5\mu m$



$V_{bi} = 0.33V$

Solution:

$$X_{RT} = X_n = \sqrt{\frac{2\epsilon_s (V_{bi})}{eN_d}}$$

$0.026V \leftarrow \frac{KT}{e}$

$$V_{bi} = \frac{KT}{e} \ln \frac{N_d}{n_i}$$

$V_{bi} = 0.33V$.

schotcky diode

$$\therefore X_{RT} = \sqrt{\frac{2 * 11.9 * 8.85 \times 10^{-14} * 0.33}{1.6 \times 10^{-19} * 5 * 10^{15}}}$$

$\therefore X_{RT} = 0.3 \mu m$.

$X_{RT} + W = 5 \mu m \longrightarrow \therefore W = 4.7 \mu m$.

$$W = \sqrt{\frac{2\epsilon_{si} (V_{bi} + V_{RT})}{eN_d}}$$

$$4.7\mu m = \sqrt{\frac{2 * 11.9 * 8.85 \times 10^{-14} (0.33 + V_{RT})}{1.6 \times 10^{-19} * 5 * 10^{15}}}$$

0.33

$V_{bi} + V_{RT} = 85 V \longrightarrow V_{RT} = 84.7V$ فولتية الانهيار

$$f = \frac{3 V_s}{4W} = \frac{3 \times 10^7}{4 * 4.7} = 16 GHz.$$ تردد العمل

IF $V_m = \frac{3}{7} V_{RT}$

$$\therefore \eta = \frac{2}{3\pi} \cdot \frac{3}{7} = 9.1\%$$ الكفاءة

Lectures of Electrical Engineering Department

Subject Title: Microelectronics

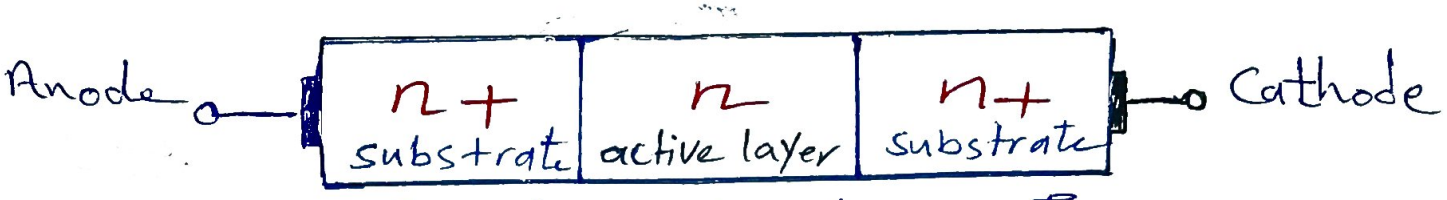
Class: 4th Electronic and Communications

Lecture Contents	**Lecture sequences:**	**First lecture**	**Instructor Name:**
	The major contents: **1- Transferred Electon Device TED or Gunn diode** **2-** **3-** **4-**		
	The detailed contents: **1- Working principle** **2- Characteristics** **3- Applications**		

اسم التدريسي: F.H. Aldabbagh & Firas عنوان البريد الاليكتروني f.h.aldabbagh@uomosul.edu.iq

Transferred-Electron Device

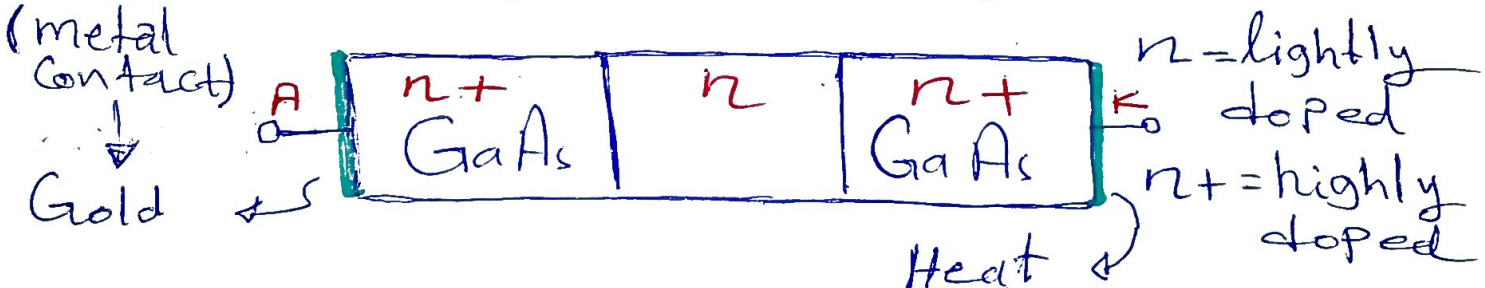
TED or Gunn diode



It is a Semiconductor device formed by only N type material. Electrons are majority carriers in N-type material and these electrons are transferred from one valley to another.

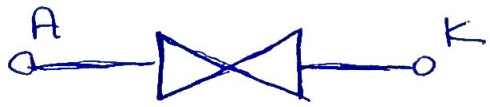
Thus: Gunn diode not a PN junction device

Gunn diode is a 3 layer device



GaAs = gallium Arsenide

Symbole of Gunn diode



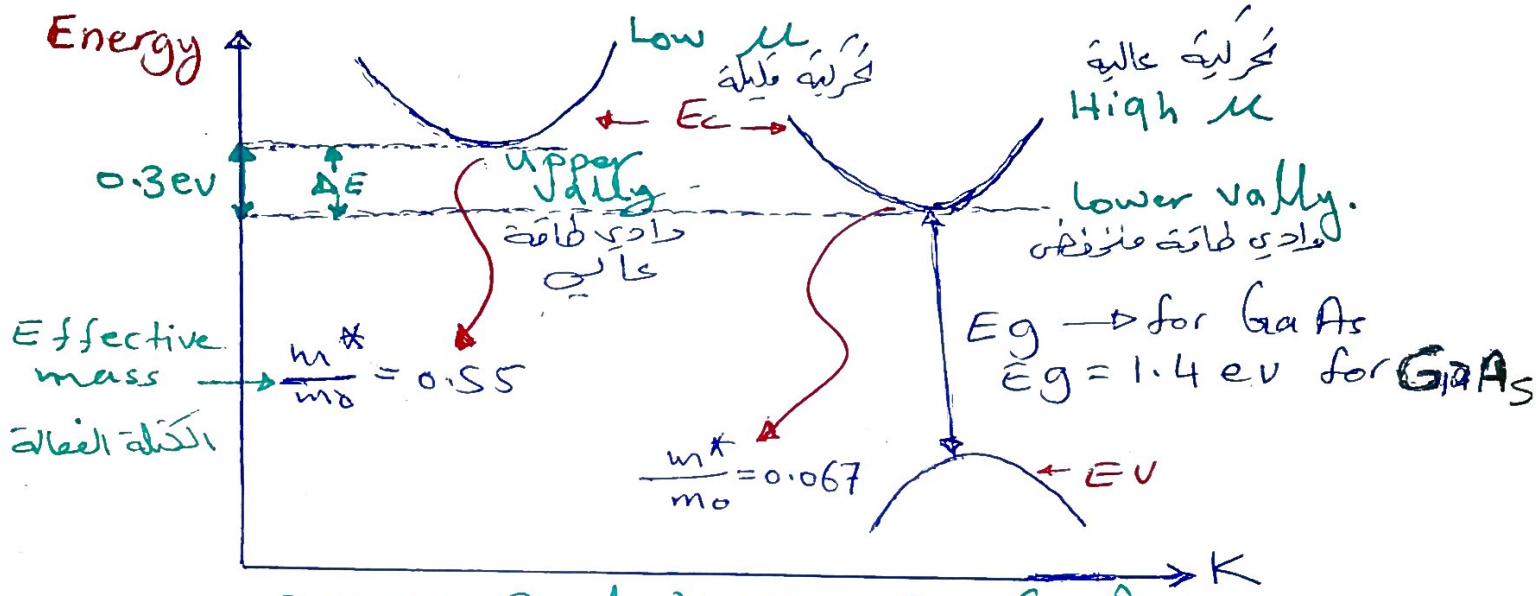
*(-)Ve = negative

Basic Information

* Gunn diode It is working based on "Gunn effect"
* Gunn diode It is discovered by J.B. Gunn 1962
* Gunn diode It is offered (-)Ve resistance.
* Gunn diode It is used High frequency. (microwave application) → oscillators.
* Gunn diode It is made up of GaAs.
* Gunn diode It is not based on PN junction

Gunn effect:

Is The basis of working of Gunn diode So, Gunn effect that occurs when external Voltage is applied to a Gunn diode in material like GaAs.



Energy Band diagram for GaAs

* for GaAs has 2 Conduction Bands.
كما يوجد أيضاً، تمتلك واديين من حزمة التوصيل

Eg = Energy band gap.

m_0 = electron mass in air.

m^* = electron mass in Certain Energy Band.

μ = mobility = التحركية $(cm^2/V.s)$

كتلة الإلكترون في المادة هي أقل من كتلة الإلكترون في الهواء

شرط الحالة $\Delta E\ (0.3eV) < Eg$

أي إذا كانت ΔE أقل من Eg فإن حركة الإلكترونات من وادي الطاقة (المنخفض) إلى وادي الطاقة (العالي)

m_0 = كتلة الإلكترون بالهواء $= 9.1 * 10^{31-} kg$

تعمل هذه البيزطة (device) أو ثنائي Gunn
Gunn diode or TED

تعمل بفعل إنتقال الإلكترونات من وادي الطاقة المنخفض [ذو التحركية العالية] إلى وادي الطاقة العالي [ذو التحركية القليلة]

μ = تحركية

$$\frac{m^*}{m_0} = 0.55 = \frac{\text{كتلة الإلكترون بالوادي العالي}}{\text{كتلة الإلكترون بالهواء}}$$

بالوادي العالي، التحركية (μ) قليلة ← لأن الكتلة كبيرة

$\frac{m^*}{m_0} = 0.55$ $\quad \mu = 180\ cm^2/V.s$

$$\frac{m^*}{m_0} = 0.067 = \frac{\text{كتلة الإلكترون بالوادي المنخفض}}{\text{كتلة الإلكترون بالهواء}}$$

بالوادي المنخفض، التحركية (μ) كبيرة ← لأن الكتلة قليلة

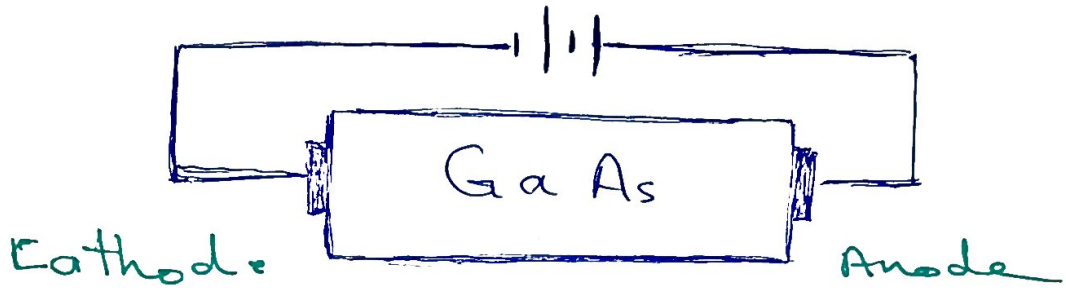
$\frac{m^*}{m_0} = 0.067$ $\quad \mu = 1800\ cm^2/V.s$

Mobility is Reverse Proportional to the mass.

ملاحظة مهمة: كل الإلكترونات التوصيل موجودة في الوادي المنخفض في حالة الاتزان الحراري.

أما الوادي العالي، فبدئياً يحتوي على إلكترونات قليلة عند حالة الاتزان الحراري.

ملاحظة مهمة: الفولتية المطبقة على Gunn diode هي فولتية امامية



① When the Sufficient forward Voltage is applied and the electric field E (المجال الكهربي) exceeds $Ec = 3.2 * 10^3$ V/cm ($E > Ec$)

② The electrons in the lower vally can gain enough energy and scattered in the upper vally. (ينتقل)

③ Electron mass in the upper Vally is much larger than that in the lower Vally.

$$m^*(\text{Upper}) \gg m^*(\text{Lower})$$

④ This means that electron mobility (μ) for the upper Vally is much Smaller than that in the lower Vally

$$\mu(\text{Lower}) \gg \mu(\text{Upper})$$

⑤ As number of electrons Transferred to the upper Vally increases; the Summation of the electron drift Velocity decrease.

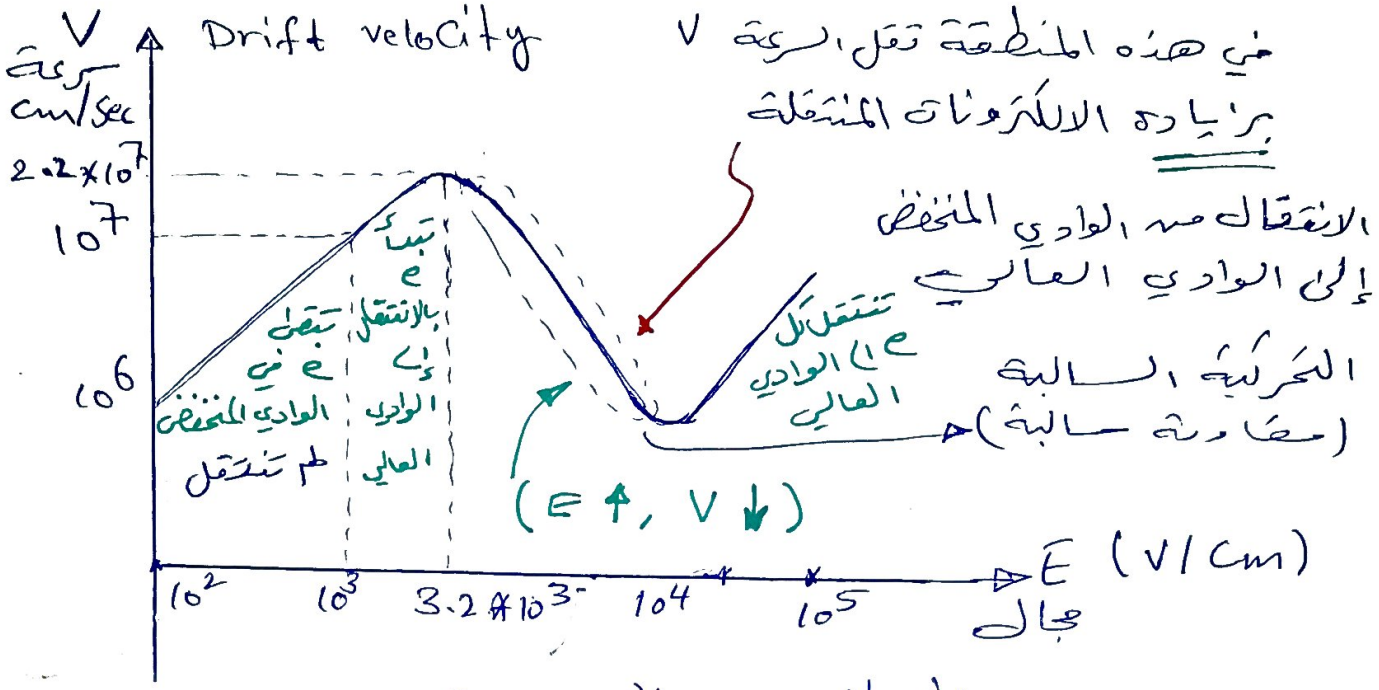
electron drift Velocity = V

$V_{Upper} < V_{Lower}$

عدد الإلكترونات ↑ ⇒ السرعة ↓

$\mu = \frac{dV_s}{dE}$ $\quad V \propto \mu$

Drift Velocity Versus the Electric Field ⑤



في هذه المنطقة تقل سرعة V بزيادة الالكترونات المنتقلة

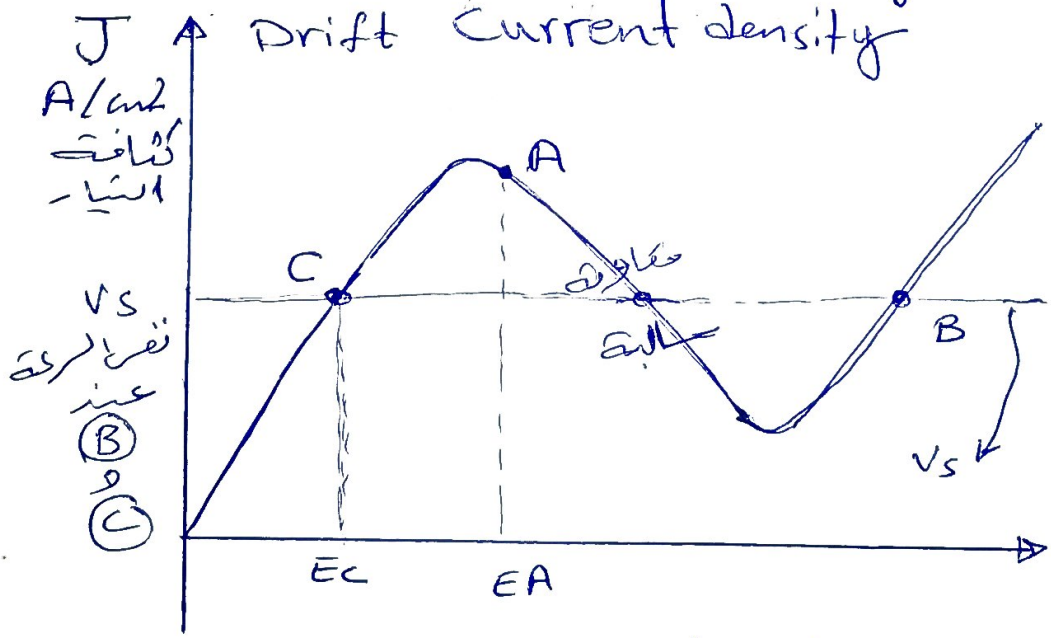
الانتقال من الوادي المنخفض إلى الوادي العالي

الحركية سالبة (مقاومة سالبة)

المجال مع السرعة

Drift Velocity Versus the electric field in GaAs

Drift current density Versus electric field



$$\mu = \frac{\text{سرعة}}{\text{مجال}}$$

$$\mu = \frac{\text{cm/sec}}{\text{V/cm}}$$

$$\mu = \frac{dV}{dE} = \frac{cm^2}{V\cdot sec}$$

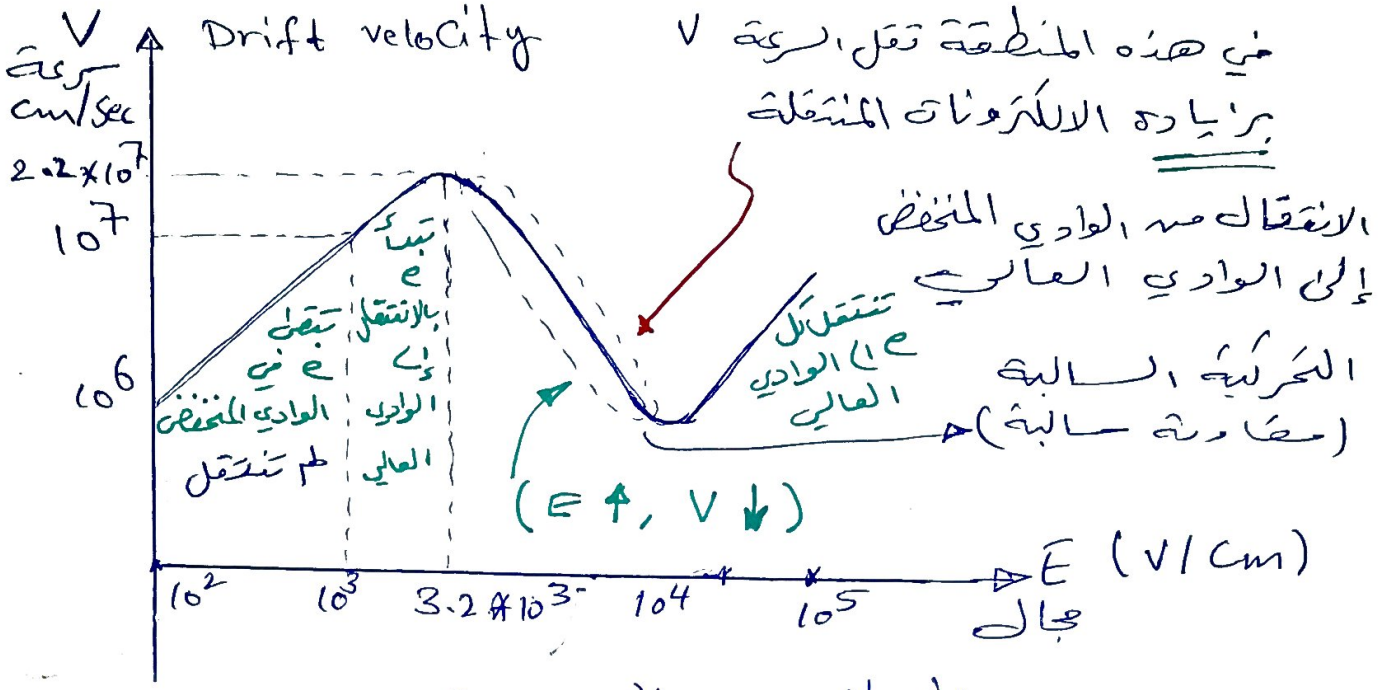
Drift current density Versus electric field in GaAs

كثافة التيار مع المجال

$$\mu = \frac{dV}{dE}$$

V و Vs نفس السرعة

Drift Velocity Versus the Electric Field ⑤



في هذه المنطقة تقل سرعة V بزيادة الالكترونات المنتقلة

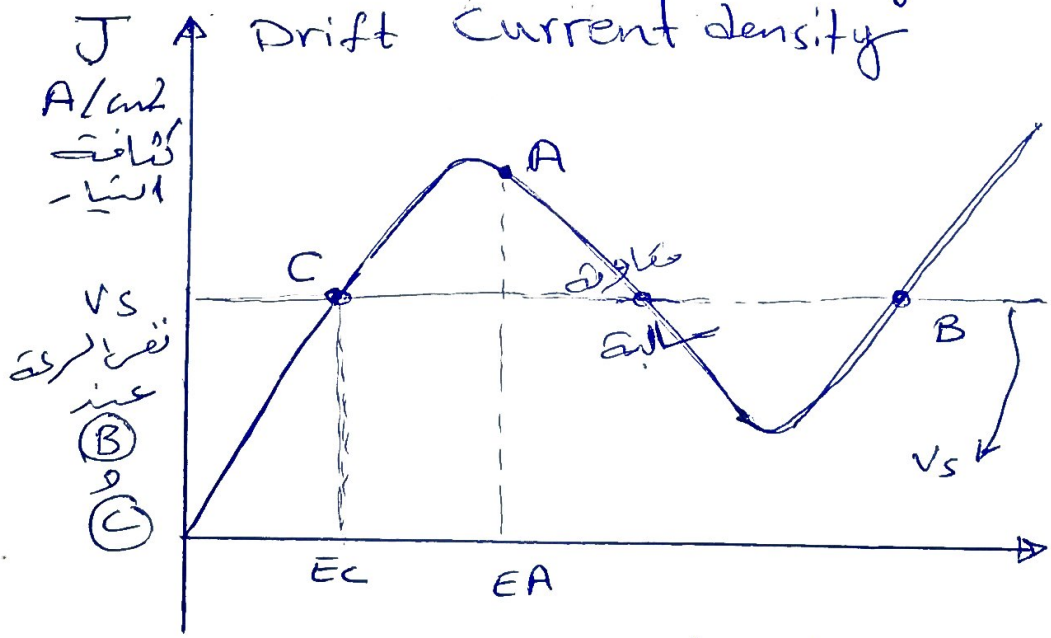
الانتقال من الوادي المنخفض إلى الوادي العالي

الحركية سالبة (مقاومة سالبة)

المجال مع السرعة

Drift Velocity Versus the electric field in GaAs

Drift current density Versus electric field



$$\mu = \frac{\text{سرعة}}{\text{مجال}}$$

$$\mu = \frac{\text{cm/sec}}{\text{V/cm}}$$

$$\mu = \frac{dV}{dE} = \frac{cm^2}{V\cdot sec}$$

Drift current density Versus electric field in GaAs

كثافة التيار مع المجال

$$\mu = \frac{dV}{dE}$$

V و Vs نفس السرعة

Lectures of Electrical Engineering Department

Subject Title: Microelectronics

Class: 4th Electronic and Communications

Lecture Contents	**Lecture sequences:**	**First lecture**	**Instructor Name:**
	The major contents: **1- MOSFET Transistors** **2-** **3-** **4-**		
	The detailed contents: **1- Structure** **2- Principle of Operation** **3- Type of MOSFETs** **4-**		

اسم التدريسي: F.H. Aldabbagh & Firas عنوان البريد الاليكتروني f.h.aldabbagh@uomosul.edu.iq

3.1 MOS FIELD-EFFECT TRANSISTOR

Objective: • Understand the operation and characteristics of the various types of metal-oxide semiconductor field-effect transistors (MOSFETs).

The **metal-oxide-semiconductor field-effect transistor (MOSFET)** became a practical reality in the 1970s. The MOSFET, compared to BJTs, can be made very small (that is, it occupies a very small area on an IC chip). Since digital circuits can be designed using only MOSFETs, with essentially no resistors or diodes required, high-density VLSI circuits, including microprocessors and memories, can be fabricated. The MOSFET has made possible the handheld calculator, the powerful personal computer, and the laptop computer. MOSFETs can also be used in analog circuits, as we will see in the next chapter.

In the MOSFET, the current is controlled by an electric field applied perpendicular to both the semiconductor surface and to the direction of current. The phenomenon used to modulate the conductance of a semiconductor, or control the current in a semiconductor, by applying an electric field perpendicular to the surface is called the **field effect.** The basic transistor principle is that the voltage between two terminals controls the current through the third terminal.

In the following two sections, we will discuss the various types of MOSFETs, develop the i–v characteristics, and then consider the dc biasing of various MOSFET circuit configurations. After studying these sections, you should be familiar and comfortable with the MOSFET and MOSFET circuits.

3.1.1 Two-Terminal MOS Structure

The heart of the MOSFET is the metal-oxide-semiconductor capacitor shown in Figure 3.1. The metal may be aluminum or some other type of metal. In most cases, the metal is replaced by a high-conductivity polycrystalline silicon layer deposited on the oxide. However, the term metal is usually still used in referring to MOSFETs. In the figure, the parameter t_{ox} is the thickness of the oxide and ϵ_{ox} is the oxide permittivity.

The physics of the MOS structure can be explained with the aid of a simple parallel-plate capacitor.[1] Figure 3.2(a) shows a parallel-plate capacitor with the top plate at a negative voltage with respect to the bottom plate. An insulator material separates the two plates. With this bias, a negative charge exists on the top plate, a positive charge exists on the bottom plate, and an electric field is induced between the two plates, as shown.

A MOS capacitor with a p-type semiconductor substrate is shown in Figure 3.2(b). The top metal terminal, also called the **gate,** is at a negative voltage with respect to the semiconductor substrate. From the example of the parallel-plate capacitor, we can see that a negative charge will exist on the top metal plate and an electric field will be induced in the direction shown in the figure. If the electric field penetrates the

[1]The capacitance of a parallel plate capacitor, neglecting fringing fields, is $C = \epsilon A/d$, where A is the area of one plate, d is the distance between plates, and ϵ is the permittivity of the medium between the plates.

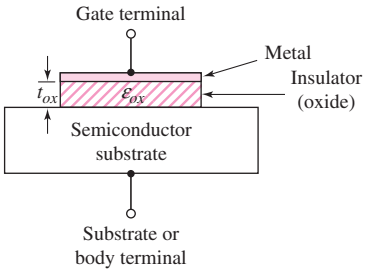


Figure 3.1 The basic MOS capacitor structure

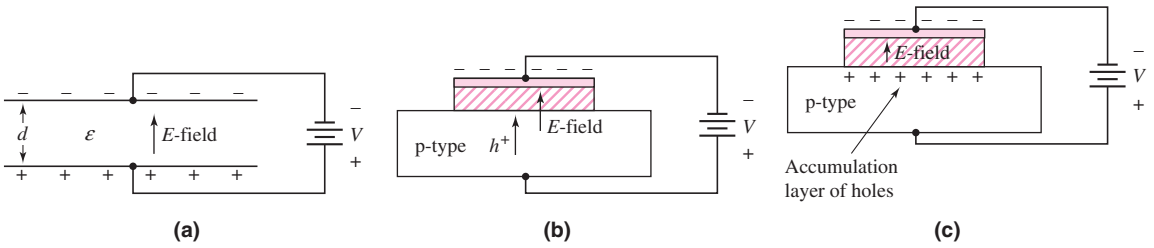


Figure 3.2 (a) A parallel-plate capacitor, showing the electric field and conductor charges, (b) a corresponding MOS capacitor with a negative gate bias, showing the electric field and charge flow, and (c) the MOS capacitor with an accumulation layer of holes

semiconductor, the holes in the p-type semiconductor will experience a force toward the oxide-semiconductor interface. The equilibrium distribution of charge in the MOS capacitor with this particular applied voltage is shown in Figure 3.2(c). An accumulation layer of positively charged holes at the oxide-semiconductor interface corresponds to the positive charge on the bottom "plate" of the MOS capacitor.

Figure 3.3(a) shows the same MOS capacitor, but with the polarity of the applied voltage reversed. A positive charge now exists on the top metal plate and the induced electric field is in the opposite direction, as shown. In this case, if the electric field penetrates the semiconductor, holes in the p-type material will experience a force away from the oxide-semiconductor interface. As the holes are pushed away from the interface, a negative space-charge region is created, because of the fixed acceptor impurity atoms. The negative charge in the induced depletion region corresponds to the negative charge on the bottom "plate" of the MOS capacitor. Figure 3.3(b) shows the equilibrium distribution of charge in the MOS capacitor with this applied voltage.

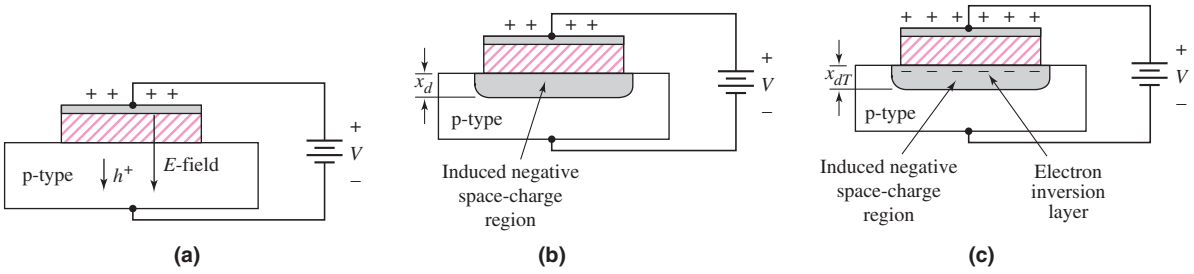


Figure 3.3 The MOS capacitor with p-type substrate: (a) effect of positive gate bias, showing the electric field and charge flow, (b) the MOS capacitor with an induced space-charge region due to a moderate positive gate bias, and (c) the MOS capacitor with an induced space-charge region and electron inversion layer due to a larger positive gate bias

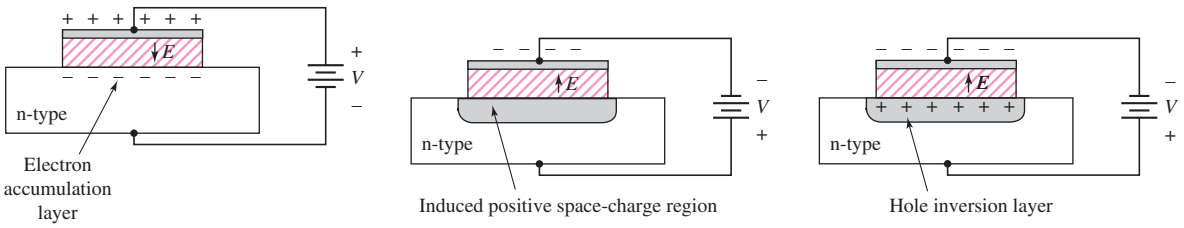


Figure 3.4 The MOS capacitor with n-type substrate: (a) effect of a positive gate bias and the formation of an electron accumulation layer, (b) the MOS capacitor with an induced space-charge region due to a moderate negative gate bias, and (c) the MOS capacitor with an induced space-charge region and hole inversion layer due to a larger negative gate bias

When a larger positive voltage is applied to the gate, the magnitude of the induced electric field increases. Minority carrier electrons are attracted to the oxide-semiconductor interface, as shown in Figure 3.3(c). This region of minority carrier electrons is called an **electron inversion layer.** The magnitude of the charge in the inversion layer is a function of the applied gate voltage.

The same basic charge distributions can be obtained in a MOS capacitor with an n-type semiconductor substrate. Figure 3.4(a) shows this MOS capacitor structure, with a positive voltage applied to the top gate terminal. A positive charge is created on the top gate and an electric field is induced in the direction shown. In this situation, an accumulation layer of electrons is induced in the n-type semiconductor.

Figure 3.4(b) shows the case when a negative voltage is applied to the gate terminal. A positive space-charge region is induced in the n-type substrate by the induced electric field. When a larger negative voltage is applied, a region of positive charge is created at the oxide-semiconductor interface, as shown in Figure 3.4(c). This region of minority carrier holes is called a **hole inversion layer.** The magnitude of the positive charge in the inversion layer is a function of the applied gate voltage.

The term **enhancement mode** means that a voltage must be applied to the gate to create an inversion layer. For the MOS capacitor with a p-type substrate, a positive gate voltage must be applied to create the electron inversion layer; for the MOS capacitor with an n-type substrate, a negative gate voltage must be applied to create the hole inversion layer.

3.1.2 n-Channel Enhancement-Mode MOSFET

We will now apply the concepts of an inversion layer charge in a MOS capacitor to create a transistor.

Transistor Structure

Figure 3.5(a) shows a simplified cross section of a MOS field-effect transistor. The gate, oxide, and p-type substrate regions are the same as those of a MOS capacitor. In addition, we now have two n-regions, called the **source terminal** and **drain terminal.** The current in a MOSFET is the result of the flow of charge in the inversion layer, also called the **channel region,** adjacent to the oxide–semiconductor interface.

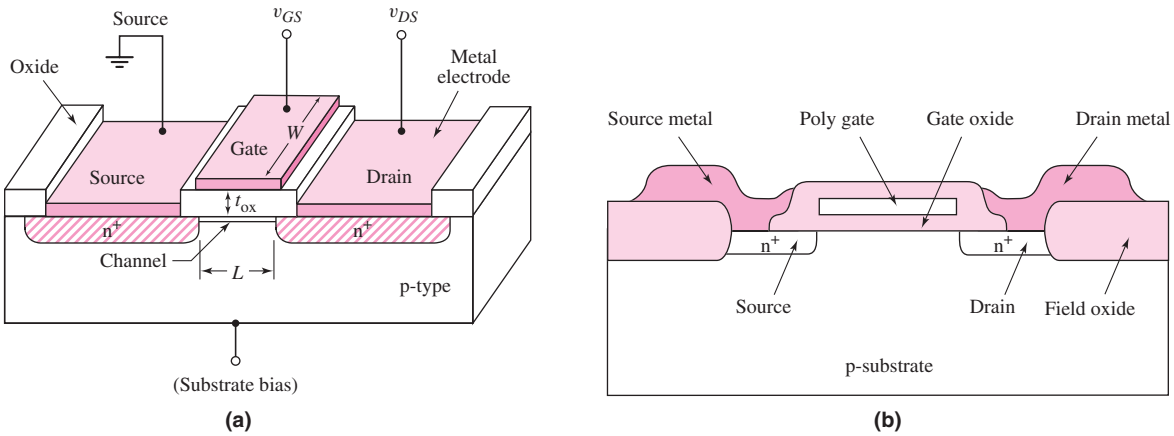


Figure 3.5 (a) Schematic diagram of an n-channel enhancement-mode MOSFET and (b) an n-channel MOSFET, showing the field oxide and polysilicon gate

The channel length L and channel width W are defined on the figure. The channel length of a typical integrated circuit MOSFET is less than 1 μm (10^{-6} m), which means that MOSFETs are small devices. The oxide thickness t_{ox} is typically on the order of 400 angstroms, or less.

The diagram in Figure 3.5(a) is a simplified sketch of the basic structure of the transistor. Figure 3.5(b) shows a more detailed cross section of a MOSFET fabricated into an integrated circuit configuration. A thick oxide, called the **field oxide,** is deposited outside the area in which the metal interconnect lines are formed. The gate material is usually heavily doped polysilicon. Even though the actual structure of a MOSFET may be fairly complex, the simplified diagram may be used to develop the basic transistor characteristics.

Basic Transistor Operation

With zero bias applied to the gate, the source and drain terminals are separated by the p-region, as shown in Figure 3.6(a). This is equivalent to two back-to-back diodes, as shown in Figure 3.6(b). The current in this case is essentially zero. If a large enough positive gate voltage is applied, an electron inversion layer is created at the oxide–semiconductor interface and this layer "connects" the n-source to the n-drain,

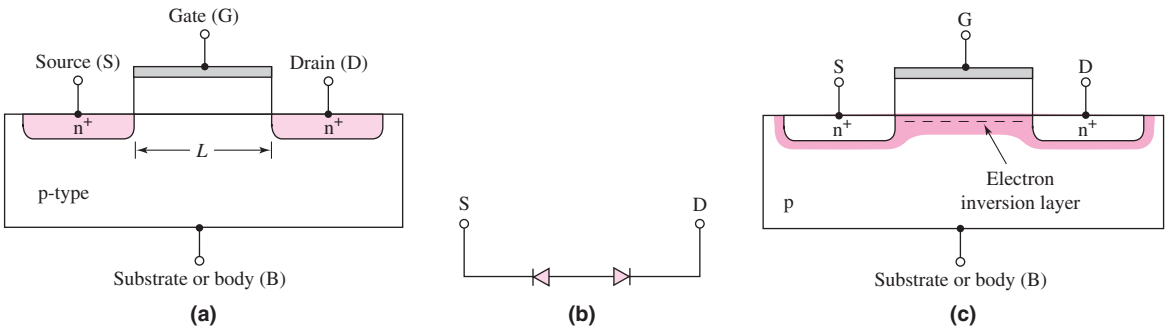


Figure 3.6 (a) Cross section of the n-channel MOSFET prior to the formation of an electron inversion layer, (b) equivalent back-to-back diodes between source and drain when the transistor is in cutoff, and (c) cross section after the formation of an electron inversion layer

as shown in Figure 3.6(c). A current can then be generated between the source and drain terminals. Since a voltage must be applied to the gate to create the inversion charge, this transistor is called an **enhancement-mode MOSFET.** Also, since the carriers in the inversion layer are electrons, this device is also called an **n-channel MOSFET (NMOS).**

The source terminal supplies carriers that flow through the channel, and the drain terminal allows the carriers to drain from the channel. For the n-channel MOSFET, electrons flow from the source to the drain with an applied drain-to-source voltage, which means the conventional current enters the drain and leaves the source. The magnitude of the current is a function of the amount of charge in the inversion layer, which in turn is a function of the applied gate voltage. Since the gate terminal is separated from the channel by an oxide or insulator, there is no gate current. Similarly, since the channel and substrate are separated by a space-charge region, there is essentially no current through the substrate.

3.1.3 Ideal MOSFET Current–Voltage Characteristics—NMOS Device

The **threshold voltage** of the n-channel MOSFET, denoted as V_{TN}, is defined[2] as the applied gate voltage needed to create an inversion charge in which the density is equal to the concentration of majority carriers in the semiconductor substrate. In simple terms, we can think of the threshold voltage as the gate voltage required to "turn on" the transistor.

For the n-channel enhancement-mode MOSFET, the threshold voltage is positive because a positive gate voltage is required to create the inversion charge. If the gate voltage is less than the threshold voltage, the current in the device is essentially zero. If the gate voltage is greater than the threshold voltage, a drain-to-source current is generated as the drain-to-source voltage is applied. The gate and drain voltages are measured with respect to the source.

Figure 3.7(a) shows an n-channel enhancement-mode MOSFET with the source and substrate terminals connected to ground. The gate-to-source voltage is less than the threshold voltage, and there is a small drain-to-source voltage. With this bias configuration, there is no electron inversion layer, the drain-to-substrate pn junction is reverse biased, and the drain current is zero (neglecting pn junction leakage currents).

Figure 3.7(b) shows the same MOSFET with an applied gate voltage greater than the threshold voltage. In this situation, an electron inversion layer is created and, when a small drain voltage is applied, electrons in the inversion layer flow from the source to the positive drain terminal. The conventional current enters the drain terminal and leaves the source terminal. Note that a positive drain voltage creates a reverse-biased drain-to-substrate pn junction, so current flows through the channel region and not through a pn junction.

The i_D versus v_{DS} characteristics[3] for small values of v_{DS} are shown in Figure 3.8. When $v_{GS} < V_{TN}$, the drain current is zero. When v_{GS} is greater than V_{TN},

---

[2]The usual notation for threshold voltage is V_T. However, since we have defined the thermal voltage as $V_T = kT/q$, we will use V_{TN} for the threshold voltage of the n-channel device.

[3]The voltage notation v_{DS} and v_{GS}, with the dual subscript, denotes the voltage between the drain (D) and source (S) and between the gate (G) and source (S), respectively. Implicit in the notation is that the first subscript is positive with respect to the second subscript.

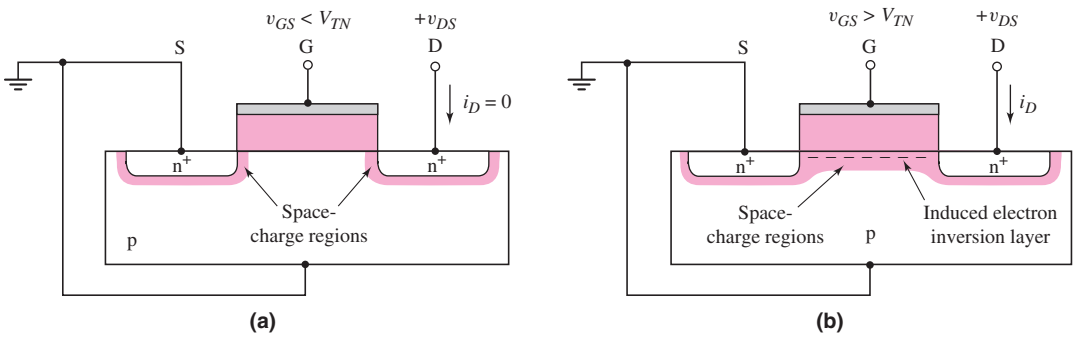


Figure 3.7 The n-channel enhancement-mode MOSFET (a) with an applied gate voltage $v_{GS} < V_{TN}$, and (b) with an applied gate voltage $v_{GS} > V_{TN}$

the channel inversion charge is formed and the drain current increases with v_{DS}. Then, with a larger gate voltage, a larger inversion charge density is created, and the drain current is greater for a given value of v_{DS}.

Figure 3.9(a) shows the basic MOS structure for $v_{GS} > V_{TN}$ and a small applied v_{DS}. In the figure, the thickness of the inversion channel layer qualitatively indicates the relative charge density, which for this case is essentially constant along the entire channel length. The corresponding i_D versus v_{DS} curve is also shown in the figure.

Figure 3.9(b) shows the situation when v_{DS} increases. As the drain voltage increases, the voltage drop across the oxide near the drain terminal decreases, which means that the induced inversion charge density near the drain also decreases. The incremental conductance of the channel at the drain then decreases, which causes the slope of the i_D versus v_{DS} curve to decrease. This effect is shown in the i_D versus v_{DS} curve in the figure.

As v_{DS} increases to the point where the potential difference, $v_{GS} - v_{DS}$, across the oxide at the drain terminal is equal to V_{TN}, the induced inversion charge density at the drain terminal is zero. This effect is shown schematically in Figure 3.9(c). For this condition, the incremental channel conductance at the drain is zero, which means that the slope of the i_D versus v_{DS} curve is zero. We can write

$$v_{GS} - v_{DS}(\text{sat}) = V_{TN} \tag{3.1(a)}$$

or

$$\boxed{v_{DS}(\text{sat}) = v_{GS} - V_{TN}} \tag{3.1(b)}$$

where $v_{DS}(\text{sat})$ is the drain-to-source voltage that produces zero inversion charge density at the drain terminal.

When v_{DS} becomes larger than $v_{DS}(\text{sat})$, the point in the channel at which the inversion charge is just zero moves toward the source terminal. In this case, electrons enter the channel at the source, travel through the channel toward the drain, and then, at the point where the charge goes to zero, are injected into the space-charge region, where they are swept by the E-field to the drain contact. In the ideal MOSFET, the drain current is constant for $v_{DS} > v_{DS}(\text{sat})$. This region of the i_D versus v_{DS} characteristic is referred to as the **saturation region,** which is shown in Figure 3.9(d).

As the applied gate-to-source voltage changes, the i_D versus v_{DS} curve changes. In Figure 3.8, we saw that the initial slope of i_D versus v_{DS} increases as v_{GS} increases. Also, Equation (3.1(b)) shows that $v_{DS}(\text{sat})$ is a function of v_{GS}. Therefore, we can

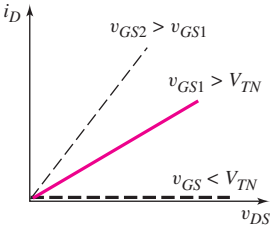


Figure 3.8 Plot of i_D versus v_{DS} characteristic for small values of v_{DS} at three v_{GS} voltages

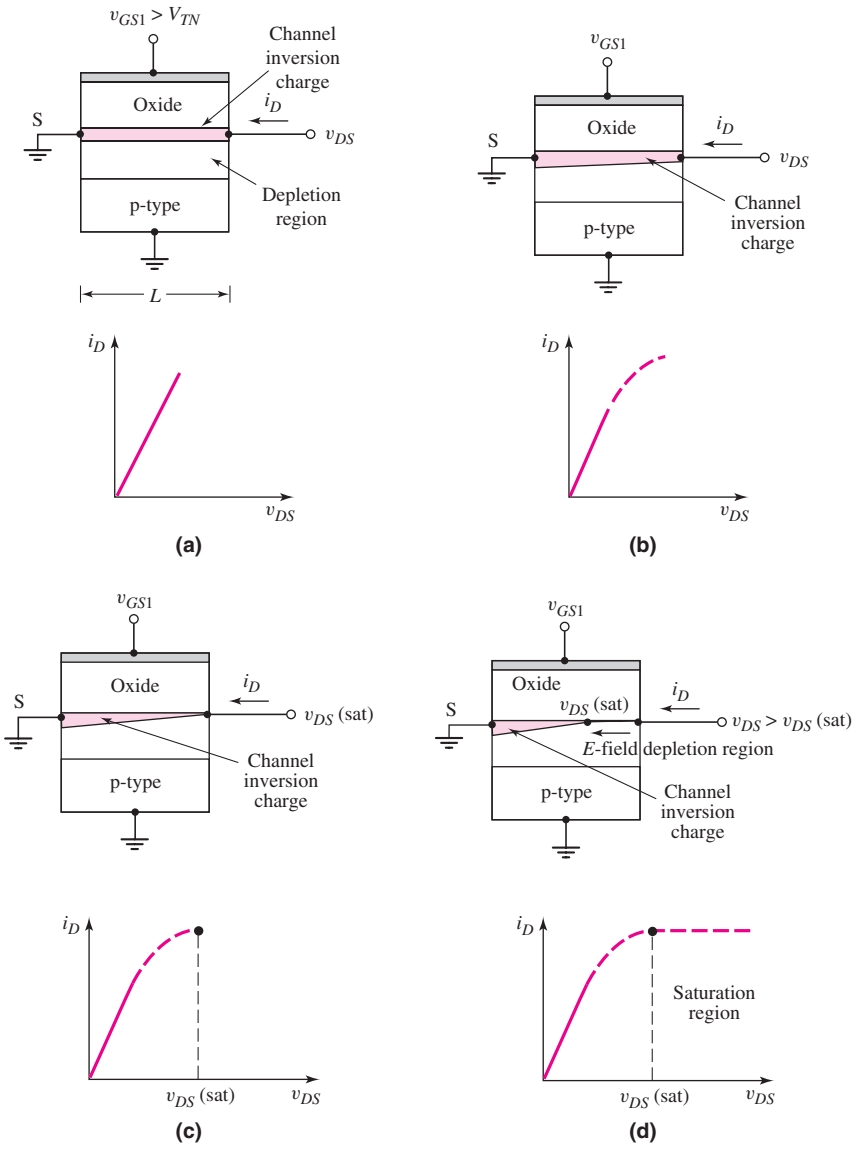


Figure 3.9 Cross section and i_D versus v_{DS} curve for an n-channel enhancement-mode MOSFET when $v_{GS} > V_{TN}$ for (a) a small v_{DS} value, (b) a larger v_{DS} value but for $v_{DS} < v_{DS}(\text{sat})$, (c) $v_{DS} = v_{DS}(\text{sat})$, and (d) $v_{DS} > v_{DS}(\text{sat})$

generate the family of curves for this n-channel enhancement mode MOSFET as shown in Figure 3.10.

Although the derivation of the current–voltage characteristics of the MOSFET is beyond the scope of this text, we can define the relationships. The region for which $v_{DS} < v_{DS}(\text{sat})$ is known as the **nonsaturation** or **triode region.** The ideal current–voltage characteristics in this region are described by the equation

$$i_D = K_n\left[2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2\right] \qquad \textbf{(3.2(a))}$$

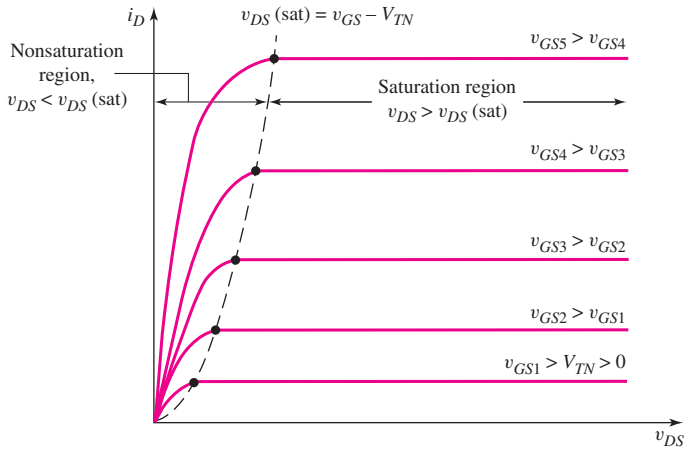


Figure 3.10 Family of i_D versus v_{DS} curves for an n-channel enhancement-mode MOSFET. Note that the v_{DS}(sat) voltage is a single point on each of the curves. This point denotes the transition between the nonsaturation region and the saturation region

In the saturation region, the ideal current–voltage characteristics for $v_{GS} > V_{TN}$ are described by the equation

$$i_D = K_n(v_{GS} - V_{TN})^2 \qquad \textbf{(3.2(b))}$$

$V_{is} \geq v_{GS} - V_{TN}$

In the saturation region, since the ideal drain current is independent of the drain-to-source voltage, the incremental or small-signal resistance is infinite. We see that

$$r_0 = \Delta v_{DS}/\Delta i_D|_{v_{GS}=\text{const.}} = \infty$$

The parameter K_n is sometimes called the transconduction parameter for the n-channel device. However, this term is not to be confused with the small-signal transconductance parameter introduced in the next chapter. For simplicity, we will refer to this parameter as the **conduction parameter,** which for an n-channel device is given by

$$K_n = \frac{W\mu_n C_{\text{ox}}}{2L} \qquad \textbf{(3.3(a))}$$

where C_{ox} is the oxide capacitance per unit area. The capacitance is given by

$$C_{\text{ox}} = \epsilon_{\text{ox}}/t_{\text{ox}}$$

where t_{ox} is the oxide thickness and ϵ_{ox} is the oxide permittivity. For silicon devices, $\epsilon_{\text{ox}} = (3.9)(8.85 \times 10^{-14})$ F/cm. The parameter μ_n is the mobility of the electrons in the inversion layer. The channel width W and channel length L were shown in Figure 3.5(a).

As Equation (3.3(a)) indicates, the conduction parameter is a function of both electrical and geometric parameters. The oxide capacitance and carrier mobility are essentially constants for a given fabrication technology. However, the geometry, or width-to-length ratio W/L, is a variable in the design of MOSFETs that is used to produce specific current–voltage characteristics in MOSFET circuits.

We can rewrite the conduction parameter in the form

$$K_n = \frac{k_n'}{2} \cdot \frac{W}{L} \qquad \textbf{(3.3(b))}$$

where $k_n' = \mu_n C_{ox}$ and is called the **process conduction parameter.** Normally, k_n' is considered to be a constant for a given fabrication technology, so Equation (3.3(b)) indicates that the width-to-length ratio W/L is the transistor design variable.

EXAMPLE 3.1

Objective: Calculate the current in an n-channel MOSFET.

Consider an n-channel enhancement-mode MOSFET with the following parameters: $V_{TN} = 0.4$ V, $W = 20\ \mu$m, $L = 0.8\ \mu$m, $\mu_n = 650$ cm^2/V–s, $t_{ox} = 200$ Å, and $\epsilon_{ox} = (3.9)(8.85 \times 10^{-14})$ F/cm. Determine the current when the transistor is biased in the saturation region for (a) $v_{GS} = 0.8$ V and (b) $v_{GS} = 1.6$ V.

Solution: The conduction parameter is determined by Equation (3.3(a)). First, consider the units involved in this equation, as follows:

$$K_n = \frac{W(\text{cm}) \cdot \mu_n \left(\frac{\text{cm}^2}{\text{V–s}}\right) \epsilon_{ox} \left(\frac{\text{F}}{\text{cm}}\right)}{2L(\text{cm}) \cdot t_{ox}(\text{cm})} = \frac{\text{F}}{\text{V–s}} = \frac{(\text{C/V})}{\text{V–s}} = \frac{\text{A}}{\text{V}^2}$$

The value of the conduction parameter is therefore

$$K_n = \frac{W \mu_n \epsilon_{ox}}{2Lt_{ox}} = \frac{(20 \times 10^{-4})(650)(3.9)(8.85 \times 10^{-14})}{2(0.8 \times 10^{-4})(200 \times 10^{-8})}$$

or

$$K_n = 1.40\ \text{mA/V}^2$$

From Equation (3.2(b)), we find:

(a) For $v_{GS} = 0.8$ V,

$$i_D = K_n(v_{GS} - V_{TN})^2 = (1.40)(0.8 - 0.4)^2 = 0.224\ \text{mA}$$

(b) For $v_{GS} = 1.6$ V,

$$i_D = (1.40)(1.6 - 0.4)^2 = 2.02\ \text{mA}$$

Comment: The current capability of a transistor can be increased by increasing the conduction parameter. For a given fabrication technology, K_n is adjusted by varying the transistor width W.

EXERCISE PROBLEM

Ex 3.1: An NMOS transistor with $V_{TN} = 1$ V has a drain current $i_D = 0.8$ mA when $v_{GS} = 3$ V and $v_{DS} = 4.5$ V. Calculate the drain current when: (a) $v_{GS} = 2$ V, $v_{DS} = 4.5$ V; and (b) $v_{GS} = 3$ V, $v_{DS} = 1$ V. (Ans. (a) 0.2 mA (b) 0.6 mA)

2

3.1.4 p-Channel Enhancement-Mode MOSFET

The complementary device of the n-channel enhancement-mode MOSFET is the p-channel enhancement-mode MOSFET.

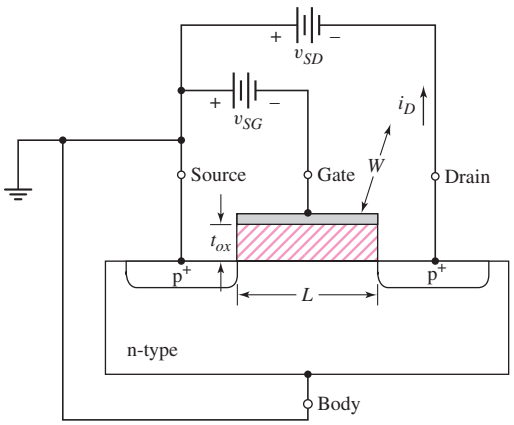


Figure 3.11 Cross section of p-channel enhancement-mode MOSFET. The device is cut off for $v_{SG} = 0$. The dimension W extends into the plane of the page.

Transistor Structure

Figure 3.11 shows a simplified cross section of the p-channel enhancement-mode transistor. The substrate is now n-type and the source and drain areas are p-type. The channel length, channel width, and oxide thickness parameter definitions are the same as those for the NMOS device shown in Figure 3.5(a).

Basic Transistor Operation

The operation of the p-channel device is the same as that of the n-channel device, except the hole is the charge carrier rather than the electron. A negative gate bias is required to induce an inversion layer of holes in the channel region directly under the oxide. The threshold voltage for the p-channel device is denoted as V_{TP}.[4] Since the threshold voltage is defined as the gate voltage required to induce the inversion layer, then $V_{TP} < 0$ for the p-channel enhancement-mode device.

Once the inversion layer has been created, the p-type source region is the source of the charge carrier so that holes flow from the source to the drain. A negative drain voltage is therefore required to induce an electric field in the channel forcing the holes to move from the source to the drain. The conventional current direction, then, for the PMOS transistor is into the source and out of the drain. The conventional current direction and voltage polarity for the PMOS device are reversed compared to the NMOS device.

Note in Figure 3.11 the reversal of the voltage subscripts. For $v_{SG} > 0$, the gate voltage is negative with respect to that at the source. Similarly, for $v_{SD} > 0$, the drain voltage is negative with respect to that at the source.

3.1.5 Ideal MOSFET Current–Voltage Characteristics—PMOS Device

The ideal current–voltage characteristics of the p-channel enhancement-mode device are essentially the same as those shown in Figure 3.10, noting that the drain current

[4]Using a different threshold voltage parameter for a PMOS device compared to the NMOS device is for clarity only.

is out of the drain and v_{DS} is replaced by v_{SD}. The saturation point is given by $v_{SD}(\text{sat}) = v_{SG} + V_{TP}$. For the p-channel device biased in the nonsaturation region, the current is given by

$$i_D = K_p\left[2(v_{SG} + V_{TP})v_{SD} - v_{SD}^2\right] \tag{3.4(a)}$$

In the saturation region, the current is given by

$$i_D = K_p(v_{SG} + V_{TP})^2 \tag{3.4(b)}$$

and the drain current exits the drain terminal. The parameter K_p is the conduction parameter for the p-channel device and is given by

$$K_p = \frac{W\mu_p C_{\text{ox}}}{2L} \tag{3.5(a)}$$

where W, L, and C_{ox} are the channel width, length, and oxide capacitance per unit area, as previously defined. The parameter μ_p is the mobility of holes in the hole inversion layer. In general, the hole inversion layer mobility is less than the electron inversion layer mobility.

We can also rewrite Equation (3.5(a)) in the form

$$K_p = \frac{k_p'}{2} \cdot \frac{W}{L} \tag{3.5(b)}$$

where $k_p' = \mu_p C_{\text{ox}}$.

For a p-channel MOSFET biased in the saturation region, we have

$$v_{SD} > v_{SD}(\text{sat}) = v_{SG} + V_{TP} \tag{3.6}$$

EXAMPLE 3.2

Objective: Determine the source-to-drain voltage required to bias a p-channel enhancement-mode MOSFET in the saturation region.

Consider an enhancement-mode p-channel MOSFET for which $K_p = 0.2\,\text{mA/V}^2$, $V_{TP} = -0.50$ V, and $i_D = 0.50$ mA.

Solution: In the saturation region, the drain current is given by

$$i_D = K_p(v_{SG} + V_{TP})^2$$

or

$$0.50 = 0.2(v_{SG} - 0.50)^2$$

which yields

$$v_{SG} = 2.08 \text{ V}$$

To bias this p-channel MOSFET in the saturation region, the following must apply:

$$v_{SD} > v_{SD}(\text{sat}) = v_{SG} + V_{TP} = 2.08 - 0.5 = 1.58 \text{ V}$$

Comment: Biasing a transistor in either the saturation or the nonsaturation region depends on both the gate-to-source voltage and the drain-to-source voltage.

EXERCISE PROBLEM

Ex 3.2: A PMOS device with $V_{TP} = -1.2$ V has a drain current $i_D = 0.5$ mA when $v_{SG} = 3$ V and $v_{SD} = 5$ V. Calculate the drain current when (a) $v_{SG} = 2$ V, $v_{SD} = 3$ V; and (b) $v_{SG} = 5$ V, $v_{SD} = 2$ V. (Ans. (a) 0.0986 mA, (b) 1.72 mA)

3.1.6 Circuit Symbols and Conventions

The conventional circuit symbol for the n-channel enhancement-mode MOSFET is shown in Figure 3.12(a). The vertical solid line denotes the gate electrode, the vertical broken line denotes the channel (the broken line indicates the device is enhancement mode), and the separation between the gate line and channel line denotes the oxide that insulates the gate from the channel. The polarity of the pn junction between the substrate and the channel is indicated by the arrowhead on the body or substrate terminal. The direction of the arrowhead indicates the type of transistor, which in this case is an n-channel device. This symbol shows the four-terminal structure of the MOSFET device.

In most applications in this text, we will implicitly assume that the source and substrate terminals are connected together. Explicitly drawing the substrate terminal for each transistor in a circuit becomes redundant and makes the circuits appear more complex. Instead, we will use the circuit symbol for the n-channel MOSFET shown in Figure 3.12(b). In this symbol, the arrowhead is on the source terminal and it indicates the direction of current, which for the n-channel device is out of the source. By including the arrowhead in the symbol, we do not need to explicitly indicate the source and drain terminals. We will use this circuit symbol throughout the text except in specific applications.

In more advanced texts and journal articles, the circuit symbol of the n-channel MOSFET shown in Figure 3.12(c) is generally used. The gate terminal is obvious and it is implicitly understood that the "top" terminal is the drain and the "bottom" terminal is the source. The top terminal, in this case the drain, is usually at a more positive voltage than the bottom terminal. In this introductory text, we will use the symbol shown in Figure 3.12(b) for clarity.

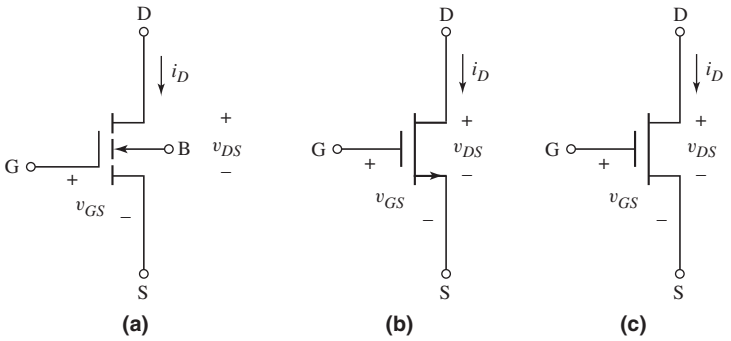


Figure 3.12 The n-channel enhancement-mode MOSFET: (a) conventional circuit symbol, (b) circuit symbol that will be used in this text, and (c) a simplified circuit symbol used in more advanced texts

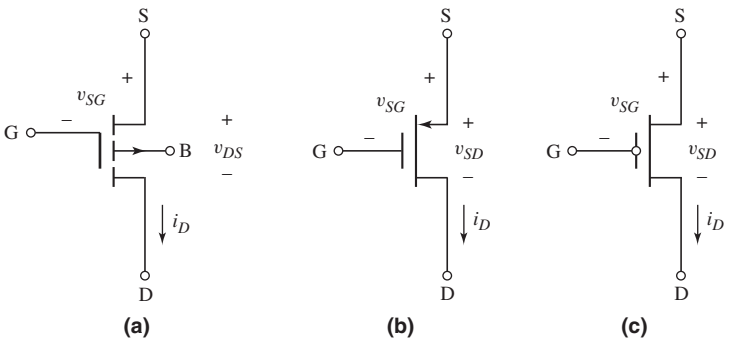


Figure 3.13 The p-channel enhancement-mode MOSFET: (a) conventional circuit symbol, (b) circuit symbol that will be used in this text, and (c) a simplified circuit symbol used in more advanced texts

The conventional circuit symbol for the p-channel enhancement-mode MOSFET appears in Figure 3.13(a). Note that the arrowhead direction on the substrate terminal is reversed from that in the n-channel enhancement-mode device. This circuit symbol again shows the four terminal structure of the MOSFET device.

The circuit symbol for the p-channel enhancement-mode device shown in Figure 3.13(b) will be used in this text. The arrowhead is on the source terminal indicating the direction of the current, which for the p-channel device is into the source terminal.

In more advanced texts and journal articles, the circuit symbol of the p-channel MOSFET shown in Figure 3.13(c) is generally used. Again, the gate terminal is obvious but includes the O symbol to indicate that this is a PMOS device. It is implicitly understood that the "top" terminal is the source and the "bottom" terminal is the drain. The top terminal, in this case the source, is normally at a higher potential than the bottom terminal. Again, in this text, we will use the symbol shown in Figure 3.13(b) for clarity.

3.1.7 Additional MOSFET Structures and Circuit Symbols

Before we start analyzing MOSFET circuits, there are two other MOSFET structures in addition to the n-channel enhancement-mode device and the p-channel enhancement-mode device that need to be considered.

3

n-Channel Depletion-Mode MOSFET

Figure 3.14(a) shows the cross section of an n-channel **depletion-mode** MOSFET. When zero volts are applied to the gate, an n-channel region or inversion layer exists under the oxide as a result, for example, of impurities introduced during device fabrication. Since an n-region connects the n-source and n-drain, a drain-to-source current may be generated in the channel even with zero gate voltage. The term **depletion mode** means that a channel exists even at zero gate voltage. A negative gate voltage must be applied to the n-channel depletion-mode MOSFET to turn the device off.

Figure 3.14(b) shows the n-channel depletion mode MOSFET with a negative applied gate-to-source voltage. A negative gate voltage induces a space-charge region under the oxide, thereby reducing the thickness of the n-channel region. The reduced thickness decreases the channel conductance, which in turn reduces the drain current. When the gate voltage is equal to the threshold voltage, which is

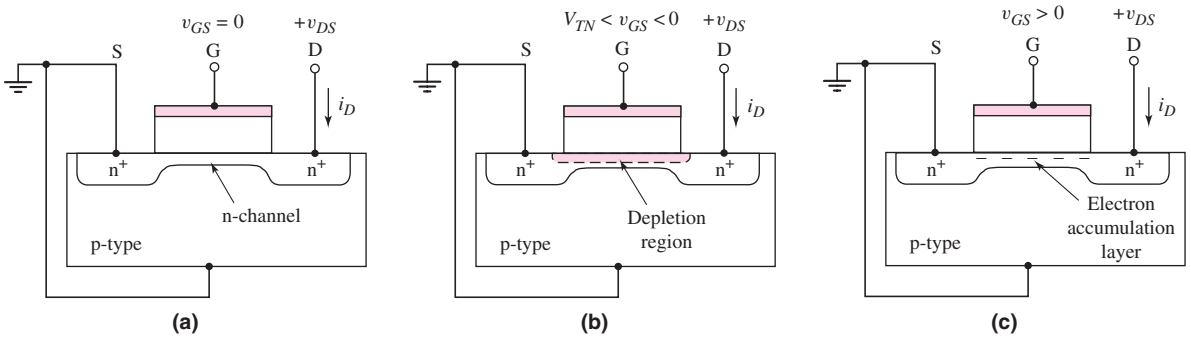


Figure 3.14 Cross section of an n-channel depletion mode MOSFET for: (a) $v_{GS} = 0$, (b) $v_{GS} < 0$, and (c) $v_{GS} > 0$

negative for this device, the induced space-charge region extends completely through the n-channel region, and the current goes to zero. A positive gate voltage creates an electron accumulation layer, as shown in Figure 3.14(c) which increases the drain current. The general i_D versus v_{DS} family of curves for the n-channel depletion-mode MOSFET is shown in Figure 3.15.

The current–voltage characteristics defined by Equations (3.2(a)) and (3.2(b)) apply to both enhancement- and depletion-mode n-channel devices. The only difference is that the threshold voltage V_{TN} is positive for the enhancement-mode MOSFET and negative for the depletion-mode MOSFET. Even though the current–voltage characteristics of enhancement- and depletion-mode devices are described by the same equations, different circuit symbols are used, simply for purposes of clarity.

The conventional circuit symbol for the n-channel depletion-mode MOSFET is shown in Figure 3.16(a). The vertical solid line denoting the channel indicates the device is depletion mode. A comparison of Figures 3.12(a) and 3.16(a) shows that the only difference between the enhancement- and depletion-mode symbols is the broken versus the solid line representing the channel.

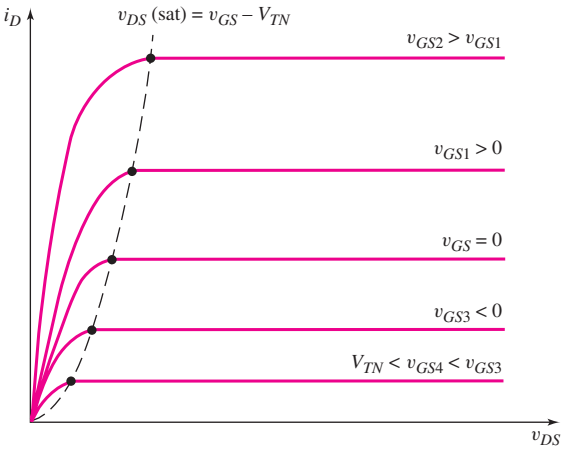


Figure 3.15 Family of i_D versus v_{DS} curves for an n-channel depletion-mode MOSFET. Note again that the v_{DS}(sat) voltage is a single point on each curve.

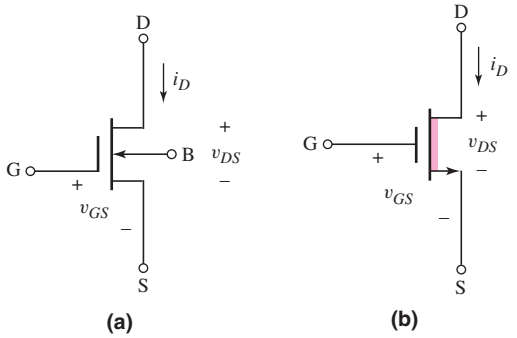


Figure 3.16 The n-channel depletion-mode MOSFET: (a) conventional circuit symbol and (b) simplified circuit symbol

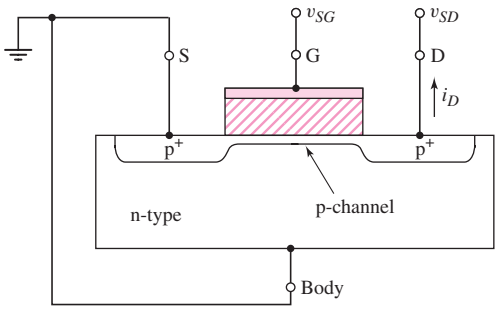


Figure 3.17 Cross section of p-channel depletion-mode MOSFET showing the p-channel under the oxide at zero gate voltage

A simplified symbol for the n-channel depletion-mode MOSFET is shown in Figure 3.16(b). The arrowhead is again on the source terminal and indicates the direction of current, which for the n-channel device is out of the source. The heavy solid line represents the depletion-mode channel region. Again, using a different circuit symbol for the depletion-mode device compared to the enhancement-mode device is simply for clarity in a circuit diagram.

4

p-Channel Depletion-Mode MOSFET

Figure 3.17 shows the cross section of a p-channel depletion-mode MOSFET, as well as the biasing configuration and current direction. In the depletion-mode device, a channel region of holes already exists under the oxide, even with zero gate voltage. A positive gate voltage is required to turn the device off. Hence the threshold voltage of a p-channel depletion-mode MOSFET is positive ($V_{TP} > 0$).

The conventional and simplified circuit symbols for the p-channel depletion-mode device are shown in Figure 3.18. The heavy solid line in the simplified symbol represents the channel region and denotes the depletion-mode device. The arrowhead is again on the source terminal and it indicates the current direction.

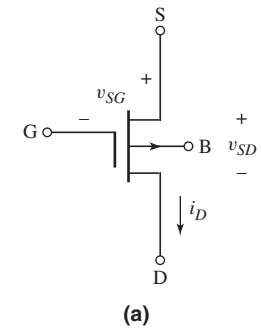


Figure 3.18 The p-channel depletion mode MOSFET: (a) conventional circuit symbol and (b) simplified circuit symbol

Complementary MOSFETs

Complementary MOS (CMOS) technology uses both n-channel and p-channel devices in the same circuit. Figure 3.19 shows the cross section of n-channel and p-channel devices fabricated on the same chip. CMOS circuits, in general, are more complicated to fabricate than circuits using entirely NMOS or PMOS devices. Yet, as we will see in later chapters, CMOS circuits have great advantages over just NMOS or PMOS circuits.

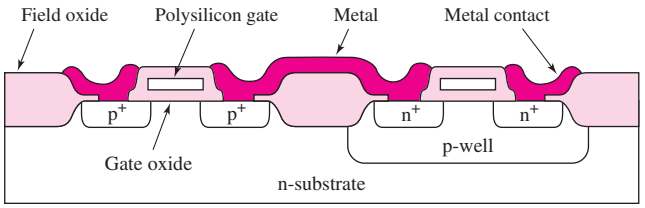


Figure 3.19 Cross sections of n-channel and p-channel transistors fabricated with a p-well CMOS technology

In order to fabricate n-channel and p-channel devices that are electrically equivalent, the magnitude of the threshold voltages must be equal, and the n-channel and p-channel conduction parameters must be equal. Since, in general, μ_n, and μ_p are not equal, the design of equivalent transistors involves adjusting the width-to-length ratios of the transistors.

3.1.8 Summary of Transistor Operation

We have presented a first-order model of the operation of the MOS transistor. For an n-channel enhancement-mode MOSFET, a positive gate-to-source voltage, greater than the threshold voltage V_{TN}, must be applied to induce an electron inversion layer. For $v_{GS} > V_{TN}$, the device is turned on. For an n-channel depletion-mode device, a channel between the source and drain exists even for $v_{GS} = 0$. The threshold voltage is negative, so that a negative value of v_{GS} is required to turn the device off.

For a p-channel device, all voltage polarities and current directions are reversed compared to the NMOS device. For the p-channel enhancement-mode transistor, $V_{TP} < 0$ and for the depletion-mode PMOS transistor, $V_{TP} > 0$.

Table 3.1 lists the first-order equations that describe the i–v relationships in MOS devices. We note that K_n and K_p are positive values and that the drain current i_D is positive into the drain for the NMOS device and positive out of the drain for the PMOS device.

Table 3.1 Summary of the MOSFET current–voltage relationships

NMOS	PMOS
Nonsaturation region ($v_{DS} < v_{DS}(\text{sat})$)	Nonsaturation region ($v_{SD} < v_{SD}(\text{sat})$)
$i_D = K_n[2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2]$	$i_D = K_p[2(v_{SG} + V_{TP})v_{SD} - v_{SD}^2]$
Saturation region ($v_{DS} > v_{DS}(\text{sat})$)	Saturation region ($v_{SD} > v_{SD}(\text{sat})$)
$i_D = K_n(v_{GS} - V_{TN})^2$	$i_D = K_p(v_{SG} + V_{TP})^2$
Transition point	Transition point
$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$	$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$
Enhancement mode	Enhancement mode
$V_{TN} > 0$	$V_{TP} < 0$
Depletion mode	Depletion mode
$V_{TN} < 0$	$V_{TP} > 0$

3.1.9 Short-Channel Effects

The current–voltage relations given by Equations (3.2(a)) and (3.2(b)) for the n-channel device and Equations (3.4(a)) and (3.4(b)) for the p-channel device are the ideal relations for long-channel devices. A long-channel device is generally one whose channel length is greater than 2 μm. In this device, the horizontal electric field in the channel induced by the drain voltage and the vertical electric field induced by the gate voltage can be treated independently. However, the channel length of present-day devices is on the order of 0.2 μm or less.

There are several effects in these short-channel devices that influence and change the long-channel current–voltage characteristics. One such effect is a variation

$V_{TN} \propto L$

in threshold voltage. The value of threshold voltage is a function of the channel length. This variation must be considered in the design and fabrication of these devices. The threshold voltage also becomes a function of the drain voltage. As the drain voltage increases, the effective threshold voltage decreases. This effect also influences the current–voltage characteristics.

The process conduction parameters, k'_n and k'_p, are directly related to the carrier mobility. We have assumed that the carrier mobilities and corresponding process conduction parameters are constant. However, the carrier mobility values are functions of the vertical electric field in the inversion layer. As the gate voltage and vertical electric field increase, the carrier mobility decreases. This result, again, directly influences the current–voltage characteristics of the device.

Another effect that occurs in short-channel devices is velocity saturation. As the horizontal electric field increases, the velocity of the carriers reaches a constant value and will no longer increase with an increase in drain voltage. Velocity saturation will lower the $V_{DS}(\text{sat})$ voltage value. The drain current will reach its saturation value at a smaller V_{DS} voltage. The drain current also becomes approximately a linear function of the gate voltage in the saturation region rather than the quadratic function of gate voltage in the long-channel characteristics.

Although the analysis of modern MOSFET circuits must take into account these short-channel effects, we will use the long-channel current–voltage relations in this introductory text. We will still be able to obtain a good basic understanding of the operation and characteristics of these devices, and we can still obtain a good basic understanding of the operation and characteristics of MOSFET circuits using the ideal long-channel current–voltage relations.

3.1.10 Additional Nonideal Current–Voltage Characteristics

The five nonideal effects in the current–voltage characteristics of MOS transistors are: the finite output resistance in the saturation region, the body effect, subthreshold conduction, breakdown effects, and temperature effects. This section will examine each of these effects.

Finite Output Resistance

In the ideal case, when a MOSFET is biased in the saturation region, the drain current i_D is independent of drain-to-source voltage v_{DS}. However, in actual MOSFET i_D versus v_{DS} characteristics, a nonzero slope does exist beyond the saturation point. For $v_{DS} > v_{DS}(\text{sat})$, the actual point in the channel at which the inversion charge goes to zero moves away from the drain terminal (see Figure 3.9(d)). The effective channel length decreases, producing the phenomenon called **channel length modulation.**

An exaggerated view of the current–voltage characteristics is shown in Figure 3.20. The curves can be extrapolated so that they intercept the voltage axis at a point $v_{DS} = -V_A$. The voltage V_A is usually defined as a positive quantity. The slope of the curve in the saturation region can be described by expressing the i_D versus v_{DS} characteristic in the form, for an n-channel device,

$$i_D = K_n[(v_{GS} - V_{TN})^2(1 + \lambda v_{DS})] \tag{3.7}$$

where λ is a positive quantity called the channel-length modulation parameter.

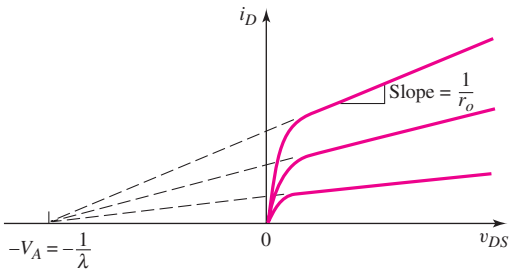


Figure 3.20 Family of i_D versus v_{DS} curves showing the effect of channel length modulation producing a finite output resistance

The parameters λ and V_A are related. From Equation (3.7), we have $(1 + \lambda v_{DS}) = 0$ at the extrapolated point where $i_D = 0$. At this point, $v_{DS} = -V_A$, which means that $V_A = 1/\lambda$.

The output resistance due to the channel length modulation is defined as

$$r_o = \left(\frac{\partial i_D}{\partial v_{DS}}\right)^{-1}\Bigg|_{v_{GS}=\text{const.}} \tag{3.8}$$

From Equation (3.7), the output resistance, evaluated at the Q-point, is

$$r_o = [\lambda K_n (V_{GSQ} - V_{TN})^2]^{-1} \tag{3.9(a)}$$

or

$$r_o \cong [\lambda I_{DQ}]^{-1} = \frac{1}{\lambda I_{DQ}} = \frac{V_A}{I_{DQ}} \tag{3.9(b)}$$

The output resistance r_o is also a factor in the small-signal equivalent circuit of the MOSFET, which is discussed in the next chapter.

Body Effect

Up to this point, we have assumed that the substrate, or body, is connected to the source. For this bias condition, the threshold voltage is a constant.

In integrated circuits, however, the substrates of all n-channel MOSFETs are usually common and are tied to the most negative potential in the circuit. An example of two n-channel MOSFETs in series is shown in Figure 3.21. The p-type

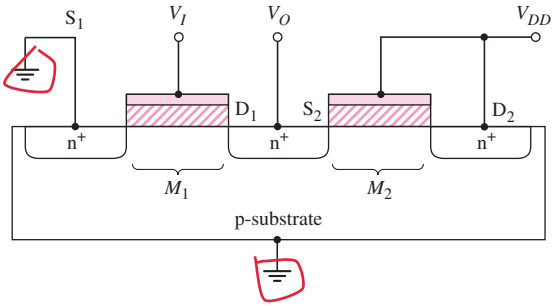


Figure 3.21 Two n-channel MOSFETs fabricated in series in the same substrate. The source terminal, S_2, of the transistor M_2 is more than likely not at ground potential.

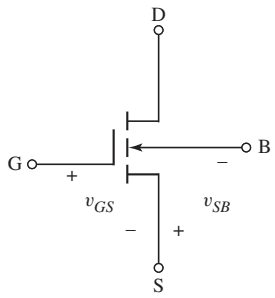


Figure 3.22 An n-channel enhancement-mode MOSFET with a substrate voltage

substrate is common to the two transistors, and the drain of M_1 is common to the source of M_2. When the two transistors are conducting, there is a nonzero drain-to-source voltage on M_1, which means that the source of M_2 is not at the same potential as the substrate. These bias conditions mean that a zero or reverse-bias voltage exists across the source–substrate pn junction, and a change in the source–substrate junction voltage changes the threshold voltage. This is called the **body effect.** The same situation exists in p-channel devices.

For example, consider the n-channel device shown in Figure 3.22. To maintain a zero- or reverse-biased source–substrate pn junction, we must have $v_{SB} \geq 0$. The threshold voltage for this condition is given by

$$V_{TN} = V_{TNO} + \gamma\left[\sqrt{2\phi_f + v_{SB}} - \sqrt{2\phi_f}\right] \tag{3.10}$$

where V_{TNO} is the threshold voltage for $v_{SB} = 0$; γ, called the bulk threshold or **body-effect parameter,** is related to device properties, and is typically on the order of 0.5 $V^{1/2}$; and ϕ_f is a semiconductor parameter, typically on the order of 0.35 V, and is a function of the semiconductor doping. We see from Equation (3.10) that the threshold voltage in n-channel devices increases due to this body effect.

The body effect can cause a degradation in circuit performance because of the changing threshold voltage. However, we will generally neglect the body effect in our circuit analyses, for simplicity.

Subthreshold Conduction

If we consider the ideal current-voltage relationship for the n-channel MOSFET biased in the saturation region, we have, from Equation (3.2(b)),

$$i_D = K_n(v_{GS} - V_{TN})^2$$

Taking the square root of both sides of the equation, we obtain

$$\sqrt{i_D} = \sqrt{K_n}(v_{GS} - V_{TN}) \tag{3.11}$$

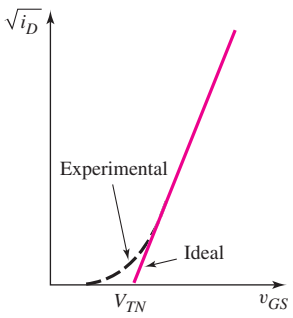


Figure 3.23 Plot of $\sqrt{i_D}$ versus v_{GS} for a MOSFET biased in the saturation region showing subthreshold conduction. Experimentally, a subthreshold current exists even for $v_{GS} < V_{TN}$.

From Equation (3.11), we see that $\sqrt{i_d}$ is a linear function of v_{GS}. Figure 3.23 shows a plot of this ideal relationship.

Also plotted in Figure 3.23 are experimental results, which show that when v_{GS} is slightly less than V_{TN}, the drain current is not zero, as previously assumed. This current is called the **subthreshold current.** The effect may not be significant for a single device, but if thousands or millions of devices on an integrated circuit are biased just slightly below the threshold voltage, the power supply current will not be zero but may contribute to significant power dissipation in the integrated circuit. One example of this is a dynamic random access memory (DRAM), as we will see in Chapter 16.

In this text, for simplicity we will not specifically consider the subthreshold current. However, when a MOSFET in a circuit is to be turned off, the "proper" design of the circuit must involve biasing the device at least a few tenths of a volt below the threshold voltage to achieve "true" cutoff.

Breakdown Effects

Several possible breakdown effects may occur in a MOSFET. The drain-to-substrate pn junction may break down if the applied drain voltage is too high and avalanche multiplication occurs. This breakdown is the same reverse-biased pn junction breakdown discussed in Chapter 1 in Section 1.2.5.

As the size of the device becomes smaller, another breakdown mechanism, called *punch-through,* may become significant. **Punch-through** occurs when the drain voltage is large enough for the depletion region around the drain to extend completely through the channel to the source terminal. This effect also causes the drain current to increase rapidly with only a small increase in drain voltage.

A third breakdown mechanism is called **near-avalanche** or **snapback breakdown.** This breakdown process is due to second-order effects within the MOSFET. The source-substrate-drain structure is equivalent to that of a bipolar transistor. As the device size shrinks, we may begin to see a parasitic bipolar transistor action with increases in the drain voltage. This parasitic action enhances the breakdown effect.

If the electric field in the oxide becomes large enough, breakdown can also occur in the oxide, which can lead to catastrophic failure. In silicon dioxide, the electric field at breakdown is on the order of 6×10^6 V/cm, which, to a first approximation, is given by $E_{ox} = V_G/t_{ox}$. A gate voltage of approximately 30 V would produce breakdown in an oxide with a thickness of $t_{ox} = 500$ Å. However, a safety margin of a factor of 3 is common, which means that the maximum safe gate voltage for $t_{ox} = 500$ Å would be 10 V. A safety margin is necessary since there may be defects in the oxide that lower the breakdown field. We must also keep in mind that the input impedance at the gate is very high, and a small amount of static charge accumulating on the gate can cause the breakdown voltage to be exceeded. To prevent the accumulation of static charge on the gate capacitance of a MOSFET, a gate protection device, such as a reverse-biased diode, is usually included at the input of a MOS integrated circuit.

Temperature Effects

Both the threshold voltage V_{TN} and conduction parameter K_n are functions of temperature. The magnitude of the threshold voltage decreases with temperature, which means that the drain current increases with temperature at a given V_{GS}. However, the conduction parameter is a direct function of the inversion carrier mobility, which decreases as the temperature increases. Since the temperature dependence of mobility is larger than that of the threshold voltage, the net effect of increasing temperature is a decrease in drain current at a given V_{GS}. This particular result provides a negative feedback condition in power MOSFETs. A decreasing value of K_n inherently limits the channel current and provides stability for a power MOSFET.

Test Your Understanding

TYU 3.1 (a) An n-channel enhancement-mode MOSFET has a threshold voltage of $V_{TN} = 1.2$ V and an applied gate-to-source voltage of $v_{GS} = 2$ V. Determine the region of operation when: (i) $v_{DS} = 0.4$ V; (ii) $v_{DS} = 1$ V; and (iii) $v_{DS} = 5$ V. (b) Repeat part (a) for an n-channel depletion-mode MOSFET with a threshold voltage of $V_{TN} = -1.2$ V. (Ans. (a) (i) nonsaturation, (ii) saturation, (iii) saturation; (b) (i) nonsaturation, (ii) nonsaturation, (iii) saturation)

TYU 3.2 The NMOS devices described in Exercise TYU 3.1 have parameters $W = 20\,\mu$m, $L = 0.8\,\mu$m, $t_{ox} = 200$ Å, $\mu_n = 500$ cm^2/V–s, and $\lambda = 0$. (a) Calculate the conduction parameter K_n for each device. (b) Calculate the drain current for each bias condition listed in Exercise TYU 3.1. (Ans. (a) $K_n = 1.08$ mA/V^2; (b) $i_D = 0.518$ mA, 0.691 mA, and 0.691 mA; $i_D = 2.59$ mA, 5.83 mA, and 11.1 mA)

TYU 3.3 (a) A p-channel enhancement-mode MOSFET has a threshold voltage of $V_{TP} = -1.2\,\text{V}$ and an applied source-to-gate voltage of $v_{SG} = 2\,\text{V}$. Determine the region of operation when (i) $v_{SD} = 0.4\,\text{V}$, (ii) $v_{SD} = 1\,\text{V}$, and (iii) $v_{SD} = 5\,\text{V}$. (b) Repeat part (a) for a p-channel depletion-mode MOSFET with a threshold voltage of $V_{TP} = +1.2\,\text{V}$. (Ans. (a) (i) nonsaturation, (ii) saturation, (iii) saturation; (b) (i) nonsaturation, (ii) nonsaturation, (iii) saturation)

TYU 3.4 The PMOS devices described in Exercise TYU 3.3 have parameters $W = 10\,\mu\text{m}$, $L = 0.8\,\mu\text{m}$, $t_{ox} = 200\,\text{Å}$, $\mu_p = 300\,\text{cm}^2/\text{V–s}$, and $\lambda = 0$. (a) Calculate the conduction parameter K_p for each device. (b) Calculate the drain current for each bias condition listed in Exercise TYU 3.3. (Ans. (a) $K_p = 0.324\,\text{mA/V}^2$; (b) $i_D = 0.156\,\text{mA}$, 0.207 mA; and 0.207 mA; $i_D = 0.778\,\text{mA}$, 1.75 mA, and 3.32 mA)

TYU 3.5 The parameters of an NMOS enhancement-mode device are $V_{TN} = 0.25\,\text{V}$ and $K_n = 10\ \mu\ \text{A/V}^2$. The device is biased at $v_{GS} = 0.5\,\text{V}$. Calculate the drain current when (i) $v_{DS} = 0.5\,\text{V}$ and (ii) $v_{DS} = 1.2\,\text{V}$ for (a) $\lambda = 0$ and (b) $\lambda = 0.03\,\text{V}^{-1}$. (c) Calculate the output resistance r_o for parts (a) and (b). (Ans. (a) (i) and (ii) $i_D = 0.625\,\mu\text{A}$; (b) (i) $i_D = 0.6344\,\mu\text{A}$, (ii) $i_D = 0.6475\,\mu\text{A}$; (c) (i) $r_o = \infty$, (ii) $r_o = 53.3\,\text{M}\Omega$).

TYU 3.6 An NMOS transistor has parameters $V_{TNO} = 0.4\,\text{V}$, $\gamma = 0.15\,\text{V}^{1/2}$, and $\phi_f = 0.35\,\text{V}$. Calculate the threshold voltage when (a) $v_{SB} = 0$, (b) $v_{SB} = 0.5\,\text{V}$, and (c) $v_{SB} = 1.5\,\text{V}$. (Ans. (a) 0.4 V, (b) 0.439 V, (c) 0.497 V)

3.2 MOSFET DC CIRCUIT ANALYSIS

Objective: • Understand and become familiar with the dc analysis and design techniques of MOSFET circuits.

In the last section, we considered the basic MOSFET characteristics and properties. We now start analyzing and designing the dc biasing of MOS transistor circuits. A primary purpose of the rest of the chapter is to continue to become familiar and comfortable with the MOS transistor and MOSFET circuits. The dc biasing of MOSFETs, the focus of this chapter, is an important part of the design of amplifiers. MOSFET amplifier design is the focus of the next chapter.

In most of the circuits presented in this chapter, resistors are used in conjunction with the MOS transistors. In a real MOSFET integrated circuit, however, the resistors are generally replaced by other MOSFETs, so the circuit is composed entirely of MOS devices. In general, a MOSFET device requires a smaller area than a resistor. As we go through the chapter, we will begin to see how this is accomplished and as we finish the text, we will indeed analyze and design circuits containing only MOSFETs.

In the dc analysis of MOSFET circuits, we can use the ideal current–voltage equations listed in Table 3.1 in Section 3.1.

3.2.1 Common-Source Circuit

One of the basic MOSFET circuit configurations is called the **common-source circuit.** Figure 3.24 shows one example of this type of circuit using an n-channel