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المحتويات

Application of Artificial Neural Networks in Mid-Term Load Forecasting for Residential Sector in Mosul City (Iraq)

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Abstract

In this paper, the application of the Artificial Neural Networks (ANN) to design a Mid-Term Load Forecasting (MTLF) model for power system to supply electricity to certain residential sector in MOSUL city (North of Iraq) was explored. One important architecture of neural networks named Multi-Layer Perceptron (MLP) feed forward with supervised learning method and Back Propagation (BP) algorithm to model MTLF system is used. The model was trained and tested using one year data collected from the metrological office, and Householders (HHs) implemented in this work. In this model a new approach concerning the input variables of the model is applied by disaggregate the daily peak load at the feeder of the residential sector to its main FIVE components namely (lighting, domestic, cooling, water heating, and space heating). These components are used as input variables with additional weather conditions, and season to forecast the daily peak load of one week ahead. The results show that MLP network has minimum forecasting error MAPE (1.921 %), and can be considered as a good method to model the MTLF systems.

Keywords: Artificial Neural Network, Iraqi load forecasting, MLP and Back Propagation, MTLF.

أستخدام الشبكة العصبية الصناعية في التنبؤ بالاحمال الكهربائية للمدى المتوسط للقطاع السكني في العراق

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الملخص

تم في هذا البحث اجراء عملية التنبؤ للحمولة الكهربائية في المدى المتوسط باستخدام أحد نماذج الشبكة العصبية الصناعية وتحديدا (المدرك المتعدد الطبقات) لقدرة هذا النموذج على تمثيل أي علاقة غير خطية معقدة بين الحمولة للطاقة وبين العوامل المؤثرة عليها. في هذا النظام تم اعتماد طريقة جديدة في أختيار المتغيرات الداخلة، حيث تم فصل مكونات الحمولة الى مركبات خمسة هي (الانارة ، الاجهزة المنزلية ، التبريد ، تسخين الماء، التدفئة). تم استخدام هذه المركبات كمتغيرات داخلة الى النظام المقترح للشبكة العصبية مع بقية العوامل الجوية الاخرى ، وطبق هذا النموذج باستخدام بيانات حقيقية لقطاع سكني معين بعد جمع البيانات اللازمة من المغذي الرئيسي لهذا القطاع حول الحمولة اليومية الحقيقية ودرجات الحرارة اليومية من الارصاد الجوية ولمدة سنة كاملة. بعد عملية التدريب والفحص لهذا النموذج بأستخدام برنامج (ماتلاب) تم أستخدامه في عملية التوقع للحمل الكهربائي اليومي المتوقع لاسبوع مقبل ، وكانت النتائج دقيقة بين الحمل اليومي الحقيقي والحمل المتوقع وكانت نسبة الخطأ (1.921 %). تم تقييم أداء النموذج بأستخدام متوسط مربع الخطأ والنسبة المئوية لمتوسط الخطأ المطلق ومعامل الارتباط.

Introduction

Optimal daily operation of electric power generation plants is very essential for any power utility. The reliable and continuous supply of electrical energy is needed for the functioning the day complex societies. Now to generate reasonably required electricity, forecast of future demand is needed. This estimation is considered the foundation for the design and operation of the electrical power system, and the detail specifications of the transmission and distribution components of the electrical system can be specified.

Load forecasting is a difficult task because the consumption is influenced by many factors such as weather conditions, economy status, habits and behavior of individuals, and numbers and types of appliances used by the HHs, therefore inaccurate load forecast may cause increasing in operating costs, failure in providing sufficient electric power, and damage of electrical utilities. Load forecasts can be classified in terms of planning horizon's duration as:

- From 1 hour to 1 week as short term load forecasting STLF.
- From 1 week to several months as mid-term load forecasting MTLF.
- from 1 year to several years as long term load forecasting LTLF.

This classification is important for different operations within utility company. A power delivery system exists because customers need electric power in order to accomplish their daily tasks. Generally, electrical power generated is distributed to 4 main types of customers; residential, commercial, industrial, and agricultural. The major part of electricity is consumed by residential sector especially in Iraq.

Modern load forecasting techniques such as expert systems, ANN, fuzzy logic, and wavelets have been developed recently showing encourage results. Among them ANN techniques are particularly attractive as they have the ability to handle the non-linear relationship between the load and factors affecting this load directly from historical data. Given a sample of input and output vectors, ANN is able automatically map the relationship between them.

Many researches have been developed different types of architecture of neural networks in MTLF using many methods of identification of input variables. Some were used, day type, and pervious average daily power demand as input variables [1], or previous (load ,temperature, humidity, wind speed, and daily index) [2]. Others used the historical load, weather conditions, macroeconomic, demographic and month index as input variables [3]. P. Bunnoon, K [4] , considered the variables such as, consumer price of electricity, industrial index, weather conditions such as (temperature, humidity, rainfall, and wind speed), and historical electrical load were used as input variables for ANN models.

This research aims to develop real case study of MTLF of average daily peak load forecasting for one week ahead in a certain residential sector which is considered as high consumption electrical energy sector, located in Mosul city, using forward back propagation supervised MLP network model. Time, weather, different types of load components related to the primary feeder are considered as input variables in the model. Historical data of load consumption at a primary feeder, and weather conditions are collected and used in the research for the period of one year starting from 1 April 2010, to 31 March 2011.

This paper is organized as follows ; section II provides overview of ANN technique especially MLP model, while section III presents the case study which is

explained in details concerning electric load in residential sector, including the analysis of collected data, identification of input variables and training algorithm. The experimental results and discussion are presented in section IV, and the paper concludes in section V.

ANN Models

Artificial Neural Networks ANN is a good choice to study the load forecasting problems, for its ability to map a complex non–linear relationship between the load and its affecting factors [5], [6]. ANN models consists of a number of simple processing elements called (neurons) which are connected together in a form of layers designed to do a variety of tasks. It is used in many applications; pattern recognition, optimization, prediction, and automatic control. For load forecasting, the forward back propagation supervised MLP type of networks is a popular choice because it offers a good generalization abilities. It includes an input, hidden, and output layers, see Fig.1. Input variables comes from historical data corresponding to the factors that affect the load. The output are the desired forecasting results, which are (in our case) the average daily peak load demand for one week ahead .

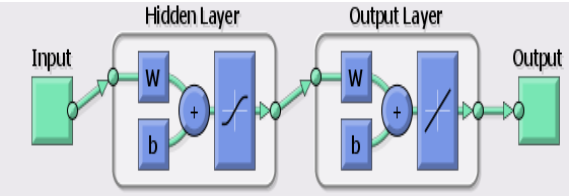

Fig. (1): The block diagram of ANN use in load forecasting.

The input vectors, number of neurons in a hidden layer, transfer functions, selection of training method, and other parameters of BP algorithm (weights, biases, learning rate, momentum factors, epochs…..etc) all these affects the forecasting performance and hence need to be chosen carefully. Any ANN model must be trained to do a certain job making use of historical input data [7]. There are many algorithms of training process, a BP is the most training algorithm used in load forecasting. In order to evaluate the performance of the model, the load forecast was compared to the actual load data. The Mean Absolute Percentage Error (MAPE), and Mean Square Error (MSE) are used in measuring the accuracy of the proposed ANN model .

Case Study

It is generally considered that the demand for electricity in residential sector is mainly depends on some factors, like (weather conditions, types of electrical appliances used in different seasons, number of persons in each household, lifestyle of HHs, price of electricity, income of HHs ,……etc), hence in studying the residential electricity demand, one must take into consideration some issues, among them are [8] :

- Numbers and types of electrical appliances ownership by HHs.
- Seasonality of these appliances utilization such as winter and summer appliances.
- Heterogeneous consumers and their behavior in each season.
- Weather conditions especially the temperature factor, rainfall.
- Others, like household income and its buying ability for appliances, price of electricity, structure of house, and size of household …..etc.

A. Collecting the Data and Input Factors:

The selected residential area is divided into 8 groups, and for each group it is assigned a person his responsibility is to collect the following information's from samples of householders selected randomly in each group. Data are collected for one year period from (1 April 2010 to 31 March 2011). These information are :

- Numbers and types of electrical appliances in each household like (space heater, air conditioners, fans, refrigerator, deep freezer, cooking equipments, water pump, water heaters, washing machine, laundry, lighting, TV, radio, PC, dish, others ….etc.
- Daily average load consumption for electricity usage for each type of appliances ownership by HHs.
- Average daily peak load at the feeder supplying electricity to the sector.
- From meteorological department in the city, weather conditions especially daily maximum, minimum temperature for the corresponding period are collected.

All these information are analyzed to find the average daily peak load consumption for the sector (8 groups). These data are collected by the cooperation of householders lived in the sector and the persons who do special efforts in collecting the data during one year. Fig. 2 shows the behavior of the average daily peak load at the feeder with related maximum and minimum temperatures. This daily load is decomposed into 5 main components according to the level of consumption as follows:

- Lighting component, which includes indoor and outdoor lightings.
- Domestic component, which includes the load consumed by daily usage of necessary appliances in every house like kitchen equipments, refrigerator, freezer, washing machine, water pump, TV, radio, PC, other electronic devices.
- Cooling components, which include water cooler, air cooler, air conditioning, ceiling and stand fans.
- Space heating components, which includes mainly the electrical space heaters. This device used widely in residential sector in cold winter days, and it consumes high electrical energy.
- Water heater component, it is considered very essential since it shares high portion of energy consumed by each household along the year. This device is used in all seasons to heat the water. We decompose this component from space heating component since the later used only in cold winter days.

All these components are determined as a percentage of the total daily average peak load consumption for the sector at the feeder. Some results of determination are listed in Table I. for selected winter and summer months

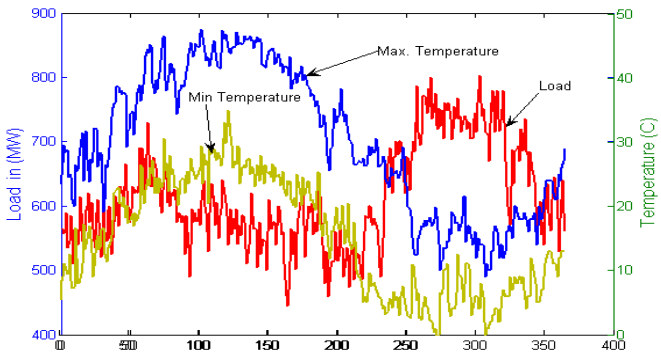

Fig. (2): Electrical load , maximum temperature for one year (April 2010 to March 2011)

Table (I): Consumption of each load components as a percentage of total daily load of August (summer) and January (winter) months.

Component type	August 2010	January 2011
Lighting	06.71 %	07.09 %
Domestic	21.33 %	17.07 %
Cooling	65.53 %	0.000 %
Space heating	01.40 %	29.31 %
Water heater	05.03 %	46.53 %
Total	100 %	100 %

B. Load components and factors affecting the load.

The load components which are vary between winter and summer months are (cooling, space heater, and water heater) is presented in Fig. 3 which show high fluctuations related with temperature. They affects the type and appliances usage by HHs. Selection of input factors is the most important work in building an ANN model. This task is mainly depends on engineering judgment and designer experience, and it is carried out by trial and error. Efficient selection of input variables yields an accurate load forecasting. In Fig. 3 it is clear that the difference in weather conditions effect very much on type of the equipments used, like space heater in winter and cooling equipments in summer. Both types can not be used at the same time.

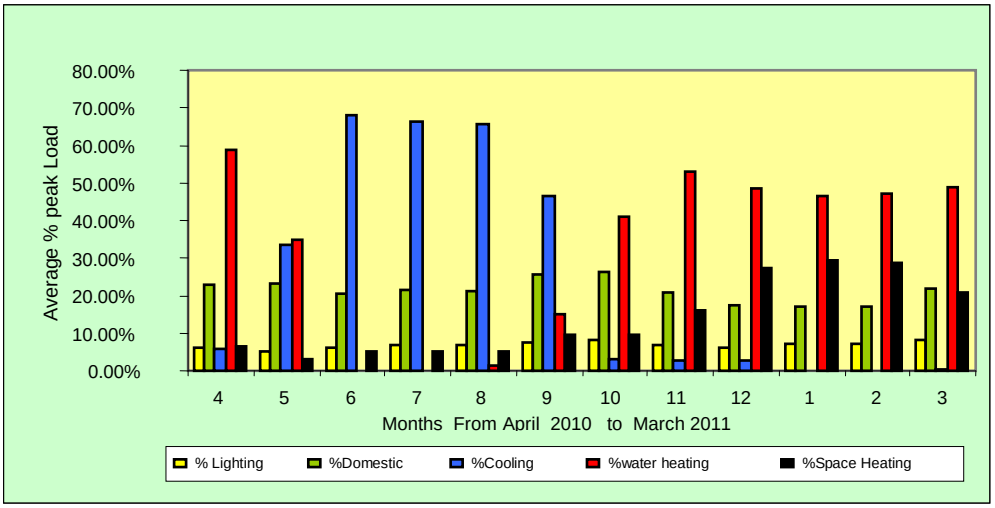

Fig. (3): Monthly average percentage peak load components for one year (April 2010 to March 2011).

In general, in load forecasting the most important input variables which affect the load forecasting are:

- Day of the week. Load is changed from day to day during a week. Fig. 4 shows the daily load for a selected cold winter month (January) and a hot summer month (August). It is clear that load consumption is different on different days, so day indicator is helpful in load forecasting.
- Weather variables. Temperature, which is considered in this work as the most important weather variable. It limits the usage and type of appliances ownership by

HHs. Daily maximum, and minimum temperature are used as input variables in this work. See Fig. 2.

- Historical load consumption. The recent and past load trend is mainly a backbone of the forecast. In Fig.3. the historical load components pattern is non-linear relationship, and non stationary in time. It is clear that it has a strong correlation with temperature.

In this study the detail input factors are composed of the following:

- Maximum daily average peak loads at the feeder for current day.
- Five main daily load components (lighting, domestic, cooling, space heating, water heating) which is as a percentage value of the total average peak daily load at the feeder.
- Day of the week, index used from 1 (Sunday) to index 7 (Saturday).
- Day number in a sequence, starting from 1 to 365 for one year period in (days).
- Daily maximum and minimum temperature for current day.
- Daily maximum and minimum temperature for one week a head.

These 12 input factors are used in this study to forecast the daily peak load for the next week. The output (target) is the daily load for one week a head. see Fig. 5.

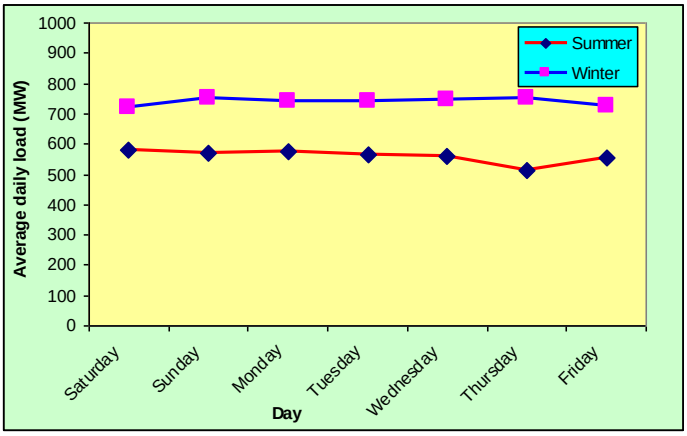

Fig. (4): Average daily peak load in winter (January) and summer (August) seasons.

C. Designing the ANN model

The proposed ANN model used in this work is the supervised BP multi-layers perceptron MLP feed forward type neural network. It consists of 3 layers, input, hidden, and output layers with sigmoid transfer function in hidden layer, and linear function in output layer. Fig.1 illustrates the architecture of this type of model. Before the implementation of this model in forecasting the future electrical load, some important different tasks must be carried out such as: selection of input / output variables, preprocessing and removing the outliers points from the collected data, data normalizing, and training algorithm. Before going to training technique, the erroneous data points collected of the electrical loads are removed by using the moving average method. The use of original historical data as input to the network may cause a convergence problems, so normalizing all input/output data set were transferred in to values between [-1, +1] by using "Premnmx", and "postmnmx" MATLAB functions [9].

D. Training of The ANN model

The ANN model is required to go through training phase before it is actually being applied in load forecasting. The goal of training process is to adjust the weights and biases of the network and minimize the error between the output of the network and the desired output. The BP algorithm is widely employed in supervised MLP feed forward neural network models. The basic BP algorithm is a gradient descent algorithm. which adjusts the network weights and biases along the steepest descent direction of the error function decreases most rapidly. Training is iterative process, which continue until an acceptable level of error will be gained.

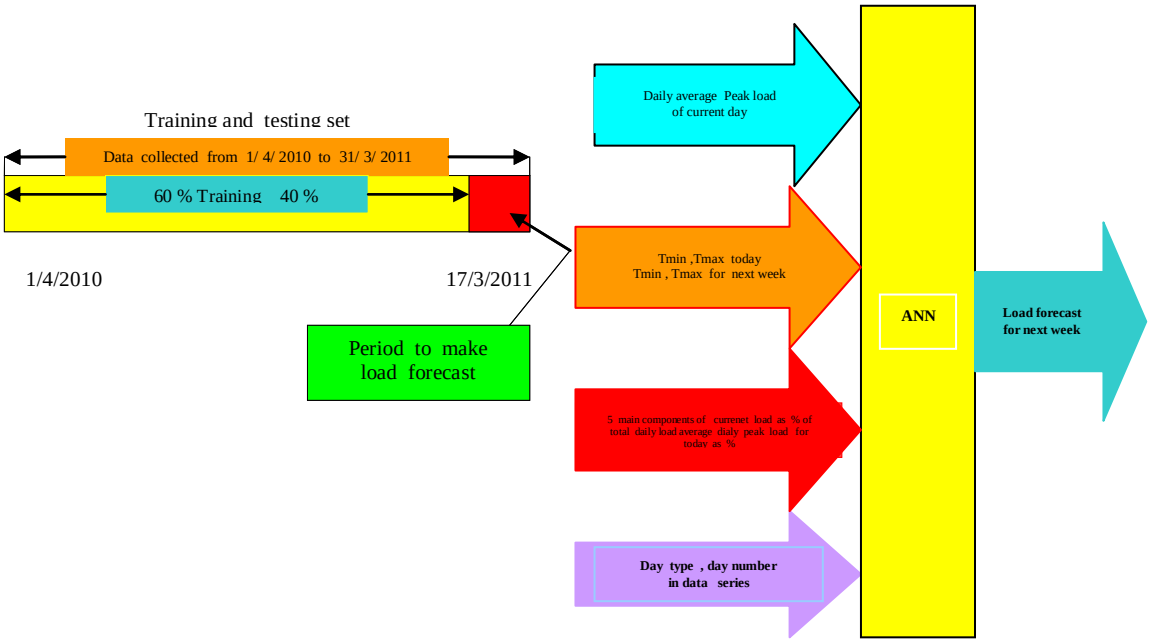

Fig. (5): Schematic of input and output vectors of the neural network with training and validation set.

The historical data collected of the weather conditions (maximum, and minimum temperature), daily peak load of electricity for a period from (1 April 2010 to 17 March 2011) which are 351 data points are used in training and testing of the model. This data set is split into two groups:

- 60 % of the data set are used for training (selected randomly).
- and the other 40 % of the data set (which are unseen by the model) are used for validation of the model as shown in Fig. 5.

The proposed network was trained using different number of neurons in hidden layer, different types of transfer functions in the hidden and output layers, and different training algorithms such as (*TRAINLM, TRAINGDM, TRAINOSS,*….etc). The training goal was set to 10^{-3}, and performance of the network was evaluated, finally suitable and acceptable results was obtained. In this work, the following performance measure functions were employed : mean square error (MSE), and mean absolute percentage error (MAPE %) to evaluate the accuracy of the proposed ANN model . These functions are given in the following equations:

$$\text{MSE}=\frac{1}{N}\sum_{1}^{N}(Xi-Yi)^{2} \qquad (1)$$

$$\text{MAPE}= \frac{1}{N}\sum_{1}^{N}\frac{(Xi-Yi)}{Xi}\times 100 \qquad (2)$$

Where :-

Xi : is the actual load., Yi : is the forecasted load., N : is the data points , for i= 1,2,….N.

IV. Results And Discussion

The proposed MLP network model was trained and tested by MATLAB software version 7.0 . The process of training is started with a network having 3 neurons in its hidden layer, and repeated by increasing the neurons up to 5 neurons at which the best performance are achieved. The output of the network was found to be close to the actual values of the electric load. The optimal structure for the model with minimum prediction error, correlation coefficient (R) between the actual and predicted values for the training and testing phases are listed in Table II. Fig.6 shows the behavior of the optimal MLP neural network model with actual and predicted values of electrical loads during the testing phase.

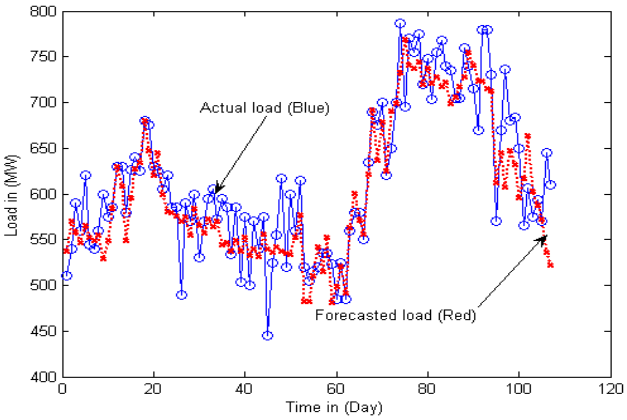

Fig. (6): Results of testing the proposed ANN model

Forecasting of the average daily peak load of one week ahead starting at 18 March 2011, has been carried out for the residential sector. The input data of previous week which are (total daily load, maximum and minimum temperature, day type, day indicator, and the 5 main components as a percentage, with daily maximum and minimum temperature of the next week), all these data presents to the MLP neural network model proposed. The results obtained for the forecasted load for one week ahead are summarized in Table III, and illustrated in Fig. 7 and Fig. 8 where the error as a percentage is calculated by:

$$\%\ \text{Error} = \frac{|Actual - Forecast|}{Actual} * 100\% \qquad (3)$$

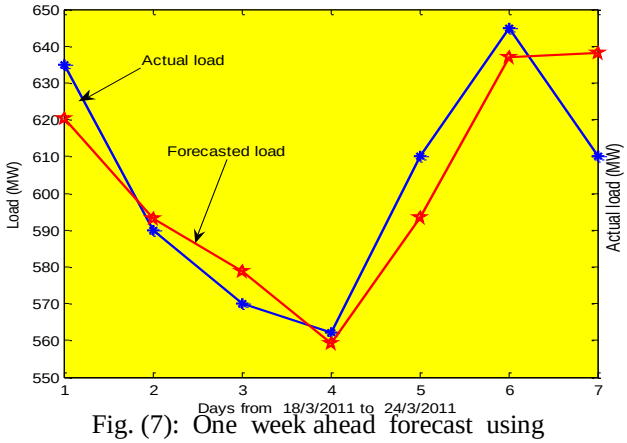

Fig. (7): One week ahead forecast using *MLP BP* neural network model (MAPE is 1.92 %).

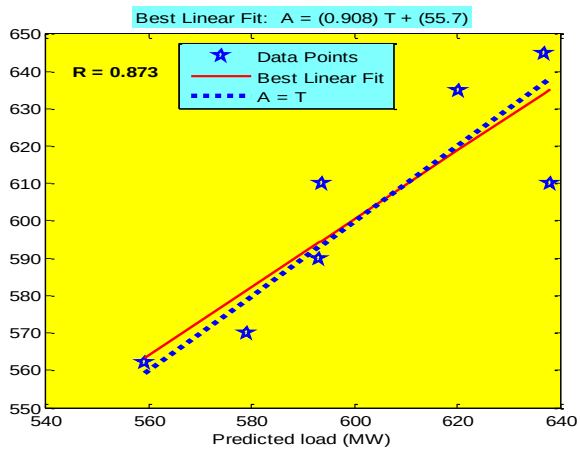

Fig. (8): Correlation coefficient of actual and predicted load.

Table II
Optimum 3 layers *MLP BP* ahead of average daily peak load model

Type and structure of *ANN*	3 layers *MLP BP* with structure (12-5-1)
Transfer functions	*Tan-sig ,Tan-sig*
Learning function	*Trainoss*
No. of epochs	1000
Learning rate	0.15
Momentum factor	0.40
Performance goal	0.001
MAPE% for training	3.39 %
MAPE% for testing	4.58 %
MSE for training	20.60
MSE for testing	28.10
Correlation coefficient (R)	0.938 for training 0.891 for testing

Table III
Forecasting for one week

Day	Date	Actual load MW	Forecasted load MW	Error %
Friday	18/3/2011	635	620	2.302
Sat.	19/3/2011	590	593	0.538
Sun.	20/3/2011	570	579	1.560
Mon..	21/3/2011	562	559	0.504
Tues.	22/3/2011	610	594	2.696
Wed.	23/3/2011	645	637	1.237
Thurs.	24/3/2011	610	638	4.608
Correlation coefficient (R)				0.873
MAPE %				1.921 %

V. Conclusions

An ANN model of type MLP of feed forward BP training algorithm was utilized in MTLF application for certain residential sector, which considered as one of the high consumption of electrical energy in Mosul city (Iraq). A new strategy concerning input variables that was used as the actual load of electricity at the feeder of the sector is disaggregate into 5 main components, then using these components in prediction of the future load. The weather temperature, day indicator, and historical load of one year data are collected by special efforts, and used in training and testing phases with good accuracy prediction.

Although the power system load for the selected sector is non stationary and unstable with high fluctuations during the study period as shown in Fig. 2 which reflects the actual behavior of load system, but a good design ANN forecasting model was presented with acceptable accuracy of 3.39 % MAPE in training phase and 4.58 % MAPE in testing phase. The model proposed was used in forecasting the daily average peak load for one week ahead with 1.921 % MAPE. The proposed model is ease in design and implementation along with flexibility and possibility of future improvements in the forecasted results. *MATLAB* software version 7 was used as modeling and forecasting engine.

With some advance techniques such as wavelet transform along with this ANN model, the work may be better and more accurate results can be achieved.

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تحجيم امثل لمنظومة طاقة متجددة هجينة لتغذية الأحمال السكنية في العراق

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الخلاصة

تستخدم الطاقات المتجددة في تزويد الأحمال الكهربائية جزئيا أو كليا. تظهر التطبيقات في دول مختلفة أفضلية استخدام منظومة قدرة هجينة لتحقيق هذا الهدف. تمثل الأحمال الكهربائية السكنية احد اكبر مكونات الحمل الكهربائي في منظومة القدرة الكهربائية العراقية. يمكن تزويد جزء من الأحمال المنزلية باستغلال الطاقات المتجددة. يدرس البحث إمكانية تغذية أحمال سكنية في مدينة الموصل – شمال العراق باستخدام منظومة طاقة متجددة هجينة ودراسة نسب مكونات المنظومة الهجينة لحالات مختلفة. استخدم برنامج HOMER في إيجاد الحل الأمثل للمنظومة المقترحة لقيم أحمال كهربائية وأسعار طاقة متعددة وحالات تشغيل متعددة.

Optimal Sizing of Hybrid Renewable Power System To Supply Iraqi Residential Loads

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Abstract

Renewable energy is used to supply electrical loads totally or partly. The Applications of utilizing renewable energies shown that a hybrid renewable system gives optimal solution. The residential load is one of the largest components of the electrical load in the Iraqi power system. Renewable energies can be used to supply a part of the residential loads in Mosul city-north of Iraq. A hybrid renewable power system is used to supply this residential loads. The optimal percentage of this hybrid renewable power system is fond using *Hybrid Optimization Model for Electric Renewables* (HOMER) software for different load, price and operating cases.

Keywords; Grid connecting loads; hybrid Renewable power system; HOMER; Residential load.

NPC: net present cost
IC: initial capital
W.T. : wind turbine
P.V. : photovoltaic

1. المقدمة :

يزداد الطلب على الطاقة الكهربائية نتيجة التطور الصناعي المتسارع والنمو السكاني ... الخ خلال العقود الماضية [1]. تسبب محطات توليد الطاقة الكهربائية التي تستثمر مصادر الطاقة التقليدية نسبة كبيرة من التلوث البيئي لذا يتسارع استثمار مصادر الطاقة المتجددة في أنظمة توليد القدرة الكهربائية [2] من اجل تقليل استهلاك الوقود التقليدي الملوث للبيئة وتقليل تكاليفه أيضا [3].

تعتبر تكنولوجيا استثمار الطاقات المتجددة هي تكنولوجيا المستقبل[4]. يتزايد معدل استثمار الطاقات المتجددة في الولايات المتحدة والاتحاد الأوربي، وكذلك في البلدان النامية وخصوصا في الصين والهند والبرازيل حيث أصبحت ألان الطاقات المتجددة تشارك في جزء مهم في توليد الطاقة الكهربائية في العالم[2].

يتم استخدام محطات الطاقة المتجددة اما لتزويد مناطق محددة معزولة بالطاقة بشكل مستقل أو بالمشاركة مع نظام مترابط للقدرة الكهربائية لتوفير جزء من الطلب الكلي للطاقة [4]. يتوقع وصول حصة مصادر الطاقة المتجددة إلى 50% من الطاقة الكلية المستخدمة خلال عقدين من الزمن [5].

يعمل الباحثون والمهندسون على وضع خطط ملائمة لتعزيز الكفاءة الاقتصادية لمحطات الطاقة المتجددة وذلك باستخدام منظومة طاقة متجددة هجينة (hybrid Renewable energy system) لتغذية الأحمال الكهربائية والتي تستثمر أكثر من مصدر للطاقات المتجددة في نفس الوقت وكذلك إمكانية تخزين الطاقة المتولدة بطريقة مناسبة لاستخدامها في حالات النقص بالطاقة ، أو عن طريق ربط نظام الطاقة الهجين بطريقة متزامنة مع الشبكة الرئيسية للقدرة الكهربائية من اجل استيراد النقص بالطاقة منها وكذلك تصدير الفائض بالطاقة إليها فتنخفض بذلك محصلة الكلفة الكلية مما يؤدي إلى زيادة كفاءة المنظومة الهجينة بشكل ملحوظ [6]. *تتكون أنظمة الطاقة الهجينة من اثنين أو أكثر من أجهزة تحويل الطاقة بالإضافة* إلى أجهزة التخزين أو نوعين أو أكثر من الوقود لنفس الجهاز[7] [8].

يتناول هذا البحث دراسة لمنظومة هجينة مثلى لتغذية أحمال كهربائية سكنية في مدينة الموصل شمال العراق. يتفاوت الاستهلاك الكهربائي للأحمال السكنية موضع الدراسة. كذلك تتناول الدراسة تسعيرات متغيرة للطاقة المشتراة من منظومة الطاقة، وحالات تشغيل متعددة. استخدم برنامج HOMER في إيجاد الحل الأمثل للمنظومة المقترحة.

يتطلب برنامج HOMER إدخال مجموعة من البيانات الضرورية أهمها:

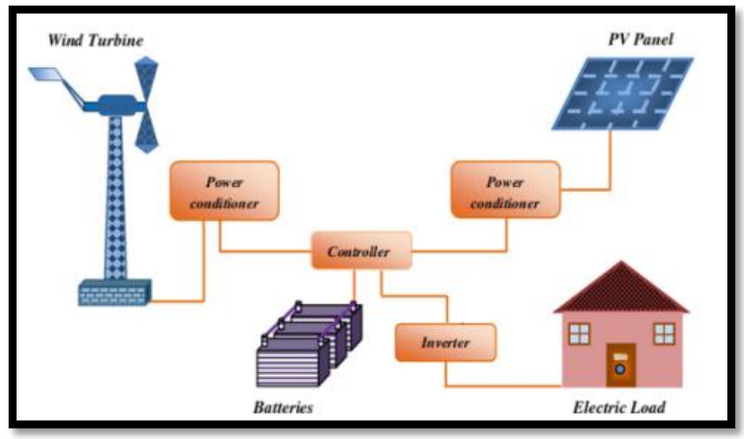
- مقننات الأحمال الكهربائية
- المقننات والأسعار والأعمار الافتراضية لوحدات توليد الطاقة المستخدمة في منظومة التوليد والوحدات الداعمة لها
- قيم العوامل الجوية المؤثرة والتي تشمل المعدلات الشهرية لشدة الإشعاع الشمسي ودرجات الحرارة وعدد ساعات النهار وسرع الرياح
- إحداثي خط الطول والعرض للمنطقة المدروسة
- كذلك يحتاج البرنامج إلى بيانات الشبكة الكهربائية (في حالة تحليل المنظومات الهجينة المتصلة بالشبكة) المتمثلة بسعة البيع والشراء للطاقة الكهربائية وأسعارها.

2. النظام الهجين المقترح

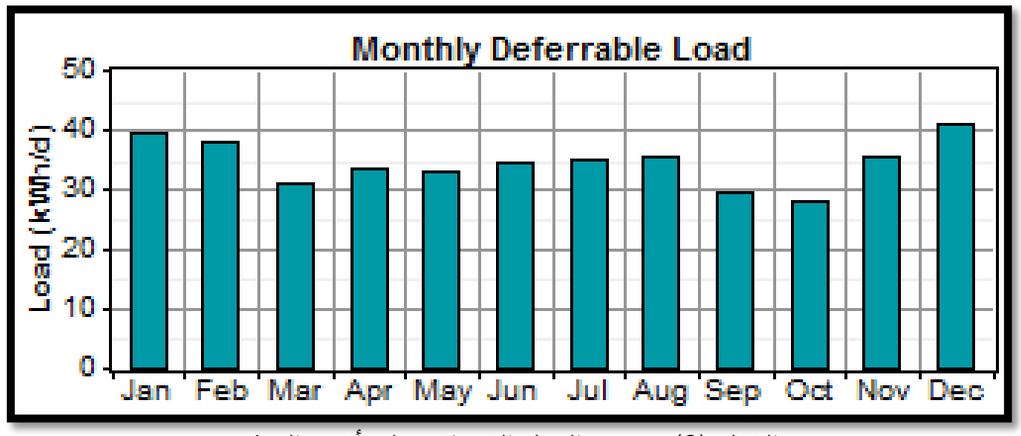
يتكون النظام الهجين المقترح من وحدات كهروضوئية وتوربينات رياح مع بطاريات ومحولات قدرة الكترونية تعمل على تغذية الحمل الكهربائي بالاتصال مع الشبكة الكهربائية (on–grid) كما موضح بالشكل(1). العمر الافتراضي للمشروع المقترح 25 سنة. برنامج هومر سيعمل على محاكاة هذا النظام وايجاد التكوين الأمثل له .

1.2 معلومات الحمل الكهربائي

تم الحصول على معطيات الأحمال المنزلية لعدد من الوحدات السكنية تقع في مدينة الموصل – شمال العراق بإحداثي خط طول 43.1558 شرقا وخط عرض 36.381 شمالا ، (المنطقة الزمنية GMT+3)[9] ضمن عقد استشاري مع المديرية العامة لتوزيع الكهرباء الشمالية. الحمل الكهربائي السكني هو عبارة عن الحمل الشهري المتزايد خلال سنة. تم تحليل منظومة الطاقات المتجددة الهجينة لثلاث مستويات من الأحمال المنزلية ، حمل سكني منخفض ومتوسط ومرتفع [10,11]. الحمل المنخفض ذو ذروة مقدارها (8.5KW) ومعدل سنوي (34.5 KWh/day) ، الحمل المتوسط ذو ذروة مقدارها (17KW) ومعدل سنوي (69 KWh/day) ، وأخيرا الحمل المرتفع ذو ذروة مقدارها (34 KW) ومعدل سنوي (138 KWh/day) .يوضح الشكل(2) توزيع الحمل الكهربائي للمنزل الأول (منخفض الاستهلاك) على أشهر السنة. يتشابه توزيع الحمل الكهربائي على أشهر السنة للمنزلين الثاني (متوسط الاستهلاك) والثالث (عالي الاستهلاك).



الشكل (1) : نظام الطاقة المتجددة المقترح.



الشكل (2) : توزيع الحمل الكهربائي على أشهر السنة.

2.2 معلومات الوحدات الكهروضوئية

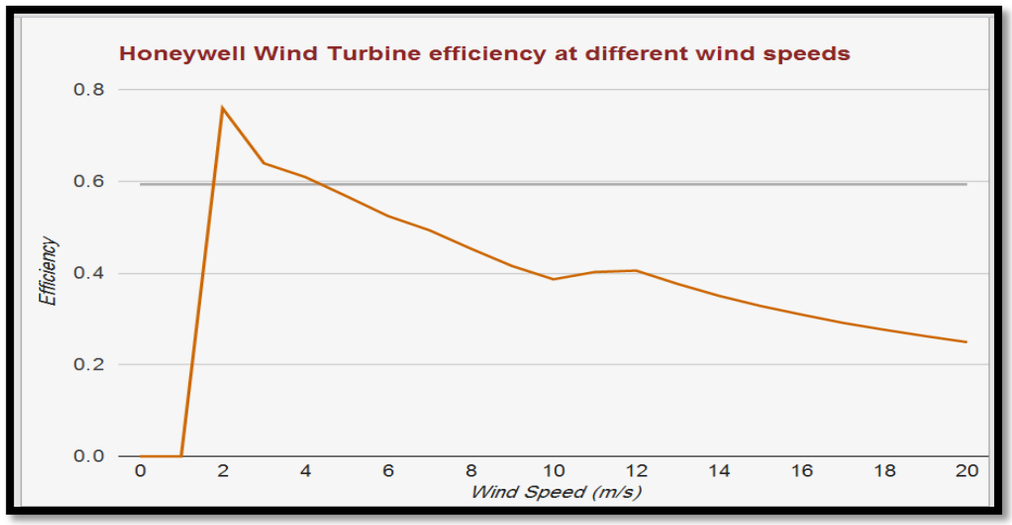
يمكن توليد طاقة كهربائية بقيمة(180w) للوحة الكهروضوئية الواحدة المستخدمة في هذا النظام ، وبكلفة مقدارها 162 $ لكل لوح وبتكلفة تبديل 120 $ (الكلفة متضمنة لنظام تعقب الشمس) ، وبمساحة (1.27 م^2) للوح الواحد. المنظومة الكهروضوئية الكلية مزودة بنظام تعقب للشمس ثنائي المحور يحمل جميع الألواح على شكل مصفوفة كما مبين بالشكل(3)[12] . العمر الافتراضي للمجموعة الكهروضوئية 25 سنة والانعكاس الارضي 35% تقريبا وعامل ديريتك 90 % . كذلك تم اخذ تأثير درجات الحرارة بالاعتبار.

الشكل (3) : مصفوفة الالواح الكهروضوئية

3.2 معلومات توربين الرياح

يبلغ المتوسط الشهري لسرعة الرياح الموسمية في منطقة الموصل على ارتفاع 10 أمتار (4.6 متر/ثانية). هذه السرعة منخفضة غير قادرة على تدوير التوربينات المزودة بصندوق تروس بشكل جيد. لذا استوجب استخدام توربين خاص صغير الحجم يتناسب مع سرعة الرياح في المنطقة. يمتاز تربين HONEYWELL WT6500 المبين بالشكل (4) بخلوه من صندوق تروس. يبدأ هذا التوربين بالدوران عند سرعة (0.2 متر/ثا) ويبدأ بالتوليد عند سرعة (0.9 متر/ثا) وحتى سرعة (17.9 متر/ثا). القدرة المقننة له (1500 واط) عند سرعة رياح (13.9 متر/ثا). يبين الشكل رقم (5) الكفاءة مع سرعة الرياح. يتبين من الشكل ان كفاءة التوربين 60 % تقريبا عند متوسط سرعة الرياح. تبلغ كلفة التوربين الواحد ($ 4500) وكلفة التبديل ($ 4000)، والمساحة التي يشغلها التوربين (2.5 م^2)[13،14]. تم اضافة التوربين اعلاه الى قائمة مصادر الطاقات المتجددة لبرنامج المحاكاة المستخدم في البحث.

الشكل (4) : توربين HONEYWELL WT6500



الشكل (5) : منحني الكفاءة لتوربين HONEYWELL WT6500

4.2 معلومات البطاريات

تم استخدام البطاريات لضمان الاستمرارية في تجهيز القدرة للحمل في حالات العجز بالتوليد. نوع البطاريات المستخدمة هو (Surrette 4-KS-25P) [15] بمقننات (7.9KWh & 4V & 1900Ah). كلفة رأس المال للبطارية الواحدة ($ 1236) وكلفة التبديل لها ($ 1000) . توضع البطاريات بشكل سلسلة من 38 بطارية لتجهز فولتية مقدارها (150 V) او اكثر لتتوافق مع إدخال محول القدرة الاليكتروني .

5.2 معلومات المحول الكهربائي

تم استخدام محول القدرة الاليكتروني للحفاظ على انسياب الطاقة بين المركبات المتناوبة (A.C.) والمستمرة (D.C.) حجم محول القدرة المستخدم في هذا النظام (2KW) بكفاءة (97%) .تكلفة رأس المال ($ 400) وتكلفة التبديل ($ 350) [16] .

6.2 معلومات الشبكة الكهربائية

سعة البيع للشبكة (12 KW) ، سعة الشراء (4.4 KW) حسب عقد مع مديرية توزيع كهرباء الشمال بشرط ضمان الاستمرارية في تجهيز القدرة. لذا فان قيمة الشراء القصوى من الشبكة (105.6 KWh/day). تم اختيار عدة أسعار لكلفة الشراء بدءا" من($/KWh 0.01) إلى ($/KWh 0.05) لتشمل اغلب الاحتمالات الممكنة لتغير سعر طاقة الشبكة. إن معظم الدول التي تُستعمل فيها تقنيات بيع الطاقة إلى الشبكة الحكومية من وحدات التوليد المحلي تعرض كلفة شراء للطاقة تقارب ضعف ما تبيع للمستهلك [17]، لذا اعتُمد في هذه الدراسة سعر بيع الطاقة للشبكة هو ضعف سعر الشراء منها.

3. المحاكاة العددية :

الهدف من هذه الدراسة هو إيجاد أفضل تكوين لمنظومة الطاقة الهجينة وذلك عن طريق تحديد الحجم المثالي واستراتيجية العمل المثالية للمنظومة[18]. تم استخدام برنامج الـ HOMER لنمذجة ومحاكاة عدد كبير من التوليفات

الممكنة لمكونات المنظومة الهجينة. وضع برنامج HOMER المختبر الوطني للطاقة المتجددة في الولايات المتحدة (NREL) للمساعدة على تصميم انظمة الطاقة الصغيرة وتسهيل المقارنة بين تقنيات توليد الطاقة عبر تشكيلة واسعة من التوليفات[19]. يعمل HOMER على محاكاة جميع الحلول الممكنة للنظام الهجين ثم يعرض قائمة من التكوينات المختلفة للنظام (توليفات مختلفة لمكونات النظام) مرتبة بالتدريج من الأقل إلى الأعلى في التكلفة الإجمالية الصافية (TNPC) .التكوين الأمثل لمنظومة الطاقة المتجددة الهجينة يكون هو الأقل تكلفة من بين التكوينات الأخرى [18].

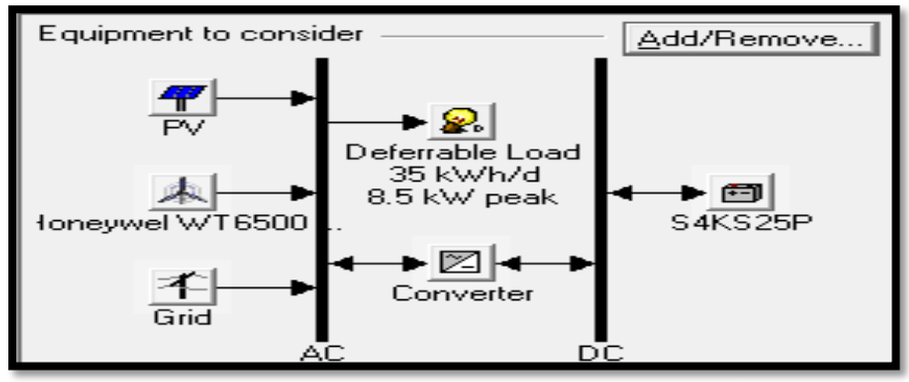
يستطيع HOMER نمذجة أنظمة الطاقة الصغيرة بنوعيها المتصلة بالشبكة (grid-connected) والمعزولة عن الشبكة (off-grid) والتي قد تحتوي على أي مزيج من الوحدات الكهروضوئية وتوربينات الرياح والطاقة المائية الصغيرة، وطاقة الكتلة الحيوية ومولدات ذات محرك احتراق داخلي ومحولات قدرة الكترونية وبطاريات وخلايا الوقود والتخزين بالهدروجين [20].

تبين في بحث سابق دراسة امكانية تغذية احمال سكنية تقع في مدينة الموصل باستخدام الطاقات المتجددة أن فصل الاحمال المنزلية عن الشبكة (off-grid) يؤدي إلى منظومة طاقة عالية الكلفة وتشغل مساحة كبيرة تفوق المساحة المتوفرة في الوحدات السكنية مما يؤدي إلى كونها غير عملية وغير اقتصادية في التطبيق لذلك تم في هذا البحث ربط الاحمال الكهربائية المنزلية إلى الشبكة الكهربائية للحصول على منظومة هجينية اقتصادية قابلة للتطبيق من ناحية مساحة وكلفة ومكونات منظومة الطاقة الهجينية .المعدلات الشهرية للإشعاع الشمسي وسرعة الرياح ودرجات الحرارة المستخدمة في البحث السابق هي نفسها المستخدمة في البحث الحالي[21].

تم دراسة حالتين للأحمال المنزلية المربوطة إلى الشبكة. يمكن في الحالة الاولى تزويد الحمل السكني بالطاقة الكهربائية عبر الشبكة الكهربائية ومنظومة الطاقة المتجددة. تتمتع الحالة الثانية بإمكانية بيع فائض الطاقة المتولدة في المنظومة الهجينية إلى الشبكة الكهربائية.

1.3 الحالة الأولى

تكون منظومة الطاقة المتجددة لها الإمكانية فقط على شراء الطاقة من الشبكة الكهربائية المتصلة بها. يوضح الشكل رقم (6) المكونات الاولية للمنظومة الهجينية المقترحة للمسكن الاول (حمل كهربائي قليل). تتشابه المنظومات المقترحة لحالتي المساكن متوسطة الاستهلاك والمساكن عالية الاستهلاك.



الشكل رقم (6) : المكونات الاولية للمنظومة الهجينية المقترحة للمساكن قليلة الاستهلاك.

1.1.3 نتائج الحالة الاولى :

أظهرت نتائج المحاكاة بان التكوينات المثلى لمنظومة الطاقة المتجددة لنموذج المساكن الثلاثة بعد استخدام برنامج HOMER الاتي:

يظهر الجدول (1) والجدول (2) نتائج تطبيق برنامج HOMER لنموذج المساكن قليلة الاستهلاك ومتوسطة الاستهلاك على التوالي. يتضح من الجدولين ان المكونات النهائية لهذه الحالة هي الشبكة الكهربائية ووحدات كهروضوئية فقط. تم الاستغناء عن البطاريات ومحولات القدرة الاليكترونية بسبب وجود الشبكة الكهربائية التي تزود الحمل بالطاقة في فترة انعدام التوليد الكهروضوئي. كذلك فان غياب توربينات الرياح في نتائج الامثلية لهذه المنظومة توافق نتائج اخرى في دراسات مشابهة لنفس المنطقة الجغرافية[22] . كذلك تقتصر المنظومة عند اسعار الطاقة الكهربائية القليلة (1 و 2 سنت) على التغذية من الشبكة الكهربائية. تظهر الحاجة إلى الالواح الكهروضوئية عند 3 سنت. تزداد مساحة الالواح الكهروضوئية مع زيادة تسعيرة الطاقة الكهربائية. كذلك تزداد قدرة الوحدات الكهروضوئية للاستهلاك المتوسط عن الاستهلاك المنخفض .. المعادلة (1) استخدمت لحساب مساحة الألواح الكهروضوئية المبينة في الجداول.

$$PV\_array\ area\ = \frac{pv\_array\ size}{pv\_panel\ size}\ (pv\_panel\ area\ m^2) \qquad (1)$$

الجدول (1) : نتائج تطبيق برنامج HOMER لنموذج المساكن قليلة الاستهلاك.

System N.O.	Price (cent)	Grid (kw)	P.V. (kw)	W.T. (unit)	Battery (unit)	Conv. (kw)	I.C. ($)	N.P.C ($)	Area (m^2)
1	1	4.4	0	0	0	0	0	2887	0
2	2	4.4	0	0	0	0	0	4496	0
3	3	4.4	1.4	0	0	0	1260	6009	9.8
4	4	4.4	1.7	0	0	0	1530	7128	11.9
5	5	4.4	1.8	0	0	0	1620	8202	12.7

الجدول (2) : نتائج تطبيق برنامج HOMER لنموذج المساكن متوسطة الاستهلاك.

System N.O.	Price (cent)	Grid (kw)	P.V. (kw)	W.T. (unit)	Battery (unit)	Conv. (kw)	I.C. ($)	N.P.C ($)	Area (m^2)
1	1	4.4	0	0	0	0	0	4496	0
2	2	4.4	0	0	0	0	0	7714	0
3	3	4.4	2.8	0	0	0	2520	10740	19.7
4	4	4.4	3.3	0	0	0	2970	12974	23.2
5	5	4.4	3.6	0	0	0	3240	15126	25.4

يتضح من الجدول (3) ان المكونات النهائية لهذه الحالة هي الشبكة الكهربائية وألواح كهروضوئية. كذلك تظهر الحاجة إلى الالواح الكهروضوئية لجميع تسعيرات الطاقة. بالإضافة للحاجة إلى توربين رياح عند التسعيرات (1,2,3) سنت. يؤدي تحديد امكانية الشراء من المنظومة ب 20 أمبير (4.4 كيلوواط) إلى قدرة عالية لمنظومة الطاقة الهجينية وكذلك كلفة عالية بسبب الحاجة إلى منظومات خزن للطاقة (محولات قدرة الكترونية وبطاريات) لضمان الاستمرارية في تجهيز الحمل الكهربائي لعدم كفاية الشبكة على تزويد الحمل بالطاقة عند فترة انعدام التوليد الكهروضوئي الأمر الذي يجعل هذه الحالة مشابه في جزء منها لحالة الأحمال المفصولة عن الشبكة.

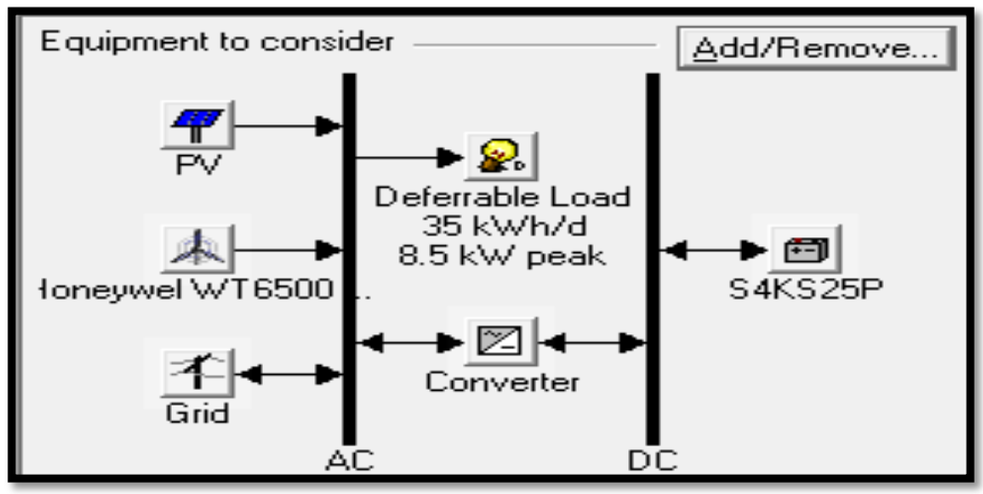
الجدول (3) : نتائج تطبيق برنامج HOMER لنموذج المساكن عالية الاستهلاك.

System N.O.	Price (cent)	Grid (kw)	P.V. (kw)	W.T. (unit)	Battery (unit)	Conv. (kw)	I.C. ($)	N.P.C ($)	Area (m^2)
1	1	4.4	20.7	3	38	17.5	78098	108552	146
2	2	4.4	20.7	3	38	17.5	78098	111356	146
3	3	4.4	20.7	3	38	17.5	78098	114160	146
4	4	4.4	29	0	38	17	76468	109100	204
5	5	4.4	27	0	38	20.5	75368	110872	190

تظهر نتائج نماذج الاحمال الثلاثة ملائمة قيمة تحديد الشراء من الشبكة ب 20 امبير لحالتي الاحمال قليلة ومتوسطة الاستهلاك والحاجة إلى زيادة التغذية من الشبكة لحالة الاحمال عالية الاستهلاك.

2.3 الحالة الثانية:

تكون منظومة الطاقة المتجددة لها الإمكانية على شراء وبيع الطاقة من والى الشبكة الكهربائية المتصلة بها كما مبين بالشكل (7). يوضح الشكل حالة لنموذج الاحمال السكنية قليلة الاستهلاك. تتشابه المكونات الاولية لمنظومة الطاقة المتجددة في كل مستهلك مع اختلاف الحمل الكهربائي فقط.



الشكل (7) : منظومة الطاقة المتجددة لنموذج المساكن قليلة الاستهلاك.

1.2.3 نتائج الحالة الثانية :

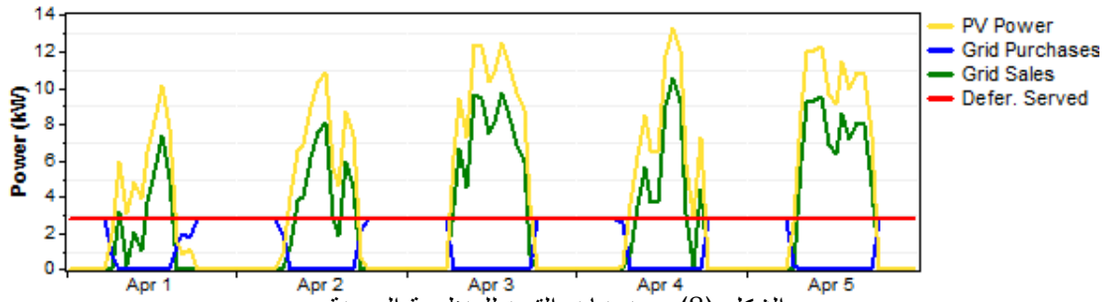
أظهرت نتائج المحاكاة بان التكوينات المثلى لمنظومة الطاقة المتجددة للأحمال الثلاثة هي كما مبين بالجداول ادناه:

الجدول (4) : نتائج تطبيق برنامج HOMER لنموذج المساكن قليلة الاستهلاك.

System N.O.	Price (cent)	Grid (kw)	P.V. (kw)	W.T. (unit)	Battery (unit)	Conv. (kw)	I.C. ($)	N.P.C ($)	Area (m^2)
1	1	4.4	0	0	0	0	0	2887	0
2	2	4.4	0	0	0	0	0	4496	0
3	3	4.4	7.92	0	0	0	7128	4	55.8
4	4	4.4	6.23	0	0	0	5607	2	44
5	5	4.4	5.47	0	0	0	4923	13	38.5

يتضح من الجدول رقم 4 ورقم 5 عدم الحاجة إلى إضافة أي من معدات الطاقة المتجددة لحالة التسعيرات القليلة (1و2 سنت). تظهر الحاجة إلى الطاقة المتجددة متمثلة بالوحدات الكهروضوئية عند سعر 3 سنت. تقل الطاقة اللازمة مع زيادة التسعيرة. كذلك لا يوجد تمثيل لتوربينات الرياح أو بطاريات الخزن في المنظومة المتجددة لغلاء أسعارها وإمكانية تبادل الطاقة (بيع وشراء) مع الشبكة الكهربائية.

تكون الكلفة الكلية (NPC) عند استخدام الوحدات الكهروضوئية قريبة من الصفر، وذلك بسبب بيع فائض الطاقة الكهربائية إلى الشبكة. يوضح الشكل (8) فترة خمسة أيام من شهر نيسان لحالة الاستهلاك المتوسط عند 3 سنت، التوليد الكهروضوئي باللون الأصفر، الحمل باللون الأحمر، فائض الطاقة المباع للشبكة باللون الأخضر، الطاقة المشترى من الشبكة باللون الأزرق. إن الربح العائد من بيع الطاقة للفائضة للشبكة جعل الكلفة الكلية لهذين الحملين تنخفض إلى ما يقرب من الصفر، وهو جزء من هدف استخدام الطاقات المتجددة.



الشكل (8) : منحنيات القدرة للمنظومة الهجينة

الجدول (5) : نتائج تطبيق برنامج HOMER لنموذج المساكن متوسطة الاستهلاك.

System N.O.	Price (cent)	Grid (kw)	P.V. (kw)	W.T. (unit)	Battery (unit)	Conv. (kw)	I.C. ($)	N.P.C ($)	Area (m^2)
1	1	4.4	0	0	0	0	0	4496	0
2	2	4.4	0	0	0	0	0	7714	0
3	3	4.4	14.66	0	0	0	13194	0	143
4	4	4.4	11.68	0	0	0	10512	9	82.4
5	5	4.4	10.38	0	0	0	9342	18	73

الجدول (6) : نتائج تطبيق برنامج HOMER لنموذج المساكن عالية الاستهلاك.

System N.O.	Price (cent)	Grid (kw)	P.V. (kw)	W.T. (unit)	Battery (unit)	Conv. (kw)	I.C. ($)	N.P.C ($)	Area (m^2)
1	1	4.4	27.1	0	38	20	75358	91713	191
2	2	4.4	27.9	0	38	19	75875	86640	196.8
3	3	4.4	28.7	0	38	17.5	76298	81111	202
4	4	4.4	29.9	0	38	16	77078	75368	211
5	5	4.4	30.5	0	38	15.5	77518	69477	215

يتضح من الجدول رقم 6 الحاجة الى اضافة الألواح الكهروضوئية بكافة التسعيرات لان مقدار الحمل يفوق القيمة القصوى للطاقة التي تزودها الشبكة ، كذلك لا يوجد تمثيل لتوربينات الرياح في منظومة الطاقة المتجددة المثلى. تظهر الحاجة الى بطاريات الخزن كذلك زيادة طاقة الألواح الكهروضوئية مع زيادة التسعيرة. يرجع السبب في ذلك الى تحديد كمية الطاقة التي يمكن شرائها وبيعها للشبكة.

يتضح من الجدول (6) عدم وجود تمثيل لتوربينات الرياح في منظومة ، تظهر الحاجة إلى إضافة الألواح الكهروضوئية واجهزة خزن الطاقة عند كافة التسعيرات لان الطاقة التي يمكن شراءها من الشبكة محددة وهي اقل من مقدار الحمل في هذه الحالة ، كذلك تزداد طاقة الألواح الكهروضوئية مع زيادة التسعيرة من اجل تحقيق مكسب اكبر من بيع الطاقة للشبكة.

ان مساحة وحجم الوحدات الكهروضوئية في هذه الحالة كما مبين بالجدول (6) كبيرة جدا ولا تتناسب مع المساحة المنزلية ، كذلك الكلفة الكلية مرتفعة أيضا لذا يجب زيادة قيمة الطاقة التي يمكن شراءها من الشبكة من اجل تقليل الحاجة للوحدات الكهروضوئية.

4. الاستنتاجات

تم في هذا البحث دراسة امكانية تغذية الاحمال السكنية بمنظومة طاقة متجددة هجينية وباستخدام برنامج HOMER ، لحالات أحمال وتسعيرات طاقة وحالات ربط متعددة. أظهرت نتائج المحاكاة بان الاستثمار الامثل للطاقات المتجددة يكون باستخدام الوحدات الكهروضوئية فقط من غير الاعتماد على طاقة الرياح حيث جرت محاولة لاستثمار طاقة الرياح واستُعملَ تربين صغير الحجم يتناسب مع سرع الرياح في المنطقة ولكن تبين عدم جدوى توربينات الرياح في توليد الطاقة الكهربائية في مدينة الموصل بسبب ارتفاع كلفتها من جهة وانخفاض توليدها من جهة أخرى لانخفاض سرعة الرياح الموسمية في المدينة بصورة عامة . كذلك اظهرت النتائج افضلية تغذية الاحمال السكنية بوجود الشبكة الكهربائية لما لها من فوائد فنية واقتصادية، وان تكون هناك امكانية لتبادل الطاقة (بيع وشراء) مع الشبكة ، حيث ينخفض الحمل الكهربائي عن الشبكة فضلا عن تزويدها بالطاقة في ذروة الحمل الكهربائي النهاري بالإضافة الى تخفيض فاتورة الطاقة الكهربائية للمستهلك. يمكن للاحتمال السكنية القليلة والمتوسطة ان تكتفي بمحدد تيار قليل (20) امبير (4.4 KW) من الشبكة. اما في حالة الاحمال السكنية العالية فيجب زيادة محدد التيار الى قيمة اعلى تتحدد بقيمة الحمل الكهربائي للوصول الى نفس الفوائد السابقة .

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New PI and PID Tuning Rules Using Simple Analytical Procedure

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Abstract

This paper aims to present tuning rules for PI and PID controllers used to control First-Order-Plus-Dead-Time and Second-Order-Plus-Dead-Time systems. The approach used to obtain these rules is a simple analytical method, based on choosing desired transfer function for the closed loop system. Then, by using straightforward procedure, a set of equations is obtained. Solving these equations leads to the desired rules. Simulation study shows clearly that the obtained sets of tuning rules give very good performance. The simulation study of the designed systems includes also comparison of the obtained results with other tuning rules. The comparison show the superiority of the proposed method.

Keywords: Analytical method, First-Order-Plus-Dead-Time (FOPDT), Second-Order-Plus-Dead-Time (SOPDT), straightforward procedure

قواعد تنغيم جديدة لمتحكمات PI و PID باستخدام طريقة تحليلية مبسطة

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الخلاصة

يهدف هذا البحث الى ايجاد معادلات تنغيم لمتحكمات تناسب–تكامل (PI) وتناسب–تكامل–تفاضل (PID) المستخدمة في السيطرة على المنظومات التي يمكن تمثيلها من خلال النماذج من نوع الدرجة الاولى ذات الزمن الميت والدرجة الثانية ذات الزمن الميت. الطريقة المستخدمة في هذا البحث تعتمد على اختيار دالة انتقالية منتخبة للمنظومة المغلقة ثم اتباع خوارزمية مباشرة للحصول على مجموعة من المعادلات التي يمكن حلها انياً للحصول على معادلات التنغيم المطلوبة. المحاكاة تعيين بشكل واضح ان معادلات التنغيم المستحصلة من خلال هذه الطريقة تعطي نتائج اداء ممتازة. كذلك تمت مقارنة النتائج المستحصلة مع نتائج مستحصلة من خلال استخدام معادلات تنغيم لطرق معروفة، فتبين ان الطريقة المقترحة اعطت نتائج افضل.

1. Introduction

It is generally believed that PID controllers are the most popular controllers used in process control. Because of their remarkable effectiveness and simplicity of implementation, these controllers are extensively used in industrial applications [1]. Because of their ability to control most of the processes, well understood control action and ease of implementation, more than 90% of existing control loops involve PID controllers [2].

The aim of PID control design is to determine PID parameters (*Kc*,*Ti* and *Td*) to meet a given set of closed loop system performance requirements.

Surveys on the current status in process control [3,4] confirms that the PID control still predominates and that "it is quite reasonable to predict that PID control will continue to be used in the future" [5].

The great difficulty of PID controllers is how to adjust the three parameters with changing in operating conditions or environmental parameters [6,7].

There are two major groups of methods to obtain PID controller parameters. The first are the methods which try to find a set of algebraic equations for these parameters. These equations 'which are often called as tuning rules' relate the controller parameters with the controlled process model parameters. The second group of methods are these which depend on the optimization techniques[8-10]. In spite of that these methods give good results, but there is a big drawback involved with them. It is the complexity of obtaining the numerical values for the controller parameters, where these parameters are given as a solution of the optimization problem. While obtaining these parameters using tuning rules is just a process of applying numerical values to a set of algebraic equations. This reason addresses popularity of tuning rules.

Since the 1942 'where the first tuning rules had been presented [11]', many methods have been proposed for designing these controllers, but every method has brought about some disadvantages or limitations [1]. As a result, the design of PID controllers still remains a challenge for researchers and engineers.

Many researchers had provided PID controller tuning rules for various process models and different performance criteria. Most of thePID controllers tuning methods reported in literature are based on the approximate plant models, and these are First-Order-Plus-Dead-Time (FOPDT) and Second-Order-Plus-Dead-Time systems (SOPDT) models derived from the step response of the plant.

2. The Process Models to be Controlled

Due to very important rules for FOPDT and SOPDT in process modeling, we have selected these models to be the two models to obtain the tuning rules for.

The T.F. for FOPDT is:-

$$p(s) = \frac{Kpe^{-ls}}{Ts+1} \quad (1)$$

Where Kp is the process gain, T is the time constant and l the dead time.

The T.F. used for SOPDT is:-

$$p(s) = \frac{Kpe^{-ls}}{t_2 s^2 + t_1 s + 1} \quad (2)$$

3. Problem Formulation

Let us consider the classical closed loop system shown below:-

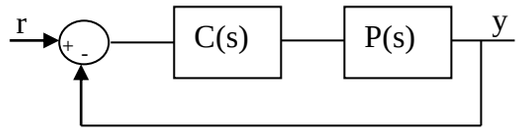


Fig. (1): A classical feedback system

Where, P is the process to be controlled and C is the controller which is assumed here to be PI or PID controller, r is the set point and y the output.
From Fig.1, the transfer function for the overall system is:-

$$T.F. = \frac{Y(s)}{R(s)} = \frac{C(s)P(s)}{1+C(s)P(s)} \quad (3)$$

In this paper, the tuning process for PI or PID controllers based on choosing desired T.F., then solving the equations obtained from equating this function with the actual T.F. function (Eq.3) of the system.

4. Design Procedure

4.1 PI Controller for FOPDT

For FOPDT, we have chosen PI controller with the following T.F. :-

$$\boldsymbol{C(s) = Kc(1 + \frac{1}{T_i s})} \quad (4)$$

To tune the PI controller, our procedure begin with choosing selected or desired T.F., then equating this equation with the actual T.F. of the closed loop system.
Let T_{ds} be the desired T.F., then:-

$$T_{ds} = \frac{C(s)P(s)}{1+C(s).P(s)} \quad (5)$$

Where, C(s) is as described by Eq.4 and P(s) is the controlled plant model which described by Eq.1.
T_{ds} should be chosen to give the desired performance beside being suitable for Eq.4 in terms of order and the nonlinear delay term.
From Eq.5:-

$$C(s) = \frac{T_{ds}(s)}{P(s)-T_{ds}(s).P(s)} \quad (6)$$

Selecting T_{ds} as:-

$$T_{ds}(s) = \frac{(s+k^2)e^{-ls}}{(tcTs+k)^2} \quad (7)$$

Where k and tc are the designed parameters.

Substituting (1), (4) and (7) into (6) and manipulating the resulting equation, the following equation can be obtained:-

$$kckpT_i[(T^2tc^2 + l) - TT_i]s^3 + [kckp(T^2tc^2 + l) - T_i - k^2TT_{i+}kckpT_i(lk^2 + 2Ttck - 1)]s^2 + [kckp(lk^2 + 2Ttck - 1) - k^2T_i]s = 0 \quad (8)$$

In the previous derivation we have used the Maclaurin approximation for time delay;

$$e^{-ls} = (1 - ls)$$

And,

$$e^{-2ls} = (1 - 2ls)$$

Eq.8 gives three equations or constraints which should be satisfiedsimultaneously to satisfy Eq.7. These equations are:-

$$\left.\begin{aligned} &kckpT_i[(T^2tc^2 + l) - TT_i] = 0 \\ &[kckp(T^2tc^2 + l) - T_i - k^2TT_{i+}kckpT_i(lk^2 + 2Ttck - 1)]=0 \end{aligned}\right\} \quad (9)$$

$kckp(lk^2 + 2Ttck - 1) - k^2T_i = 0$

These equations contain the two parameters of PI controller kc and T_i besides the two design parameters tc and k.

Solving these three equations for kc, T_i and tc gives three valid sets of solutions, we selected the following set:-

$$kc = \frac{T}{kpT^2tc^2+kpl} \quad (10)$$

$$T_i = T \quad (11)$$

$$k = \frac{1}{Ttc} \quad (12)$$

In these equations, Eq.(10) and (11) represent the tuning rules for PI controller, while (12) represents the relationship between the desired T.F. parameters k and tc.

4.2 PID Controller for SOPDT

The model we try to tune PID controller for is described by Eq.2. The desired T.F. is selected as follow:-

$$T_{ds} = \frac{(s+k)e^{-ls}}{s^2+tct1t2s+k} \quad (13)$$

PID controller is used here instead of PI controller with the following T.F.:-

$$C(s) = Kc(1 + \frac{1}{T_is} + T_ds) \quad (14)$$

Substituting Eq.(2), (13) and (14) into (6) and manipulating the resulting equation, the following equation can be obtained:-

$$[kcT_dkpT_i\alpha - T_i]s^4 + [kckpT_i\alpha - t_2T_i - kT_i + kcT_dkpT_i\beta]s^3 + [kckp\alpha - t1T_i - kt2T_i + kckpT_i\beta]s^2 + [(kckp\beta - kt1T_i]s = 0 \quad (15)$$

Where,

$\beta = kl + t1t2tc - 1$

$\alpha = l + 1$

Eq.14 can be used to obtain four equalities which should be satisfied simultaneously to satisfy Eq.6, these equations are:-

$$\left.\begin{array}{l} kcT_dkpT_i\alpha - T_i = 0 \\ kckpT_i\alpha - t_2T_i - kT_i + kcT_dkpT_i\beta = 0 \\ kckp\alpha - t1T_i - kt2T_i + kckpT_i\beta = 0 \\ kckp\beta - kt1T_i = 0 \end{array}\right\} \quad (16)$$

We have solved Eqs.16 for kc, T_i, T_d and tc, the result is three valid sets of solutions, from which we have selected the following set:-

$$kc = \frac{kt1+\frac{1}{2}t2-\frac{1}{2}l\delta+\frac{1}{2}lt2-\frac{1}{2}\delta}{kpl^2+2kpl+kp} \quad (17)$$

$$T_i = \frac{l-kt1+k^2lt1+1+\frac{1}{2}k(2t1+t2+l\delta+lt2+\delta-2klt1)}{k+kl} \quad (18)$$

$$T_d = \frac{kt1+\frac{1}{2}t2+\frac{1}{2}lt2+\frac{1}{2}l\delta+klt1+\frac{1}{2}\delta}{l+kt2+k^2t1+k^2lt1+klt2+1} \quad (19)$$

$$tc = \frac{2t1+t2+l\delta-2klt1+lt2+\delta}{2t1^2t2} \quad (20)$$

Where,

$\delta = \sqrt{t2^2 - 4t1}$

Eqs.17 to 19 are the tuning rules for PID, while (20) represents the relationship between the design parameters which determine the behavior of desired T.F.. Then it can be said that the process of tuning has been transformed to just tuning of one parameter (tc) in term of other parameter (k) by one equation (Eq.20).

5. Simulation Study

In this section, the validity and performance of the obtained tuning rules is investigated by simulation, using randomly chosen process models. The simulation study for FOPDT includes comparison with other known tuning rules.

5.1 PI Controller for FOPDT

In order to investigate the performance of the obtained tuning rules, we have compared the results obtained using our tuning rules with results obtained using some other known tuning rules. These are the well-known Ziegler-Nichols method [11], Cohen-Coon method [12] and the optimal tuning rules proposed by Saeed-Mahdi Tavakoli [13]. We will refer to these methods by Z-N, C-C and S-M respectively. We have selected three FOPDT models for our simulation:-

$$P1 = \frac{2e^{-0.3s}}{0.5s + 1}$$

$$P2 = \frac{10e^{-0.6s}}{12s + 1}$$

$$P3 = \frac{5e^{-1.2s}}{23s + 1}$$

To find the controller parameters, we first select suitable value for tc, then applying Eqs.10 to 12 to find Kc, Ti and K. Table.1 shows these parameters for the three models selected for simulation study.

Figures 2 to 4 show the step responses for the three models for the four tuning rules.

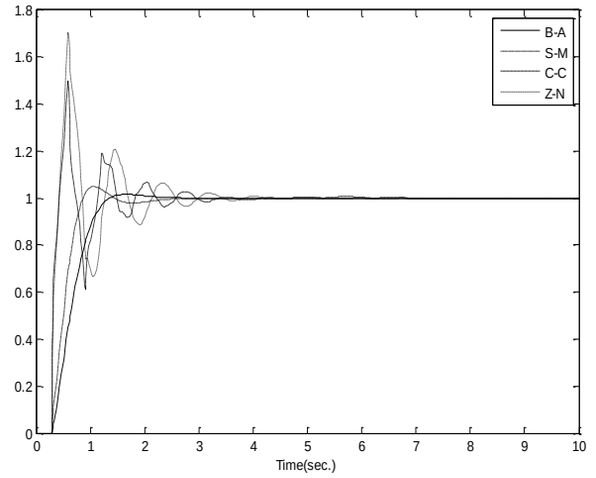
To compare between the responses obtained using the four tuning rules, we have selected the following performance measure:

- Rise time (tr):- the time required by the response to reach 80% of the final value for the first time.
- Maximum overshoot:- The maximum peak value of the response curve measured from unity.
- Settling time:- The time required by the response to reach 2% of the final value and staying within that limit.

Tables. 2 to 4 show the values of these parameters for the four tuning rules simulated for the three models P1, P2 and P3.

Table (1): The parameters of T_{ds} and PI controllers for the three FOPDT models .

	tc	Kc	Ti	K
P1	1.2	0.38	0.5	1.66
P2	0.07	0.9	12	1.19
P3	0.05	1.8	23	0.87



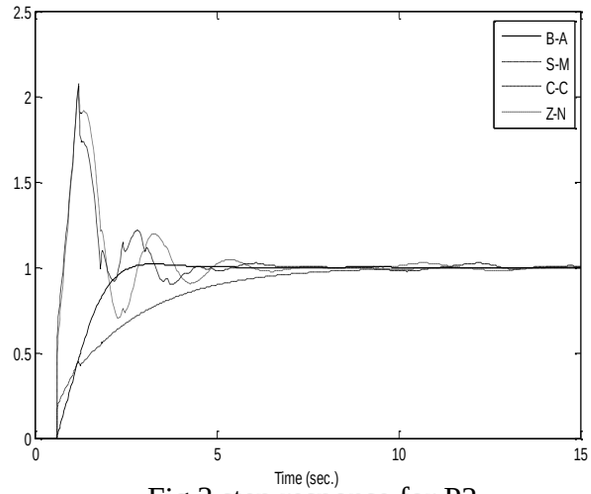


Fig.3 step response for P2.

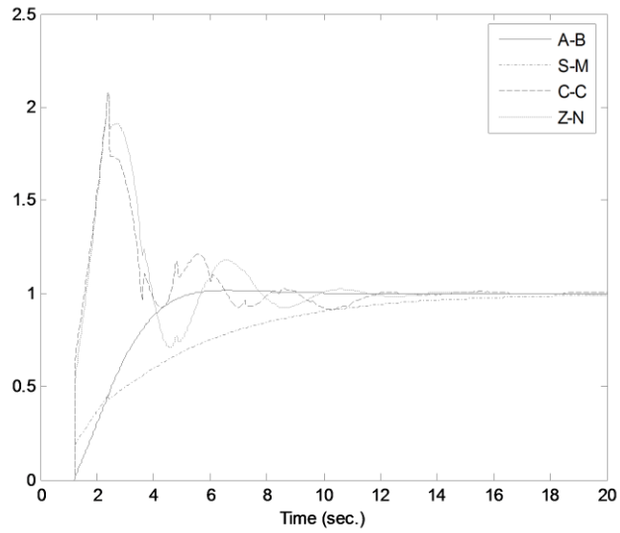


Fig. (4): Step response for P3.

Table (2): Performance measures values for P1 model.

	rt(s)	Overshoot	ts(s)
Z-N	0.3	0.85	3.3
C-C	0.36	0.44	3
S-M	0.67	0.07	1.8
The proposed rules	0.9	0	1.2

Table (3): Performance measures values for P1 model.

	rt(s)	Overshoot	ts(s)
Z-N	0.63	1.2	13
C-C	0.62	1.15	12
S-M	3.5	0	8
The proposed rules	1.77	0	2.2

Table (4): Performance measures values for P1 model.

	rt(s)	Overshoot	ts(s)
Z-N	1.4	2.2	11.5
C-C	1.43	2.5	12.3
S-M	7	0	15
The proposed rules	3.5	0	5

To investigate the robustness of the proposed tuning rules, we have simulated the model P2 for different values of process gain Kp. The controller parameters have been obtained using the nominal value of Kp (Kp=10), the system has been simulated using these this controller with Kp=6, 8, 10, 12and 14. Fig.5 shows the step responses of the system for these values of Kp.

Fig.5 shows clearly that the proposed tuning rules have good robustness for process gain variations.

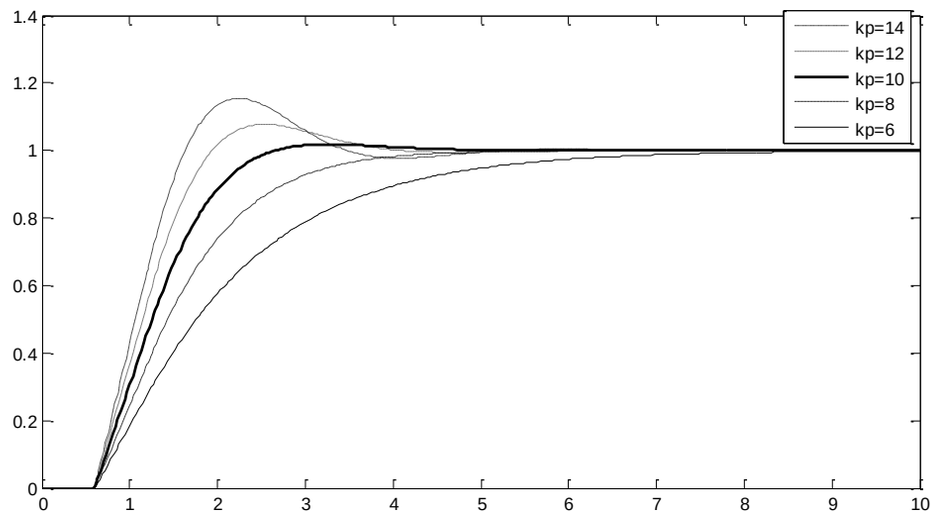


Fig. (5): Step responses for P2 with different values of Kp.

5.2 PI Controller for SOPDT

We have selected three SOPDT models for the simulation study:-

$$p1 = \frac{20e^{-0.5s}}{0.6s^2 + 2s + 1}$$

$$p2 = \frac{10e^{-0.8s}}{5s^2 + 12s + 1}$$

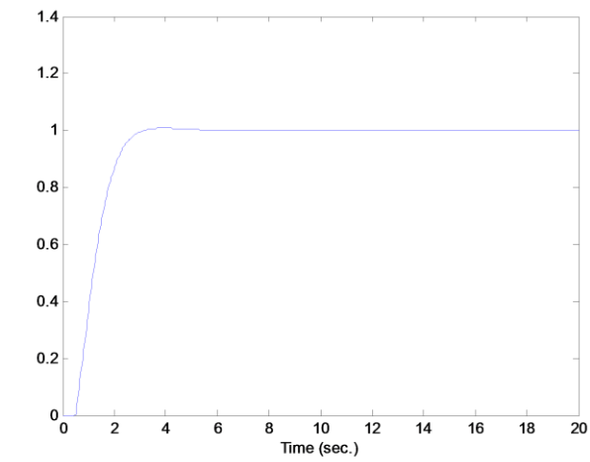
$$p3 = \frac{100e^{-1.1s}}{10s^2 + 50s + 1}$$

To find the controller parameters, suitable value for K has been chosen, then by applying Eqs.17 to20 the design parameters can be found. Table.2 shows these parameters for the three models.

Table (5): The parameters of T_{ds} and PID controllers for the three SOPDT models .

	K	Kc	Ti	Kd	tc
P1	3	0.07	1.96	0.3	3
P2	2.2	0.63	12	0.43	0.056
P3	4.2	0.2	50	0.24	0.014

Fig.6 to 8 show the step responses for the three models.



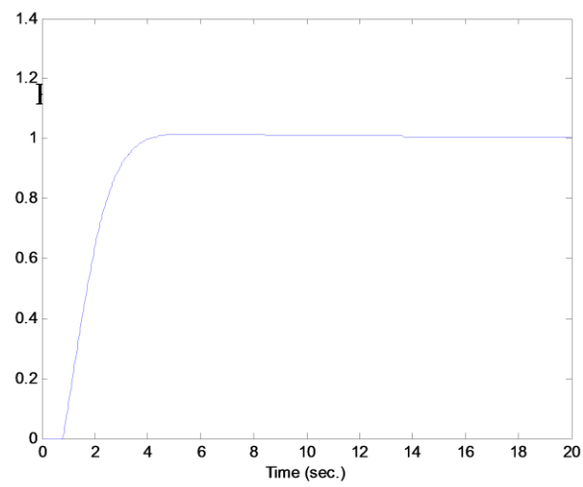


Fig. (7): Step response for P2.

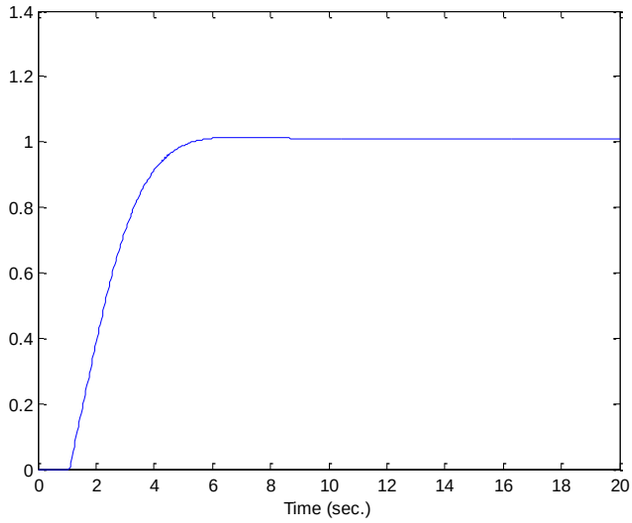


Fig. (8): Step response for P3.

For robustness study of the proposed tuning rules, P2 model have been simulated for different values of process gain Kp. The controller parameters have been obtained using the nominal value of Kp (Kp=10), the system has been simulated using this controller with Kp=6, 8, 10, 12and 14. Fig.9 shows the step responses of the system for these values of Kp.

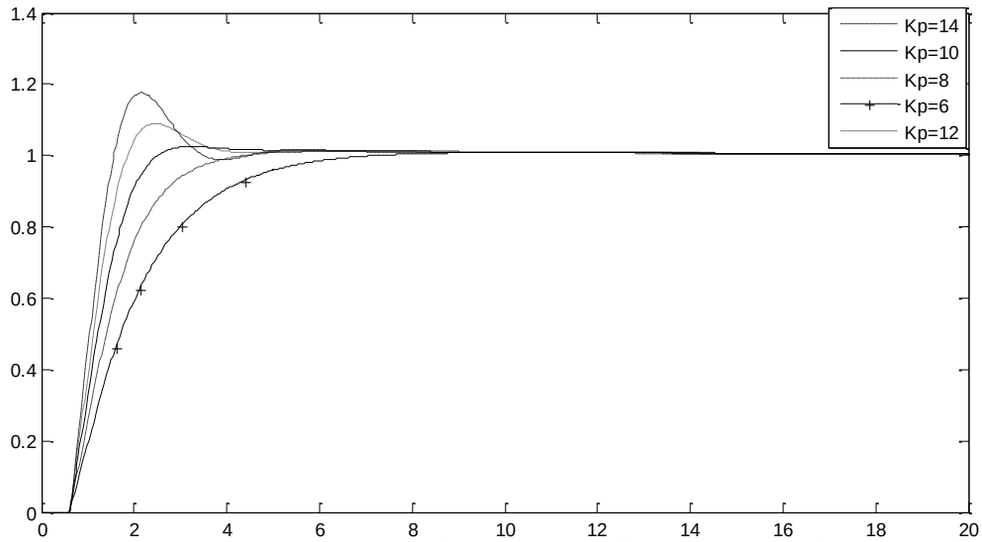


Fig. (9): Step responses for P2 with different values of Kp.

6. Conclusions

Simple and straightforward procedure has been used to obtain new tuning rules for PI and PID controllers. These tuning rules is dedicated for FOPDT and SOPDT models which are widely used to approximate high order processes. Extensive simulation study has been made to investigate the validity and features of the proposed tuning rules, also to compare these rules with other known tuning rules. From this simulation study the following can be concluded:-

1- The proposed tuning rules for both FOPDT and SOPDT are valid to apply for these models and give very good features in transient response and steady state.

2- By comparing the results obtained using controllers tuned by some known tuning rules with that obtained using the proposed rules, we can easily concluded that these give superior performance.
3- By varying the process gain for a specified FOPDT and SOPDT models controlled by controllers tuned by the proposed rules at a nominal value of the process gain, we found that the responses remain good even with large gain variations. This leads to the conclusion that the proposed tuning rules are robust.

Simulation study has showed that the obtained tuning rules are easy to apply and have fast and good response for step changes in set point.
Extending the design procedure for more general models is our suggestion for future works.

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Analysis of Seven Level Cascaded Multilevel DC-Link Inverter

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Abstract

Multilevel inverter is an effective and practical solution for increasing power demand and reducing harmonics of AC waveforms. This paper deals with modeling and simulation of seven level cascaded half-bridge Multilevel DC Link (MLDCL) single phase inverter. An MLDCL can be a diode-clamped phase leg, a capacitor-clamped phase leg, or cascaded half-bridge inverter structure. The MLDCL provides a DC voltage with the shape of a staircase approximating the rectified shape of a commanded sinusoidal wave to the bridge inverter, which in turn alternates the polarity to produce an AC voltage. As compared with the conventional types of multilevel inverters, the MLDCL inverters can significantly reduce the component count (power switches, clamping diodes, or flying capacitors) as the number of voltage levels increases to beyond five. An Optimized Harmonic Elimination Stepped Waveform (OHESW) technique is applied to determine the switching angles for the MLDCL multilevel inverters, which eliminates specified higher order harmonics while maintains the required fundamental voltage. The simulation of the inverter is carried out by ORCAD PSPICE.

Keywords: MLDCL, ORCAD PSPICE.

تحليل مغير فولتية ذو سبع مستويات من نوع MLDCL

أحمد محمد النائب
المعهد الفني / الحويجة / كركوك

الخلاصة

يعتبر عاكس الفولتية المتعدد المستويات الحل الفعال والعملي عند ازدياد الحاجة للقدرة الكهربائية الخالية تقريبا من التوافقيات المتناوبة والغير مرغوب فيها. في هذا البحث تم نمذجة و تمثيل عاكس فولتية احادي الطور ذي سبع مستويات من نوع MLDCL. هذا النوع من العاكسات من الممكن ان يكون من نوع diode-clamped, capacitor-clamped او من النوع التعاقبي. ان عاكس الفولتية (MLDCL) يوفر فولتية مستمرة على شكل مدرجات يمكن ان تتحول الى شكل جيبي تقريبا من خلال عاكس فولتية قنطري. مقارنة مع عاكس الفولتية متعدد المستويات التقليدي فأن هذا النوع من العاكسات يحتاج لعدد اقل من المكونات (مفاتيح القدرة الكهربائية، عدد الدايودات،أو عدد المتسعات اللازمة) كلما زاد عدد مستويات الفولتية عن خمسة. استخدمت تقنية OHESW لإيجاد زوايا القدح اللازمة لعاكس الفولتية، حيث ان هذه التقنية تحذف توافقيات محددة عالية المرتبة وتحافظ على التوافقية الاساسية المطلوبة في الفولتية. تمت النمذجة من خلال برنامج ORCAD PSPICE.

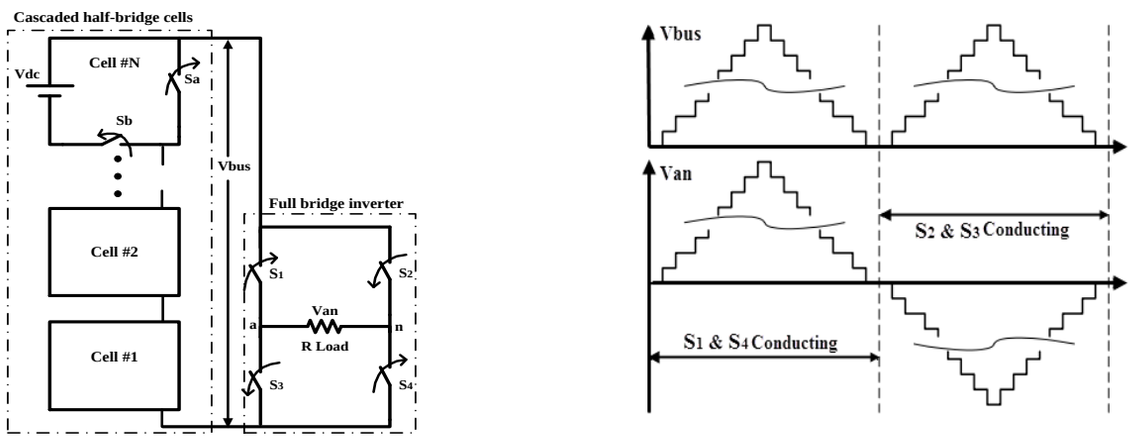
I. Introduction

Multilevel inverters are mainly devised for high power applications, due to higher voltage operating capability, lower dv/dt and more sinusoidal outputs. Multilevel inverter synthesizes a desired voltage from several levels of DC voltages with low harmonics [1]. As the number of levels increases, the harmonic distortion of the output wave decreases. But the disadvantage is increasing in number of power switches and their gate drivers. To overcome this disadvantage a multilevel DC link inverter (MLDCL) is propose by many authors [2, 3, and 4]. This comparatively reduces the number of switches, and their gate drivers, compared with the existing multilevel inverter counterparts. For a given number of voltage levels (M), the required number of active switches is $2 * (M - 1)$ for the existing multilevel inverters, but it is $M + 3$ for the MLDCL inverters [2, 3]. The MLDCL's can be cascaded half-bridge, a diode-clamped phase leg, or capacitor-clamped phase leg inverter. Compared to diode-clamped & capacitor-clamped type MLDCL inverters cascaded MLDCL inverter requires least number of components to achieve the same number of voltage levels [2]. The cascaded half-bridge based MLDCL topology is simulated in this paper.

II. MLDCL Inverter

1- Cascaded Half-Bridge Based MLDCL Inverter:

The cascaded MLDCL inverter consists of N half-bridge cells and one full bridge cell as shown in Fig. 1 (a). Each half-bridge cell has two switches S_a and S_b. They operate in a toggle fashion. The cell source is bypassed when S_a is on and S_b is off. The cell source adds to the DC link voltage when S_a is off and S_b is on. Fig. 1 (b) illustrates the DC bus and load voltage waveforms. The half-bridge cell produces DC bus voltage (V_{bus}) waveform with the staircase shape with (N) steps and the full bridge inverter consists of four switches S_1-S_4 cell alternates the voltage polarity to produce an AC output voltage of staircase waveform (V_{an}) with ($2N + 1$) levels [2,3, and 4].



(a) **(b)**

Fig. (1): (a): (2N+1) level cascaded half-bridge MLDCL inverter,
(b): DC bus and load voltage waveforms

2- Diode-Clamped Phase-Leg Based MLDCL Inverter:

Similarly to the half-bridge cell based MLDCL inverter, the diode-clamped MLDCL provides a DC bus voltage (V_{bus}), with the shape of a staircase to the full bridge inverter, which in turn alternates the voltage polarity to produce an AC voltage of the staircase shape (V_{an}) [4]. As an example, Fig. 2 shows a 7-level MLDCL inverter based on a diode-clamped phase leg.

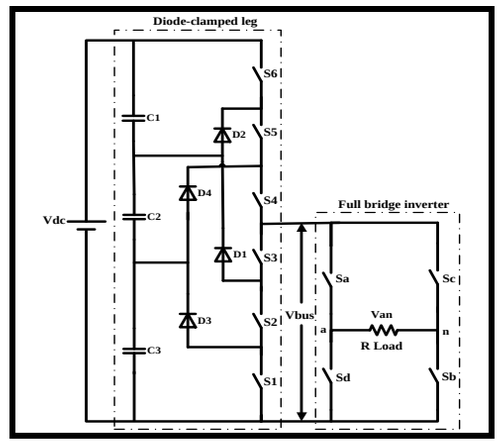


Fig. (2): Seven level diode-capacitor based MLDCL inverter

3- Capacitor-Clamped Phase-Leg Based MLDCL Inverter:

The capacitor-clamped phase leg can also be used to provide a multilevel DC bus voltage with the shape of a staircase to the full bridge inverter. As an example, Fig. 3 shows a 7-level MLDCL inverter based on a diode-clamped phase leg [5].

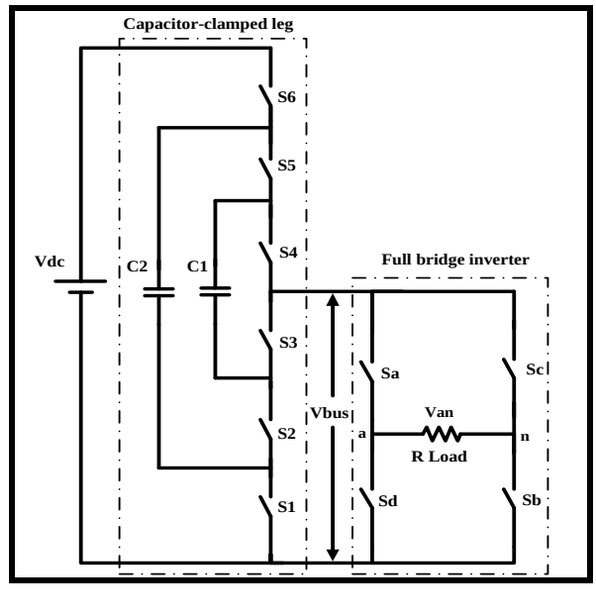


Fig. (3): Seven level capacitor-clamped based MLDCL inverter

III. Comparison of the Traditional Multilevel Inverter and New MLDCL Inverter

The proposed MLDCL inverters can significantly reduce the component count as the number of voltage levels increases. Table 1 summarizes the required number of switches, clamping diodes, and capacitors of the three proposed inverters compared with the existing count part, for a given number of output voltage level, M[5].

Table (1): Component Count Comparison

	Cascaded		Diode Clamped		Flying Capacitor	
	traditional	new	traditional	new	traditional	new
Switches	$2*(M-1)$	$M+3$	$2*(M-1)$	$M+3$	$2*(M-1)$	$M+3$
Clamping Diodes	--	--	$2*(M-2)$	$M+3$	--	--
Clamping Capacitors	--	--	--	--	$M-2$	$(M-3)/2$

Fig. 4 plots a chart for comparison of the required number of switches between the proposed MLDCL inverter and the cascaded H-bridge count part. As the number of voltage levels, M, grows, the number of active switches increases according to $M+3$ for the MLDCL inverter, compared to $2*(M-1)$ for the traditional cascaded H-bridge multilevel inverters, which is also true for the diode-clamped and flying capacitor multilevel inverters.

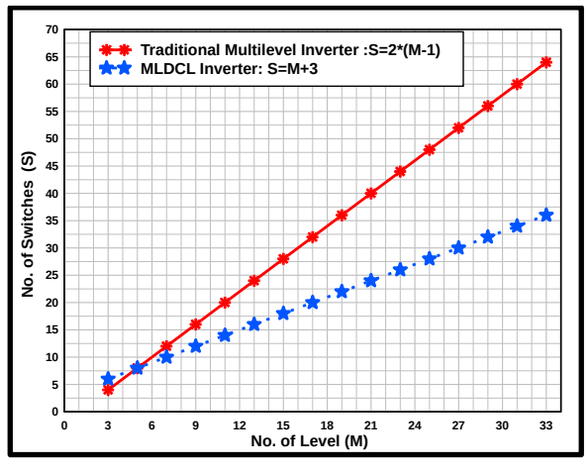


Fig. (4) : Comparison of required number of switches

Fig. 5 plots a chart for comparison of the required number of diode-clamped between the proposed diode-clamped based MLDCL inverter and the traditional diode-clamped count part. As the number of voltage levels, M, grows, the number of diode-clamped increases according to $M-3$ for the MLDCL inverter, compared to $2*(M-2)$ for the traditional diode-clamped inverters. Similarly, Fig. 6 plots a chart for comparison of the required number of capacitor-clamped between the proposed capacitor-clamped based MLDCL inverter and the traditional capacitor-clamped count part.

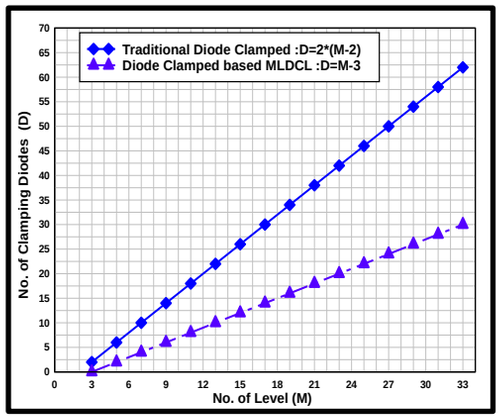


Fig. (5): Comparison of required number of diode- clamped

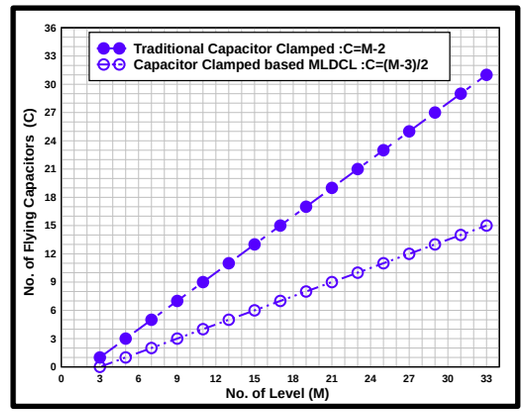


Fig. (6): Comparison of required number of capacitor-clamped

IV. Switching Angles Calculation

A Selective Harmonic Elimination (SHE) technique is combined with Optimized Harmonic Stepped Waveform (OHSW) method to decrease output harmonic contents and filter size with less complexity and switching losses. Harmonic elimination technique is an offline method in which switching angles are used to control the fundamental component and to eliminate low order harmonic contents [1, 6].

Fourier series expansion is used to find out switching angles and eliminate desired harmonic contents. Then the Fourier series expansion of the (staircase) output voltage waveform of the multilevel inverter as shown in Fig.7 [1, 6] is

$$V_0(\omega t) = \frac{4V_{dc}}{\pi}\sum_{n=1,2,3,\dots}^{\infty}\frac{1}{n}\left(\cos n\theta 1 + \cos n\theta 2 + cosn\theta 3\right)\sin n\omega t\ ) \quad (1)$$

Where $\theta 1, \theta 2,$ and$\theta 3$ are the optimized switching angles of the seven level inverter, which must satisfy the following condition: $0 < \theta 1 < \theta 2 < \theta 3 < \frac{\pi}{2}$.

From equation (1), the harmonic components in the waveform can be described as follows:

- The amplitude of DC component is equals zero.
- The amplitude of all even harmonics is equal zero, since it is symmetric.
- The amplitude of all odd harmonic components (H) including fundamental one, are given by:

$$H(n) = \frac{4V_{dc}}{\pi}\sum_{n=1,3,5,\dots}^{\infty}\frac{1}{n}\left(\cos n\theta 1 + \cos n\theta 2 + cosn\theta 3\right) \quad (2)$$

If one wants to control the peak value of the output voltage to be V_1 and eliminate the most significant low frequency harmonic components (3^{rd} and 5^{th} order harmonics), the resulting harmonic equations will be:

$$\frac{4V_{dc}}{\pi}\left[\cos\theta 1 + \cos\theta 2 + cos\theta 3\right] = V_1 \quad (3)$$

$$\cos 3\theta 1 + \cos 3\theta 2 + cos3\theta 3 = 0 \quad (4)$$

$$\cos 5\theta 1 + \cos 5\theta 2 + cos5\theta 3 = 0 \quad (5)$$

One can also rewrite equation (3) as:

$$\cos\theta 1 + \cos\theta 2 + cos\theta 3 = \frac{\pi V_1}{4V_{dc}} \quad (6)$$

The set of nonlinear transcendental equations (4, 5, and6) can be solved based on OHESW technique to obtain the optimized switching angles: ($\theta 1$=8.76655^0, $\theta 2$=28.6886^0, and $\theta 3$=54.9395^0).

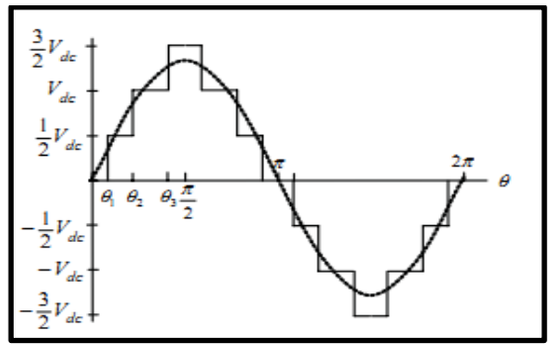


Fig. (7): Output voltage waveform of the seven level cascaded MLDCL

V. Simulation Circuit

To verify the proposed schemes, a simulation model for a seven level cascaded MLDCL inverter is implemented. The model of the inverter is simulated by using ORCAD PSPICE simulation tool as shown in Fig.8. The simulation is performed with 100V DC source.

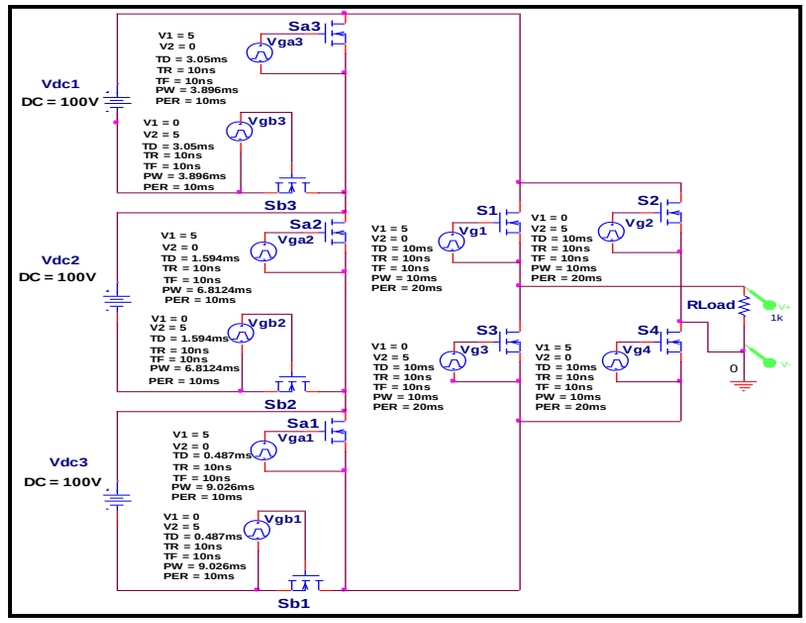


Fig. (8): Simulation circuit of seven level cascaded MLDCL inverter

Seven modes of switching sequence are given in Table 2 to produce DC bus voltage V_{bus} with the shape of staircase with (N=3) steps, where N is the number of cell sources that is given to the full-bridge inverter.

Table (2): Seven modes of switching sequence to produce DC bus voltage

Mode (1) $V_{bus} = 0$	Mode (2) $V_{bus} = V_{DC}$	Mode (3) $V_{bus} = 2V_{DC}$	Mode (4) $V_{bus} = 3V_{DC}$	Mode (5) $V_{bus} = 2V_{DC}$	Mode (6) $V_{bus} = V_{DC}$	Mode (7) $V_{bus} = 0$
S_{b1}:OFF S_{b2}: OFF S_{b3}: OFF	S_{b1}:ON S_{b2}: OFF S_{b3}: OFF	S_{b1}: ON S_{b2}: ON S_{b3}: OFF	S_{b1}: ON S_{b2}: ON S_{b3}: ON	S_{b1}: ON S_{b2}: ON S_{b3}: OFF	S_{b1}: ON S_{b2}: OFF S_{b3}: OFF	S_{b1}: OFF S_{b2}: OFF S_{b3}: OFF

Based on the various modes given in Table 1 switching signals are generated for the switches in the half-bridge cells. The switching pulses (V_{gb1}, V_{gb2}, and V_{gb3}) are shown in Fig. 9.

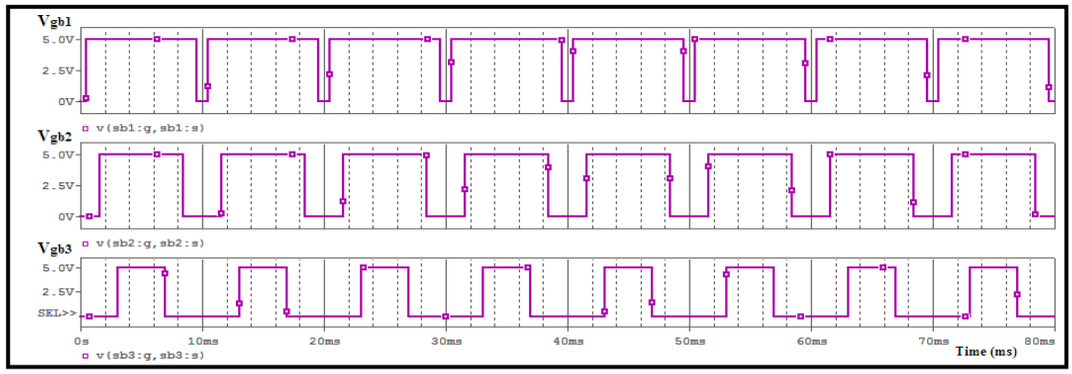


Fig. (9): Switching pulses (V_{gb1}, V_{gb2}, and V_{gb3})

By giving the switching pulses shown in Fig. 9 to the switches in three half-bridge cells, the MLDCL voltage source produces DC bus voltage (V_{bus}) with the shape of staircase as shown in the Fig. 10. The switches in the three cells will operate at frequency twice of the fundamental frequency of the output voltage.

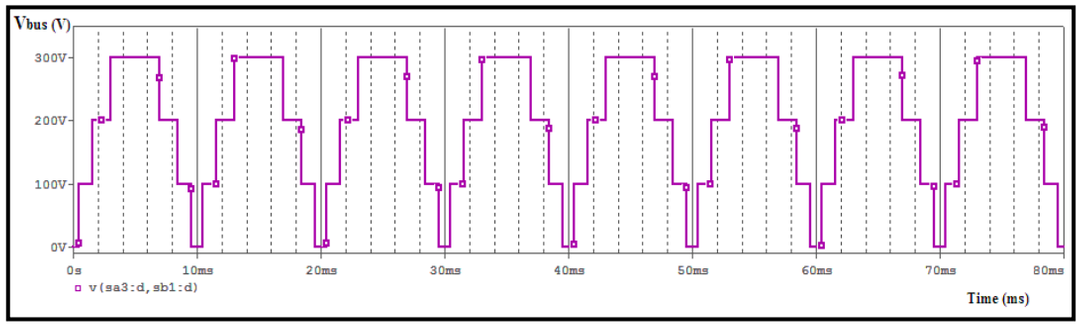


Fig. (10): DC bus voltage (V_{bus}) of seven level cascaded MLDCL inverter

The switches S1-S4 always work in pairs, such that S1&S4 are triggered for positive half cycle and S2&S3 are trigger to produce negative half cycle to produce a voltage alternate at the desired fundamental frequency. The switching sequence for producing multilevel AC output voltage is shown in Fig. 11. The output voltage waveform of the seven level cascaded MLDCL inverter is shown in Fig. 12. While the spectra of the output voltage waveform is shown in Fig. 13.

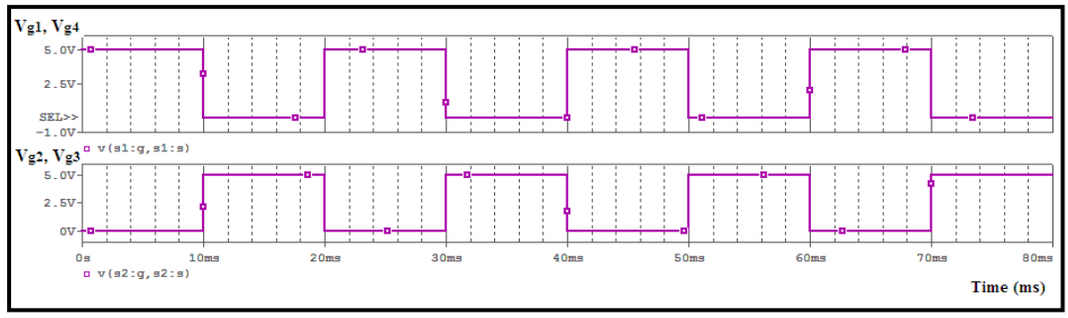


Fig. (11): Switching pulses (V_{g1}, andV_{g2}) of the full bridge inverter

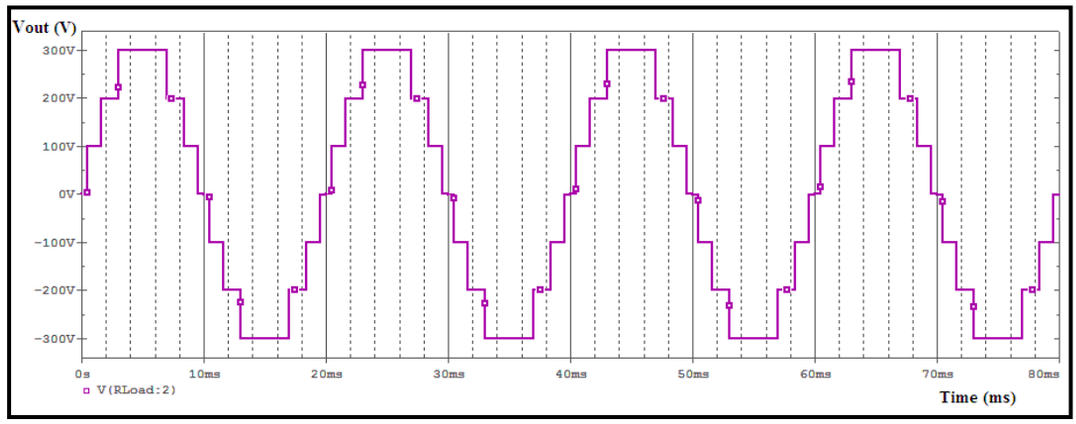


Fig. (12): Output voltage (V_{out}) waveform of seven level cascaded MLDCL inverter

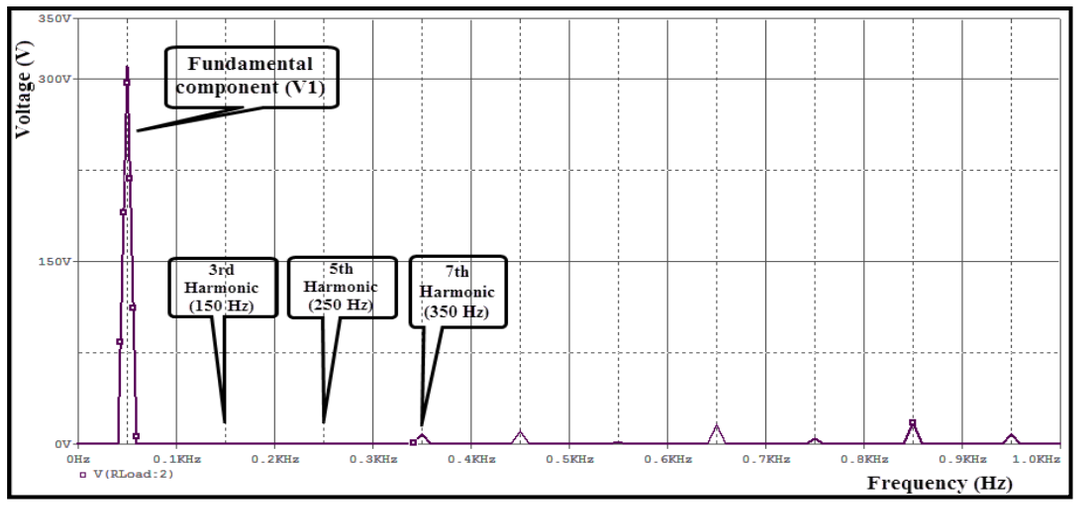


Fig. (13): Harmonic spectrum of the output voltage (V_{out})

The spectra of the output voltage show that the peak amplitude of the fundamental component (V_1) equals 313V, the 3^{rd} and 5^{th} harmonics are eliminated, whereas the 7^{th} harmonic (at 350 Hz) will appear in the spectra as a first harmonic (which is 8.21V). Obviously, there are no even harmonic components available in such a waveform. Also, the spectra show the Total Harmonic Distortion equals to 11.90% which is considered as low amplitude.

VI. Conclusions

A seven level cascaded MLDCL inverter has been designed and tested using ORCAD simulator. The output results from ORCAD simulator indicate satisfactory level of performance. The presented seven level cascaded H-bridge MLDCL inverters can eliminate two switches and their gate drivers compared with the existing cascaded multilevel inverter counterparts. MLDCL inverters are cost less due to the savings from the eliminated component and from fewer assembly steps, which also leads to a smaller size and volume.

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Modeling and Simulation of Salient Pole Synchronous Machine With Comparison Between Actual and d-q Models

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Abstract

This paper presents an investigation of both actual(direct 3-phase) and d-q dynamic models. Also simulation for a three-phase salient pole synchronous machine, using MATLAB- SIMULINK, has been performed. These two models have been compared under different operating conditions. The simulation results for synchronous machine under normal and abnormal dynamic conditions, for the two models, are obtained and compared to show the applicability, accuracy and feature for each model. On line experiment setup tests have been performed to verify the accuracy of the actual and d-q models of synchronous machine.

نمذجة وتمثيل ماكنة تزامينة ذات الاقطاب البارزة مع مقارنة بين النموذج الحقيقي والنموذج d-q

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هندسة الكهرباء

الخلاصة

هذا البحث يقدم نوعين من التمثيل وهما النموذج الحقيقي والنموذج نوع d-q لماكنة تزامنية ثلاثية الطور ذات الاقطاب البارزة باستخدام برنامج (MATLAB-SIMULINK). هذان النموذجان تم مقارنتهما و لحالات تشغيل مختلفة. ان نتائج المحاكات للماكنة التزامنية للحالات الحركية الاعتيادية وغير الاعتيادية لنموذجين تم مقارنتهما لبيان مجال التطبيق والدقة و المميزات. تم اجراء قياسات عملية و في الزمن الحقيقي من اجل تحقيق صحة ومدى دقة النموذجين.

1. Introduction

Synchronous machines are the most important and valuable machine that exist in industries, electrical tractions, renewable generation, and power generation plants. A proper model for synchronous machine is needful for a correct analysis of stability and dynamic performance. Actual model is nonlinear, complex electromechanical device, whose dynamic behavior directly affects the performance and reliability of the power system[1]. This model is presented by set of parameter equations. Therefore the equations have the self inductances, resistances, mutual inductances and effective damper winding of the stator and rotor circuit in the machine . In addition, there equations take transient effective. The model also includes the effect of dynamics involving electrical and mechanical domains. The aim of presenting the machine model can be describe to start investigating the behavior of the synchronous machine under different operating environments. Such as, power factor control , driving the machines from non-sinusoidal supply ,fault diagnosis, ac drives, improving the steady stead behavior machine , predicting the machine parameters. , etc. However, there were many research work that deal with modeling salient pole synchronous machine there numerous from model of synchronous machine important from researchers, d-q model, state space, actual model. This paper is trying to compare between two main models . These two models, have been presented in time domain, are based on actual three phase dynamic model and two d-q axis space model. Due to their basic natures, the first type is more suitable model, while the second one is suitable for limited operating conditions.

Since most of recent previous research works deal with d-q model that may give less accuracy, compared with the actual three phase model, therefore the present paper is presenting and focusing on which case d-q model can be used. This is important specially when using abnormal conditions or even in ac drive applications.

On line model required for wide applications, such as, but not limited, power stability, fault diagnosis, protection, power factor compensation, ac drives, optimizing operation, and energy managements. The degree of accuracy depend on the type of model and synchronous machine parameters [2]. However, the behavior model of the synchronous machine under abnormal condition has not been thoroughly studied and few methods exist for analyzing faults in synchronous machines[3].

2. Three-Phase Mathematical Dynamical Model of a Salient-Pole Synchronous Machine.

The three-phase synchronous machine consists of a three-stator windings mounted on the stator and one field winding mounted on the rotor part. Another two additional damper windings are mounted, with orthogonal space of electrical angle. on the rotor core, which model the short-circuited paths of the damper windings. These windings are shown schematically in Fig.1.[1].

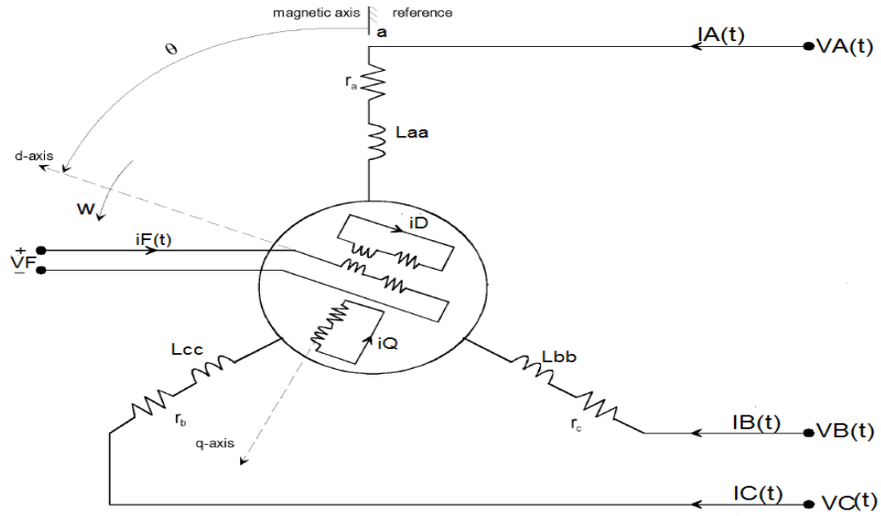

Fig. (1): Schematic three phase model representation of a salient synchronous machine circuits[1].

Electric and magnetic equations of the synchronous machine are written according to the multiple-coupled circuit theory from application of Kirchhoff's voltage law (B. H curve, eddy currents, hysteresis and thermal effects are neglected) as in the following equations [1][4]:

$$[V] = [r][i] + \frac{di}{dt}\{[L][i]\} \quad (1)$$

Where :

$$[V] = [v_a(t)\ v_b(t)\ v_c(t)\ v_f(t)\ 0\ 0]^t$$

$$[r] = diagonal[r_a\ r_b\ r_c\ r_f\ r_{kd}\ r_{kq}]$$

$$[i] = \left[i_a(t)\ i_b(t)\ i_c(t)\ i_f(t)\ i_{kd}(t)\ i_{kq}(t)\right]^t$$

$$[L] = \begin{bmatrix} [L_{ss}(\Theta(t))] & [L_{sr}(\Theta(t))] \\ [L_{rs}(\Theta(t))] & [L_{rr}] \end{bmatrix}$$

See Appendix A.1

Where: $[v]$ is the vector consisting of voltages of three phase a, b ,c, field voltage, $v_f(t)$ and two damper windings (volt). $[r]$ is the vector consisting of resistance of three phase winding a, b ,c, field and two damper windings (ohm). $[i]$ is the vector consisting of currents of three phase a, b ,c, field current $i_f(t)$ and two current damper windings (Ampère). $[L]$ is vector consisting of inductances which are dependent on the rotor position (Θ) in henry.

The electromagnetic torque for a complete dynamic model of the system is [5] :

$$Te = \frac{2}{3\sqrt{3}}\left\{\Psi_a\left(i_c(t) - i_b(t)\right) + \Psi_b\left(i_a(t) - i_c(t)\right) + \Psi_c\left(i_b(t) - i_a(t)\right)\right\} \quad (2)$$

$$\frac{d_{wr}}{d_t} = \frac{P}{J}(T_m - T_e) \quad (3)$$

where T_m and T_e are the mechanical and the electromagnetic torques(N.M), respectively $i_a(t)$, $i_b(t)$ and $i_c(t)$are the stator phase currents (Amp.), Ψ_a, Ψ_b and Ψ_c are stator flux linkages (Wb), w_r is the angular speed (rad/sec), p is number of poles ,J is the moment of inertia (kg.m^2).

3. Actual Modeling and Simulation of a Salient-Pole Synchronous Machine Using Matlab-simulink

The basic Simulink , compared with simpower system library is effective, fast, reliable, improve accuracy, speeding up simulation and easy to tune, compare and follow for on line applications. The study model is performed on a salient-pole synchronous machine by using Matlab-Simulink to solve the above equations. These equations are rewritten in suitable way to suit the basic Simulink. For example refer to phase "a" the solve one phase current $i_a(t)$ rewritten of equation in the following from :

$$\frac{d_{ia}}{d_t} = \frac{1}{L_{aa}}\{(v_a - i_a * r_a) - \frac{d}{d_t}(L_{ab} * i_b + L_{ac} * i_c + L_{af} * i_f + L_{aD} * i_{kd} + L_{aQ} * i_{kq}) \quad (4)$$

Where L_{aa}, L_{ab}, L_{ac} ,L_{af} ,LaD and L_{aQ} ara inductances and their value are dependent on the rotor position (θ).[6].See appendix A.1

Similarly the above equations can be arranged for the other two phases (d_{ia}/d_t and d_{ic}/d_t) currents and two damper windings currents . The complete Simulink block for three phase dynamic model of salient pole synchronous machine is shown in Fig. 2.

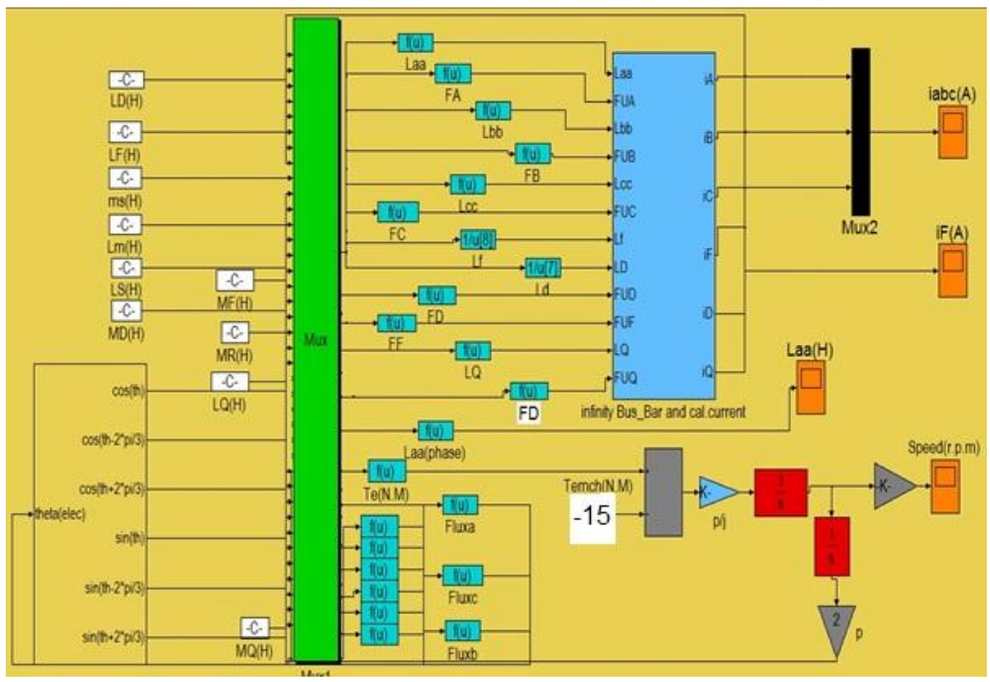

Fig. (2): Three phase dynamic Simulink model of salient pole synchronous machine

4. Mathematical d-q Model of a Salient-Pole Synchronous Machine

The transformation from the actual abc phases time variables to the dq0 variables can be performed by using park transformation [3][7]. For the intent of comparison between the actual and d-q models for Salient-Pole synchronous machine, is shown in Fig. 3. The d-q model is also build and implemented using in basic Simulink.

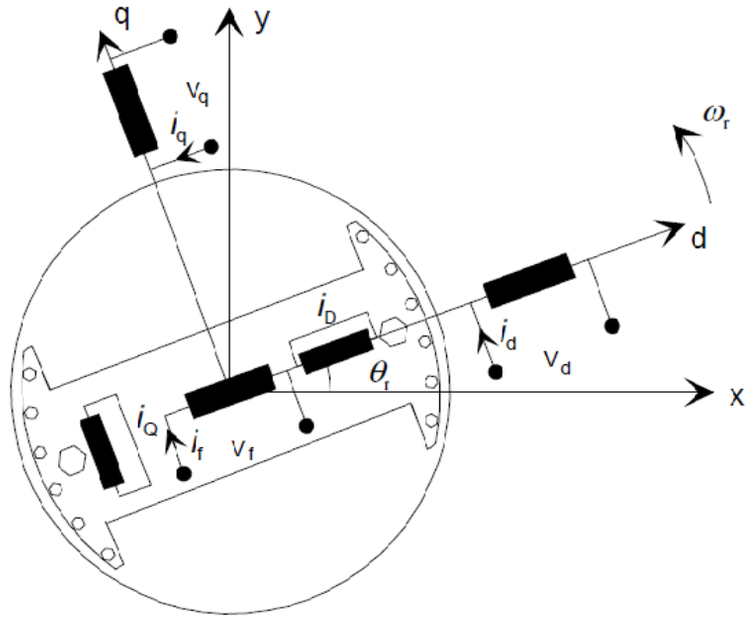

Fig. (3): Schematic d-q model representation of a salient synchronous machine circuits

The synchronous machine d-q model equations are as follow (expressed in the rotor reference frame which is simple to be used for wide control application compare with other type)[1][8]:

Voltage equation (V)

$$V_d = r * i_d + \rho\lambda_d - w_r * \lambda_q \quad (5)$$

$$V_q = r * i_q + \rho\lambda_q - w_r * \lambda_d \quad (6)$$

$$0 = r_{kd} * i_{kd} + \rho\lambda_{dr} \quad (7)$$

$$0 = r_{kq} * i_{kq} + \rho\lambda_{qr} \quad (8)$$

$$V_f = r_f * i_f + \rho\lambda_f \quad (9)$$

Where ρ is differential operation

where fluxes linkage (wb)

$$\lambda_d = L_d * i_d + L_{md} * i_d + L_{md} * i_f \quad (10)$$

$$\lambda_q = L_q * i_q + L_{mq} * i_q \quad (11)$$

$$\lambda_{kd} = L_{kd} * i_{kd} + L_{md} * i_d + L_{md} * i_f \quad (12)$$

$$\lambda_{kq} = L_{kq} * i_{kq} + L_{mq} * i_q \quad (13)$$

$$\lambda_f = L_f * i_f + L_{md} * i_{kd} + L_{md} * i_d \quad (14)$$

The electromagnetic torque(N.M) in d-q model is[8]:

$$T_e = \left(\frac{3}{4}\right) * P * \{(L_{md} * i_f * i_{kq}) + (L_{md} * i_{kd} * i_q) - (L_{mq} * i_{kq} * i_d) + (L_d - L_q) * i_d * i_q\} \quad (15)$$

Descriptions of the symbols in above equations are as follows:

P, number of poles, r_{kd} is rotor d-axis damper winding resistance (ohm), r_{kq} is rotor q-axis damper winding resistance (ohm), rf is rotor field winding resistance (ohm), Ld is stator d-axis winding inductance (H), L_q is stator q-axis winding inductance (H), L_{kd} is rotor d-axis damper winding inductance (H), L_{kq} is rotor q-axis damper winding inductance (H), L_{md} is d-axis magnetizing inductance (H), L_{mq} is q-axis magnetizing inductance (H),L_f is rotor field winding inductance (H).

5. D-q Modeling and Simulation of a Salient-Pole Synchronous Machine Using Matlab-Simulink

The analysis of synchronous machine equations for direct-quadrature (d-q) transformation is a mathematical transformation used to simplify the analysis of three phase circuit. In case of balanced three phase circuits, application of d-q transformation reduces the complex AC quantities to two quantities.[9,10,11]. The parameters associated with d and q axes may be directly measured from terminal tests[1].

But the equations, concerning d-q model, represent the machine when it is assumed linear, symmetrical, operate at normal conditions, symmetrical windings and supplied by balance three phase sinusoidal supply voltage. The results accuracy depends on how much the machine deviated from ideal conditions. The complete Simulink block for d-q dynamic model of salient pole synchronous machine is given in Fig. 4.

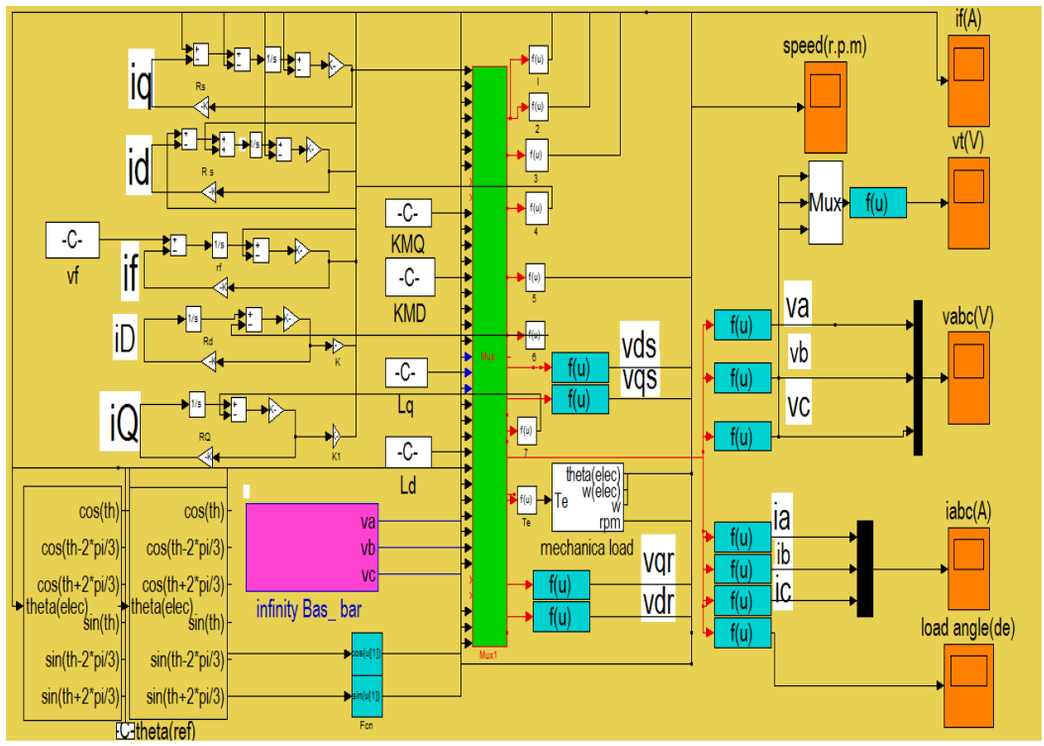

Fig. (4): MATLAB-SIMULINK d-q dynamic model of three phase salient pole synchronous machine.

6. Simulation Results

The simulation results, using the two types of machine models, have been obtained for different operating conditions. These operating conditions are classified in to two main points; the first is assumed the machine and the supply are symmetrical, balance, or unbalance steady state, and normal operations. While the second classifier is operating at different conditions, by one point or more points than that of the first classifier, other condition for example single phasing i.e. The first type assume the power supply is balance and sinusoidal, at 2sec from simulation time apply the mechanical torque load of -15 Nm. The obtained results comparing between the actual three phase-and d-q phase models, are almost coincides at steady state. While in the transient condition, the simple different between actual and d-q models for simulation results, because assume that mutual inductance between damper winding (D) and

stator windings are same as the mutual inductance between field winding and stator windings which is an acceptation approximate[2][17][18] as shown in Figs. (5-10).

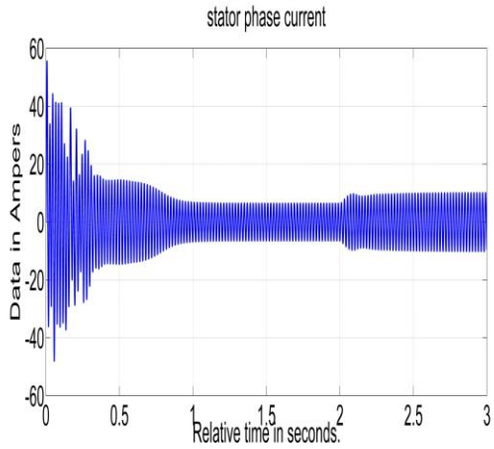

Fig. (5): Stator current of actual model (A)

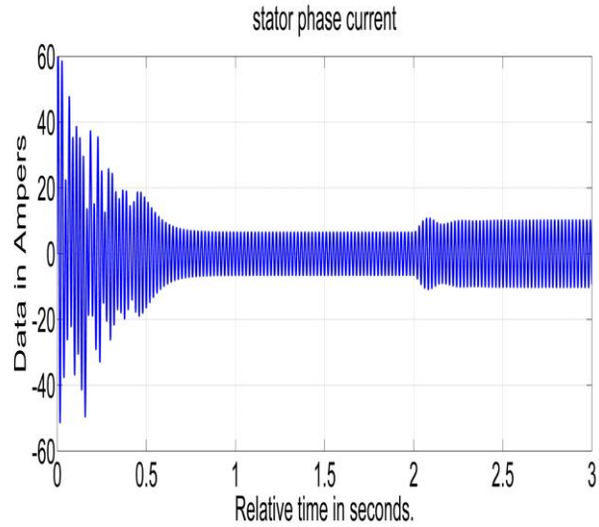

Fig. (6): Stator current of d-q model(A)

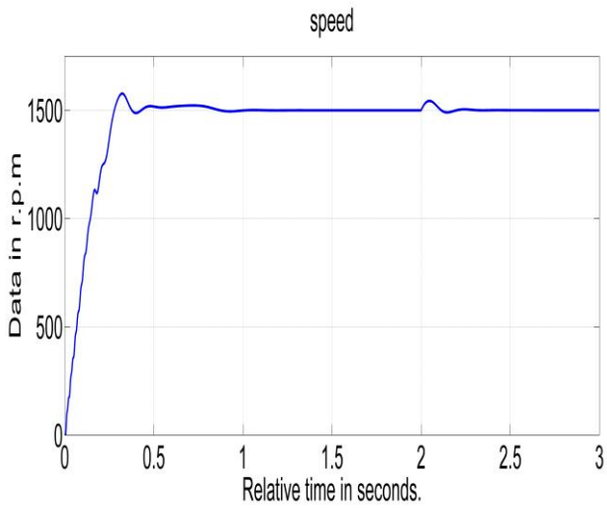

Fig. (7): Rotor speed of actual model (r.p.m)

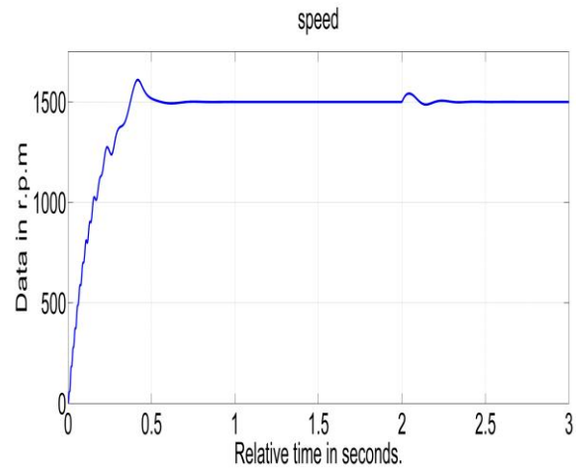

Fig. (8): Rotor speed of d-q model (r.p.m)

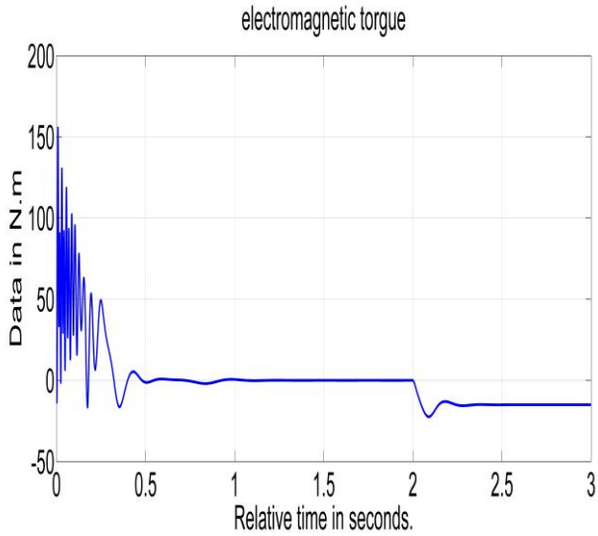

Fig.9.

Electromagnetic torque of actual model (N.m)

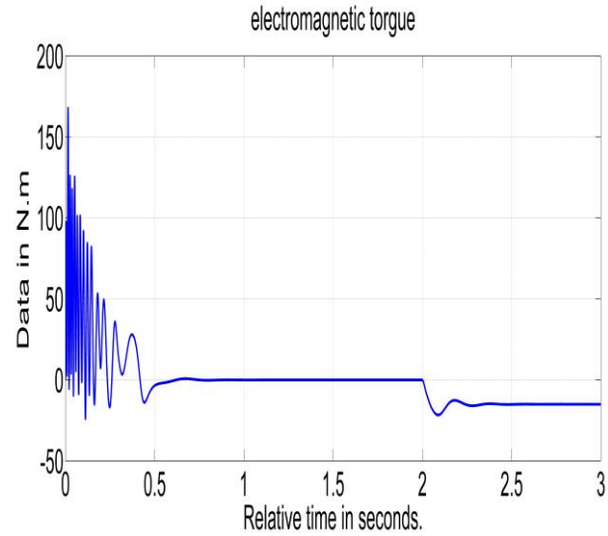

Fig.10 .

Electromagnetic torque of d-q model (N.m)

The second type conditions , by considering a non-sinusoidal power supply such as quasi square waveform voltage. The obtained results, comparing between the actual three phase and d-q phase models, for steady state condition as shown in Figs(11-14).The differences are due to the nature of d-q model which consider the transformation matrix by assuming the variable parameters vary sinusoidally.

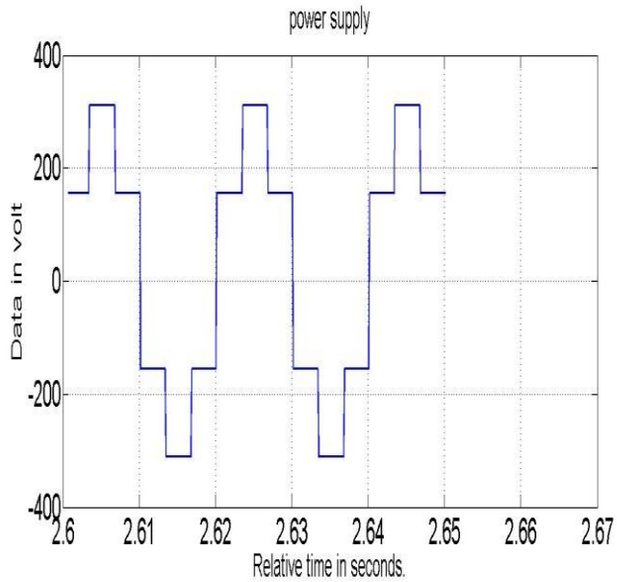

Fig.11

Voltage source of actual and d-q models (V)

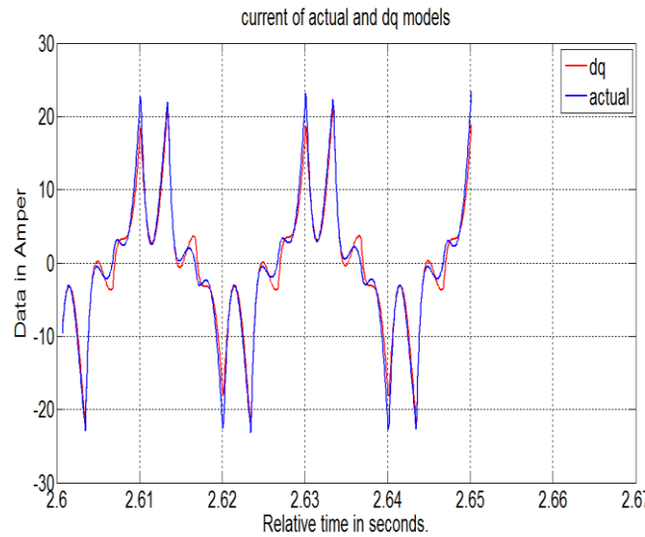

Fig.12.

stator current of actual and d-q models (A)

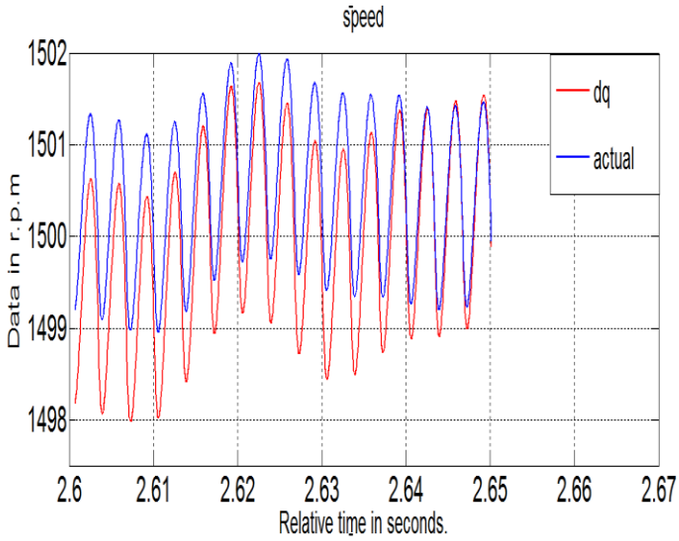

Fig.13

Rotor speed of actual and d-q models (r.p.m)

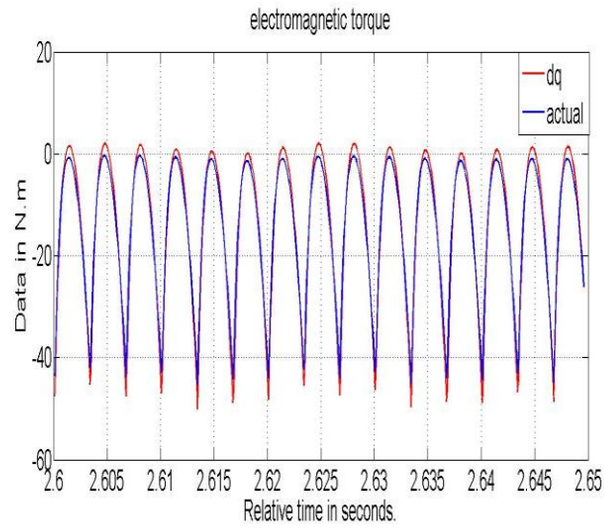

Fig.14.

Electromagnetic torque of actual and d-q models (N.m)

7.Experimental Results

The experimental setup, is shown in Fig.15-a, includes a 6.2 kVA, 50Hz, 380 V, 4 pole, three phase salient-pole synchronous machine without damper windings,and the schematic of on line experiment setup shown in Fig.15-b.The three phase source voltage from practical work supposed for both actual and d-q models to comprise of perform simulation models. The current signature analysis (FFT) can be compered for the actual and d-q models with practical current waveform, see Figs(16-23) .

Fig.15-a. on line experiment setup

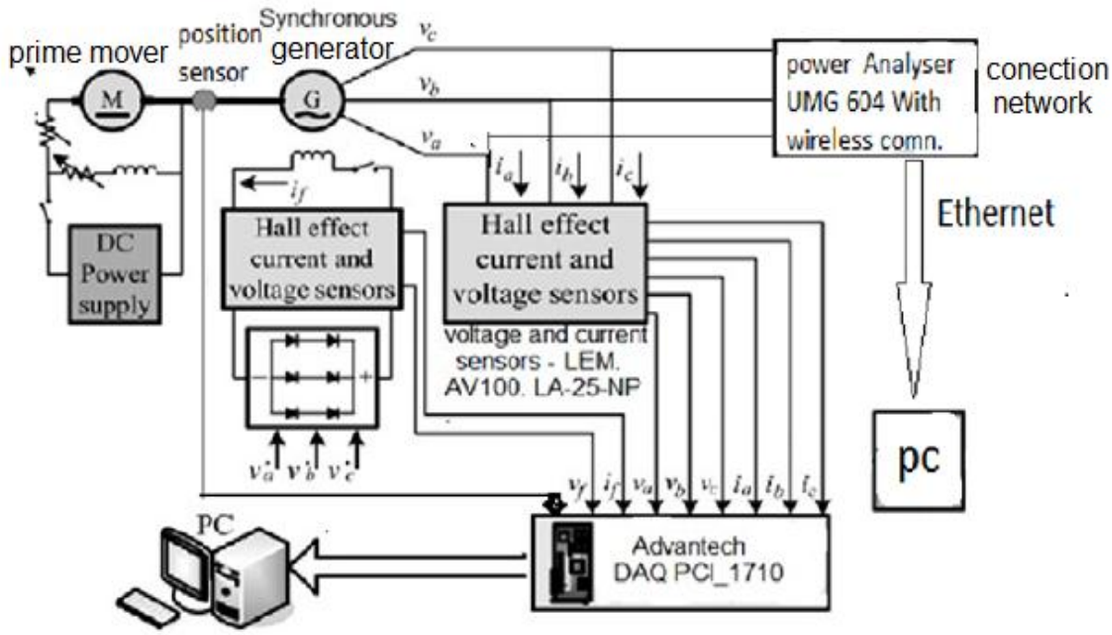

Fig.15-b. Schematic of on line experiment setup

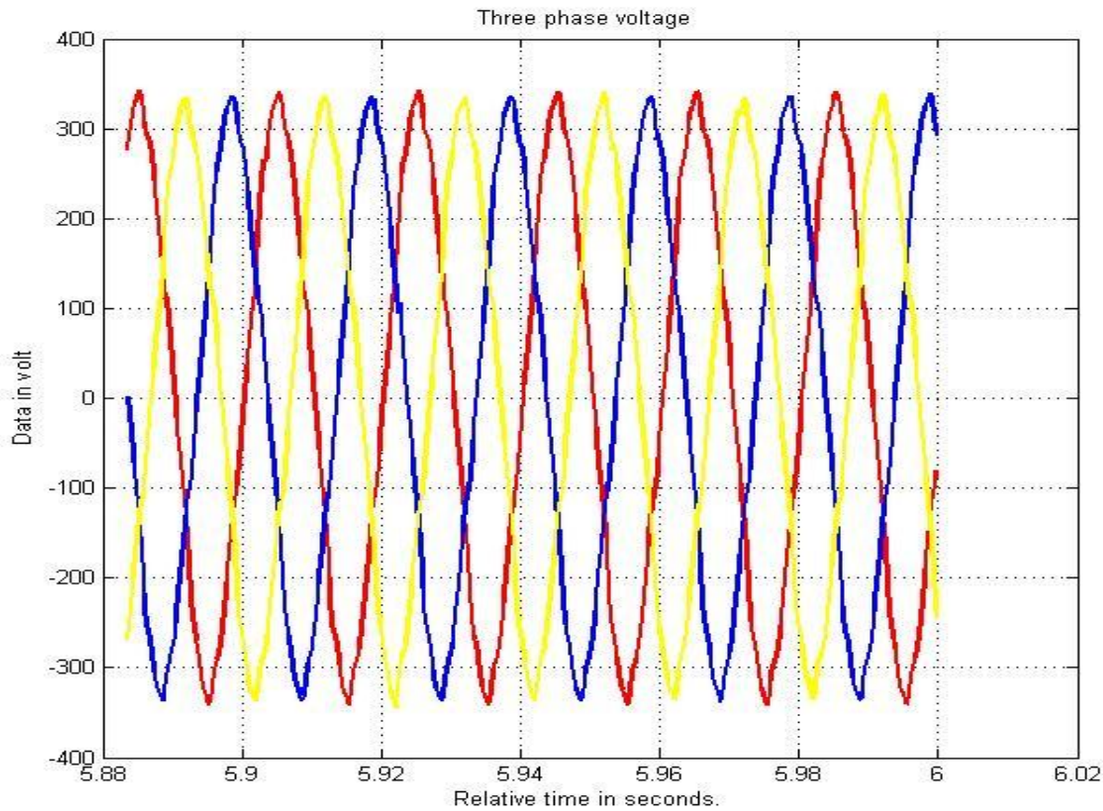

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Fig.16. The practical three phase terminal voltage waveforms

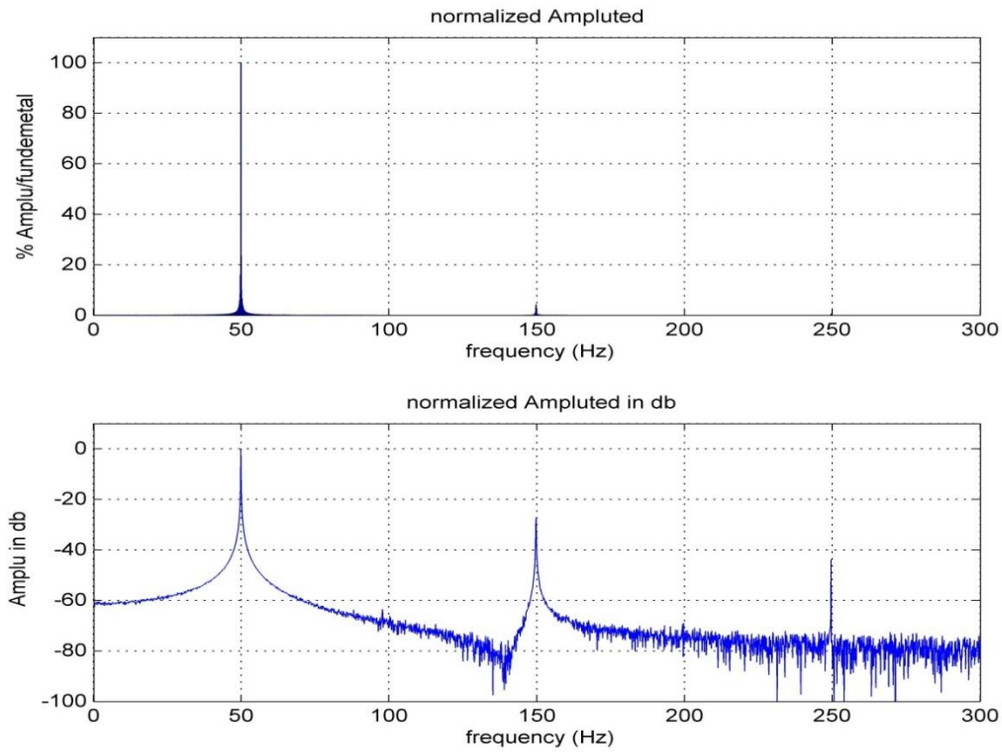

Fig.(17): Phase voltage spectrum (practical results)

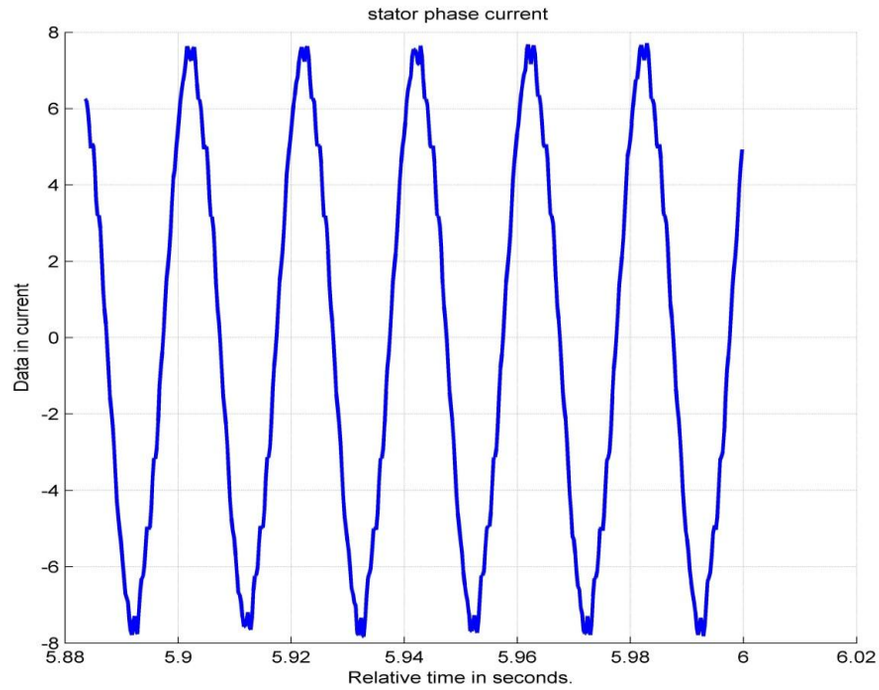

Fig. (18): The practical stator phase current waveform

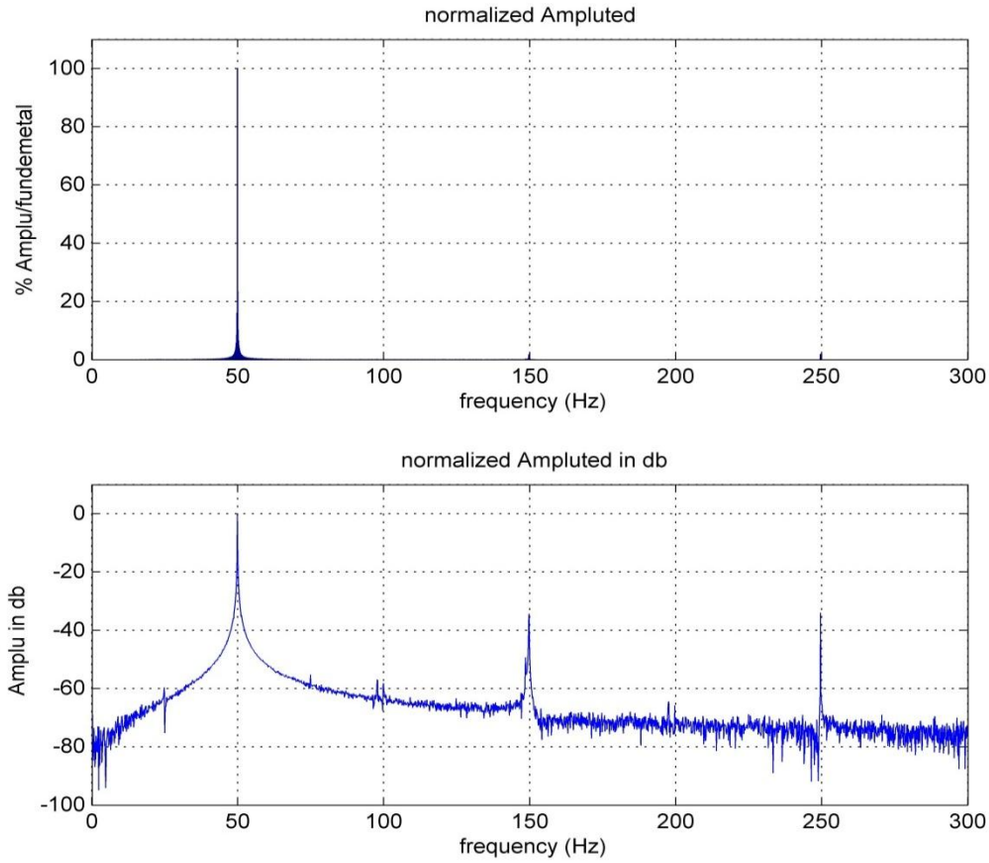

Fig. (19): Phase current spectrum (practical results)

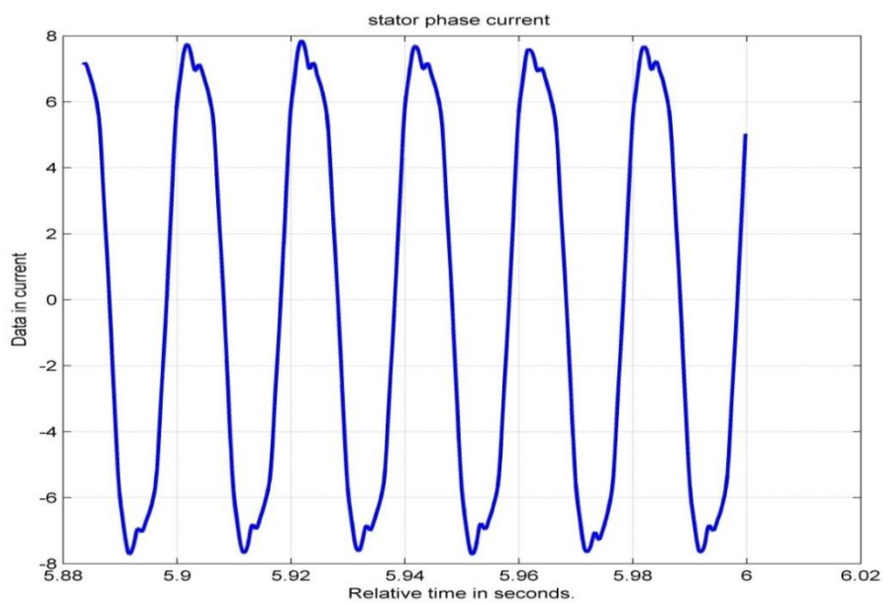

Fig. (20): Stator phase current actual model (A)

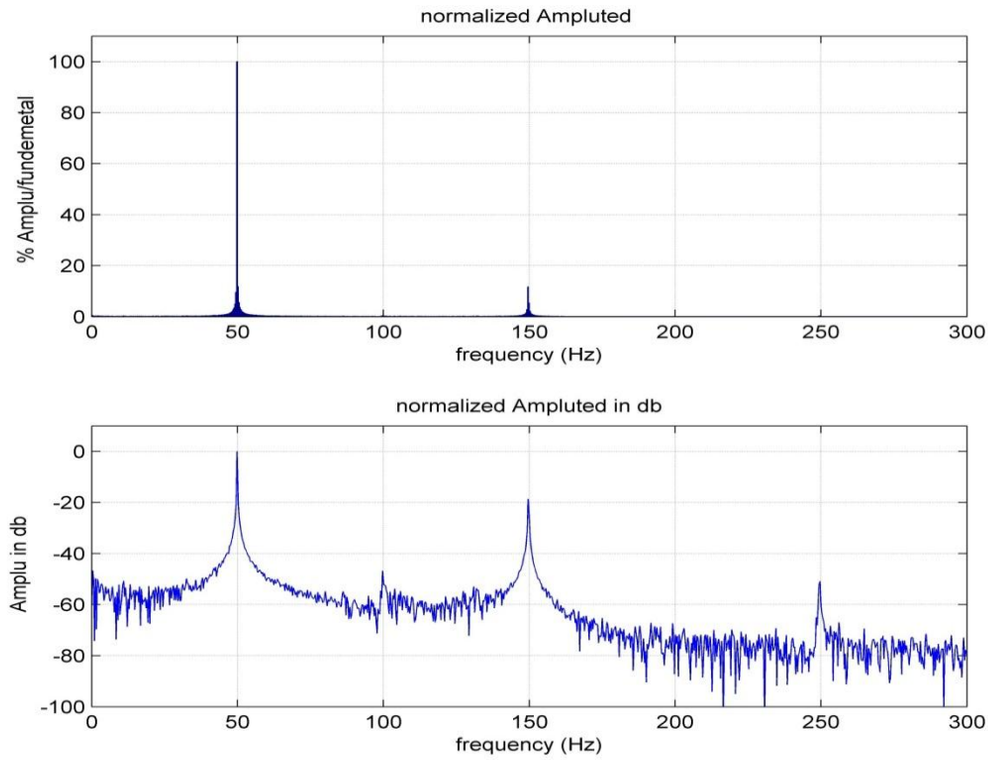

Fig. (21): Phase current spectrum actual model

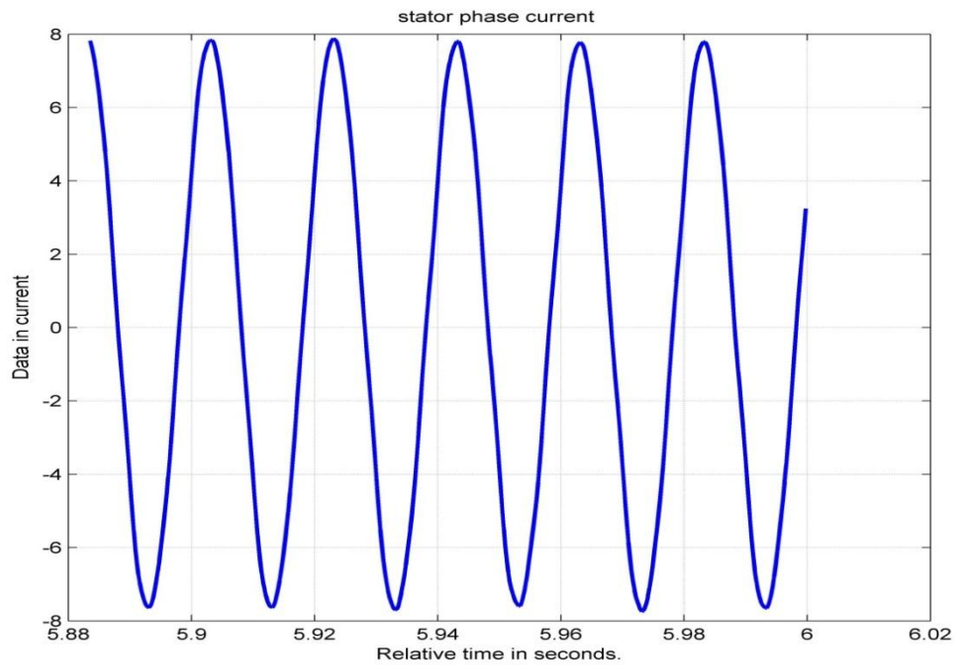

Fig. (22): Stator phase current d-q model (A)

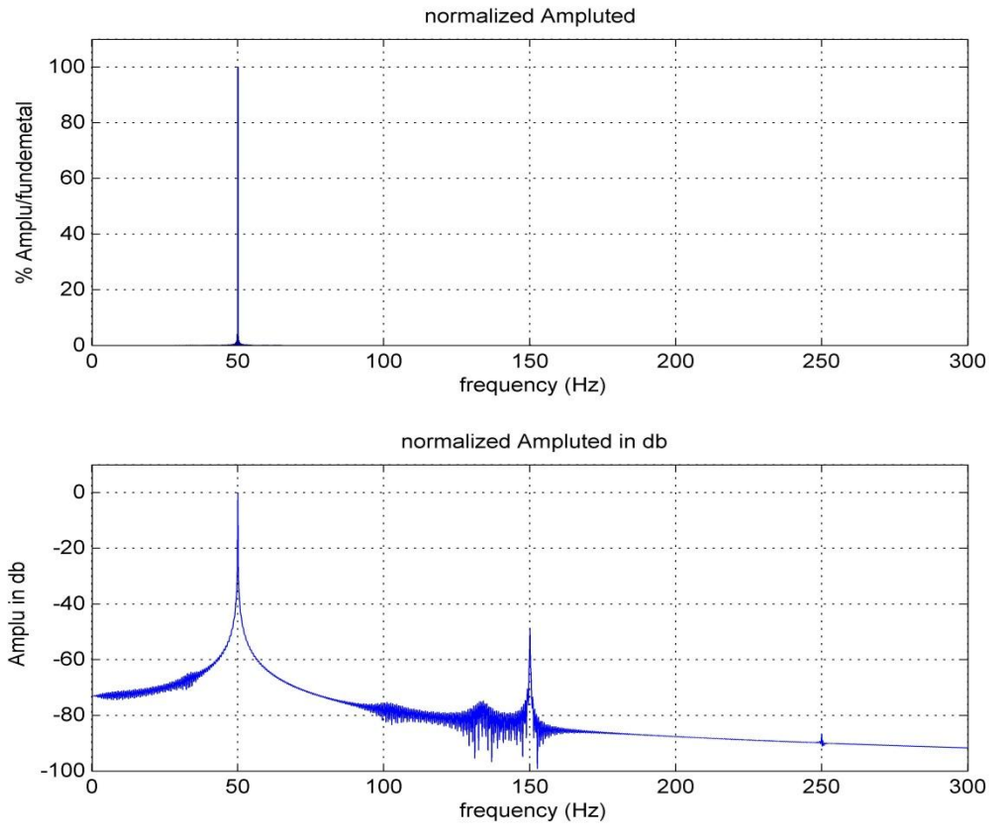

Fig. (23): Phase current spectrum d-q model

9. Conclusions

From both theoretical and practical results, the actual three phase model is more convenient to be used for normal and abnormal conditions, even the supply voltage is nonsinusoidal. While the d-q model is suitable to be used for normal condition and others type conditions, this model simulation results according to accuracy and efficiency depended on the conversion parameters from actual to d-q parameters. The degree of accuracy depends on how the operating conditions are far from normality or effect value of THD of voltage supply. Therefore, actual model is more preferable than d-q model. In some cases like machine parameter estimations or methods of speed control using PWM strategies, such as space vector control, d-q model is more simpler and faster , than actual model to be used as on line.

10.Appendix

A.1:

Expressions for the inductance matrix $[Lss(\Theta(t))]$ are given below[11,12,13].

stator self-inductances

$Laa = Ls + Lmcos(2\Theta)$

$Lbb = Ls + Lmcos(2(\Theta - 2\pi/3))$

$Lcc = Ls + Lmcos(2(\Theta + 2\pi/3))$

stator mutual inductances

The stator to stator mutual inductances are a function of rotor position since they are influenced by rotor saliency.

$Lab = Lba = -Ms - Lmcos2(\Theta + \pi/6)$

$Lbc = Lcb = -Ms - Lmcos2(\Theta - \pi/2)$

$Lca = Lac = -Ms - Lmcos2(\Theta + 5\pi/6)$

The inductance matrix $[Lsr(\Theta(t))] = [Lrs(\Theta(t))]$are given below,

Stator-to-rotor(field winding) mutual inductances

$Laf = Lfa = Mfsin(\Theta)$

$Lbf = Lfb = Mfsin(\Theta - 2\pi/3)$

$Lcf = Lfc = Mfsin(\Theta + 2\pi/3)$

Stator-to-rotor(two damper winding) mutual inductances

$LaD = LDa = MDcos(\Theta)$

$LbD = LDb = MDcos(\Theta - 2\pi/3)$

$LcD = LDc = MDcos(\Theta + 2\pi/3)$

$LaQ = LQa = MQsin(\Theta)$

$LbQ = LQb = MQsin(\Theta - 2\pi/3)$

$LcQ = LQc = MQsin(\Theta + 2\pi/3)$

The inductance matrix $[Lrr]$is rotor self-inductances are constant[11][14].

A.2:

Synchronous machine Parameters:

4-pole, 6.2KVA, 380V, 50,Hz, 36 stator slots

R : Stator phase resistance=2.1Ω

Ld :Equivalent direct axis inductance = 0.0882H

Lq : Equivalent quadrature axis inductance =0.0579H

Ms : Stator phase winding mutual inductance= -0.0243H

MF :Stator to field mutual inductance= 0.4969H

Rf :Equivalent field resistance=21Ω

Lf : Field winding self inductance=6H

Lm :Stator phase winding magnetizing inductance= 0.0101H

Ls :Stator phase winding inductance =0.0669H

J : machine shaft inertia =0.07981 kgm^2

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Modified Cuk Convertor Optimal Controller Design Using Particle Swarm Optimization

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Abstract

This paper presents and discusses the results of a PSO-based controller, designed to control the performance of one modification of the Cuk dc-dc converter. The studied modification involve coupling the two coils around one mutual core. Mathematical state space model has been derived for the modified Cuk convertor. A state feedback controller for the modified converter has been designed, using a particle swarm optimization technique with a time-decreased weighting inertia. Particle swarm optimization technique has been used for selecting the optimal values of the state feedback controller gains. The closed-loop system, together with the open-loop system responses have been analyzed and composed. The proposed method gives promisable results.

Keywords : Modified Cuk Convertor, Particle Swarm Optimization.

تصميم مسيطر لدائرة المغير كوك المطورة باستخدام أمثلية حشد الجزيئات

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قسم الهندسة الكهربائية / كلية الهندسة / جامعة الموصل

الخلاصة

تقدم هذه الورقة البحثية نتائج تصميم مسيطر ذكي ذي أمثلية لمغير فولتية مطور من نوع (Cuk) بإستخدام تقنية حشد الجزيئات (PSO)، مع مناقشة هذه النتائج. يشمل التطوير في دائرة المغير (Cuk) على وضع كلا ملفيه على قلب مشترك واحد. تم إيجاد التمثيل الرياضي لمنظومة المغير بصيغة مصفوفات فضاء الحالة. وتم تصميم مسيطر تغذية خلفية بإستخدام تقنية حشد الجزيئات ذات عزم القصور المتناقص مع الزمن. حيث تم إستخدام هذه التقنية لإختيار قيم كسب ذات أمثلية لمسيطر التغذية العكسية (الخلفية). وقد تم عرض إستجابة النظام في حالة الحلقة المفتوحة وإستجابته في حالة الحلقة المغلقة (مع المسيطر)، عند عدة حالات تشغيل مختلفة لكل منها، للتعرف على مدى التحسن الحاصل في الإستجابة نتيجة إستخدام المسيطر المصمم بهذه الطريقة، والتي تعد من الطرق الواعدة.

1. Introduction:

Switching mode power supplies (SMPSs) have occupied a considerable interest among the other power electronics applications. This is duo to the fact that they have high efficiency with an easy requirements to construct and a low cost. Cuk convertor is one of the basic types of the (SMPSs) which has the ability to increase or decrease the level of the dc voltage. This is according to the duty cycle of the switch.[1] This type ,as the others, has witnessed many successful modifications on its basic construction design, aimed to improve their performance.[2] In addition, to the above mentioned importance of such devices, many of the modern applications i.e. control, industrial and communication applications, need a very high reliable devices. Therefore, more attention have to be focused on the (SMPSs) devises. This research dealt with the design of an optimal controller for one of the modifications of the Cuk convertor, making used of one of the most important techniques of the computational intelligence methods which is the particle swarm optimization (PSO).

2. Literature Review:

Many researchers have paid their attention to the study of (SMPSs) control, as:

1. Dr. A. H. Ahmed and other have designed a robust state feedback controller for the Cuk convertor by using the H∞/μ technique at 2006.[3]
2. O. A. Taha has designed a state feedback controller for the Cuk convertor using the H∞/μ technique at 2006.[4]
3. S. Eshtehardiha and others have designed a linear quadratic optimal controller to achieve the voltage controller for the Cuk convertor, and used the genetic algorithm to chose the parameters of the LQR. This was at 2007.[5]
4. S. S. Sabri has used the genetic algorithm to select the parameters of the fuzzy controller for the Cuk convertor at 2008.[6]
5. S. Eshtehardiha and others have used the genetic algorithm to design the pole placement controller for the Cuk Convertor, at 2008. [7]
6. S. Eshtehardiha and others have used a hybrid technique of the genetic algorithm and the particle swarm optimization, to design the pole placement controller for the Cuk Convertor, at 2008. [8]
7. K. Sundereswaran and others have desined the state feedback controller for the Boost Convertor by using an optimization technique mimics the ants' foraging process, at 2011. [9]
8. M. A. Narsardin has designed the artificial neural network controller for the buck convertor at 2012. [10]
9. A. N. Al-Rabadi and M. A. Barghash have used a global search genetic algorithm for tunning the parameters of a fuzzy-PID controller for the buck convertor at 2012.[11]

3. The Modified Cuk Convertor Circuit: [3]

This convertor is one of the many succeeded modifications which have been being made to the normal Cuk convertor. It has been done by winding the two coils of the convertor around a single mutual core, as shown in figure (1).

This modificion has many advantages over the common Cuk convertor. It is the ability to reduce the ripple current to zero, if proper turn ratio and coupling coefficient are chosen. Also, it produces a device with a lower weight, cost, and smaller size.

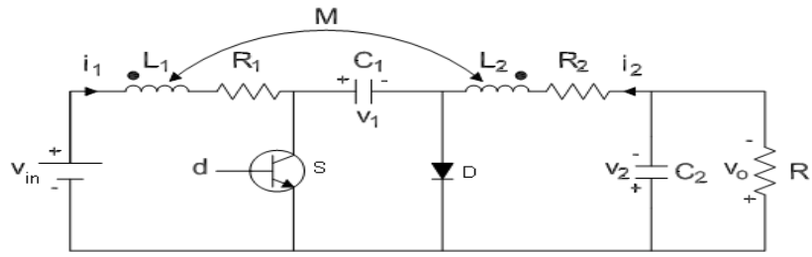

Figure (1): The Modified Cuk Circuit.

4. Analysis of the System: [4]

There are three main problems that can be examined in the study of a system in the control contexts: system dynamics, system identification or modeling, and system control. Since Cuk convertor has four energy storage devices (C_1, C_2, L_1, L_2), therefore; the system dynamics are expressed by a fourth order representation.

The system works with two modes to accomplish the dc level conversion: [2,12]

Mode 1: When the switch is ON, as in figure (1.2.a): The capacitor (C_1) is charged by the source when the switch is turned ON, the current through (L_1) increases proportionally with the duty cycle of the switch.The diode will be reverse biased, and the capacitor (C_1) will lose its charge through two directions; through the closed switch to the load and (C_2), and through (L_2) then (L_1) by the mutual core.

Mode 2: When the switch is OFF, as in figure (1.2.b): The diode will be forward biased. The capacitor C_1 will be recharged through the voltages of the source L_1, and the voltage induced through the mutual core.

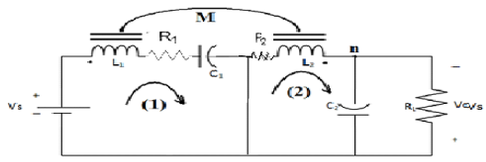

Figure (2.a): Mode 1 (switch on)

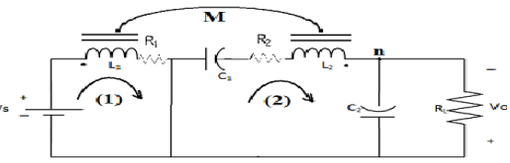

Figure (2.b): Mode 2 (switch off).

5. System Mathematical Modeling:

Since the path of current is the same into the both inductors, then one can use the algebraic sum to express the relations of the inductances, as follows:

$$V_{L1} = L_1 \frac{di_1}{dt} + M \frac{di_2}{dt} \tag{5.1}$$

$$V_{L2} = M \frac{di_1}{dt} + L_2 \frac{di_2}{dt} \tag{5.2}$$

By solving these two instantaneous equations, one can obtain:

$$\frac{di_1}{dt} = \frac{L_2}{L_1 L_2 - M^2} V_{L1} + \frac{-M}{L_1 L_2 - M^2} V_{L2} \tag{5.3}$$

$$\frac{di_2}{dt} = \frac{-M}{L_1 L_2 - M^2} V_{L1} + \frac{L_1}{L_1 L_2 - M^2} V_{L2} \tag{5.4}$$

5.1 Differential equations for the two modes:

Mode 1: Applying Kirchhoff's law to the equivalent circuit of this mode, and by neglecting the voltages across the switch, the following equations may be written:

$$V_{L1} = V_{in} - i_1 R_1 \quad (5.5)$$

$$V_{L2} = V_{C1} - V_{C2} - i_2 R_2 \quad (5.6)$$

Substituting these two equations into (4.3) and (4.4):

$$\frac{di_1}{dt} = \frac{-L_2 R_1}{\tilde{n}} i_{L1} + \frac{MR_2}{\tilde{n}} i_{L2} + \frac{-M}{\tilde{n}} V_{C1} + \frac{M}{\tilde{n}} V_{C2} + \frac{M}{\tilde{n}} V_{in} \quad (5.7)$$

$$\frac{di_2}{dt} = \frac{MR_1}{\tilde{n}} i_{L1} + \frac{-L_1 R_2}{\tilde{n}} i_{L2} + \frac{L_1}{\tilde{n}} V_{C1} + \frac{-L_1}{\tilde{n}} V_{C2} + \frac{-M}{\tilde{n}} V_{in} \quad (5.8)$$

$$\text{As:} \quad \tilde{n} = L_1 L_2 - M^2$$

While : $-i_{L2} = C_1 \frac{dv_{c1}}{dt}$ (5.9)

$$\frac{dv_{c1}}{dt} = -\frac{1}{C_1} . i_{L2} \quad (5.10)$$

Now, by applying Kirchhoff's law at node (n) :

$$i_{c2} = i_{L2} - Io \quad (5.11)$$

$$Io = \frac{v_{c_2}}{R_L} \quad (5.12)$$

(5.13)

$$i_{c2} = C_2 . \frac{dv_{c2}}{dt}$$

$$\frac{dv_{c2}}{dt} = \frac{1}{C_2} . i_{c2} \quad (5.14)$$

$$\frac{dv_{c2}}{dt} = \frac{1}{C_2} . i_{L2} - \frac{1}{C_2 R_L} . v_{c2} \quad (5.15)$$

The output matrix can be represented easily by the relation:

$$Vo = v_{c2} \quad (5.16)$$

Mode 2: Applying Kirchhoff's law to the equivalent circuit of this mode, and by neglecting the voltages across the switch, the following equations may be written:

$$V_{L1} = V_{in} - i_1 R_1 - V_{C1} \quad (5.17)$$

$$V_{L2} = -V_{C2} - i_2 R_2 \quad (5.18)$$

Substituting these two equations into (4.3) and (4.4):

$$\frac{di1}{dt} = \frac{-L_2R_1}{\tilde{n}} i_{L1} + \frac{MR_2}{\tilde{n}} i_{L2} + \frac{-L_2}{\tilde{n}} V_{C1} + \frac{M}{\tilde{n}} Vc_2 + \frac{L_2}{\tilde{n}} V_{in} \quad (5.19)$$

$$\frac{di2}{dt} = \frac{MR_1}{\tilde{n}} i_{L1} + \frac{-L_1R_2}{\tilde{n}} i_{L2} + \frac{M}{\tilde{n}} V_{C1} + \frac{-L_1}{\tilde{n}} Vc_2 + \frac{-M}{\tilde{n}} V_{in} \quad (5.20)$$

As in Mode 1, the representation of the voltages across the inductors may be obtained by the following equations, as follows:

$$i_{L1} = C_1 . \frac{dvc_1}{dt} \quad (5.21)$$

$$\frac{dvc_1}{dt} = \frac{1}{C_1} i_{L1} \quad (5.22)$$

$$\frac{dvc_2}{dt} = \frac{1}{C_2} . i_{L2} - \frac{1}{C_2 . R_L} v_{c2} \quad (5.23)$$

And the output matrix is expressed by the same equation of (5.16).

5.2 State space representation of the system:

In order to write the general state space mathematical model for the overall system, let the state variable to be:

$x_1 = i_{L1}$
$x_2 = i_{L2}$
$x_3 = v_{c1}$
$X_4 = v_{c2}$

$$x = \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} = \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \end{bmatrix}$$

Applying the standard form of the state space representation:

$$x^{\cdot} = Ax + Bu \quad (5.24)$$

$$y = Cx + Du \quad (5.25)$$

$$Aon = \begin{bmatrix} -\frac{L_2R_1}{L_1L_2 - M\wedge 2} & \frac{MR_2}{L_1L_2 - M\wedge 2} & -\frac{M}{L_1L_2 - M\wedge 2} & \frac{M}{L_1L_2 - M\wedge 2} \\ \frac{MR_1}{L_1L_2 - M\wedge 2} & -\frac{L_1R_2}{L_1L_2 - M\wedge 2} & \frac{L_1}{L_1L_2 - M\wedge 2} & -\frac{L_1}{L_1L_2 - M\wedge 2} \\ 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & -\frac{1}{R_LC_2} \end{bmatrix}$$

$$Aoff = \begin{bmatrix} -\frac{L_2R_1}{L_1L_2 - M\wedge 2} & \frac{MR_2}{L_1L_2 - M\wedge 2} & -\frac{L_2}{L_1L_2 - M\wedge 2} & \frac{M}{L_1L_2 - M\wedge 2} \\ \frac{MR_1}{L_1L_2 - M\wedge 2} & -\frac{L_1R_2}{L_1L_2 - M\wedge 2} & \frac{M}{L_1L_2 - M\wedge 2} & -\frac{L_1}{L_1L_2 - M\wedge 2} \\ -\frac{1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & -\frac{1}{R_LC_2} \end{bmatrix}$$

$$Boff = Bon = \begin{bmatrix} \frac{L_2}{L_1L_2 - M\wedge 2} \\ -\frac{M}{L_1L_2 - M\wedge 2} \\ 0 \\ 0 \end{bmatrix} \quad \text{and} \quad Coff = Con = [0 \quad 0 \quad 0 \quad 1]$$

In order to find the system matrix (A) of the overall system, (*Aon*) is multiplied by the ON period, and (*Aoff*) is multiplied by the OFF period, then adding the two matrices to each other, the overall system matrix is found,[13] and as follows:

Doff = 1 – Don (5.26)

A = A1 * Don + A2 * Doff (5.27)

$$A = \begin{bmatrix} -\frac{L_2 R_1}{L_1 L_2 - \mathrm{M}\text{^}2} & \frac{M R_2}{L_1 L_2 - \mathrm{M}\text{^}2} & \frac{-\mathrm{DonM} + L_2 + \mathrm{Ds} L_2}{L_1 L_2 - \mathrm{M}\text{^}2} & \frac{M}{L_1 L_2 - \mathrm{M}\text{^}2} \\ \frac{M R_1}{L_1 L_2 - \mathrm{M}\text{^}2} & -\frac{L_1 R_2}{L_1 L_2 - \mathrm{M}\text{^}2} & \frac{\mathrm{Don} L_1 + \mathrm{M} - \mathrm{DonM}}{L_1 L_2 - \mathrm{M}\text{^}2} & -\frac{L_1}{L_1 L_2 - \mathrm{M}\text{^}2} \\ -\frac{1 - \mathrm{Don}}{C_1} & -\frac{\mathrm{Don}}{C_1} & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & -\frac{1}{R_L C_2} \end{bmatrix}$$

6. System Open Loop Performance:

The system open-loop performance has been represented taking the system parameters as shown in table (1).The responses of the system with these parameters at three different loads are shown in the figures (3_a,b,c).

Table (1): Elements of the Modified Cuk Convertor.

Vs : Supply voltage	12 V		
Duty Cycle: (d)	0.5		
L_1 : First Inductance	2mH		
L_2 : Second Inductance	2mH		
M : Mutual Inductance	-1.6mH		
R_1 : Inductance resistor	0.01 Ω		
R_2 : Inductance resistor	0.01 Ω		
C_1 : First Capacitance	30µF		
C_2 : Second Capacitance	470µF		
R_L : Load resistance	2 Ω	10 Ω	45 Ω

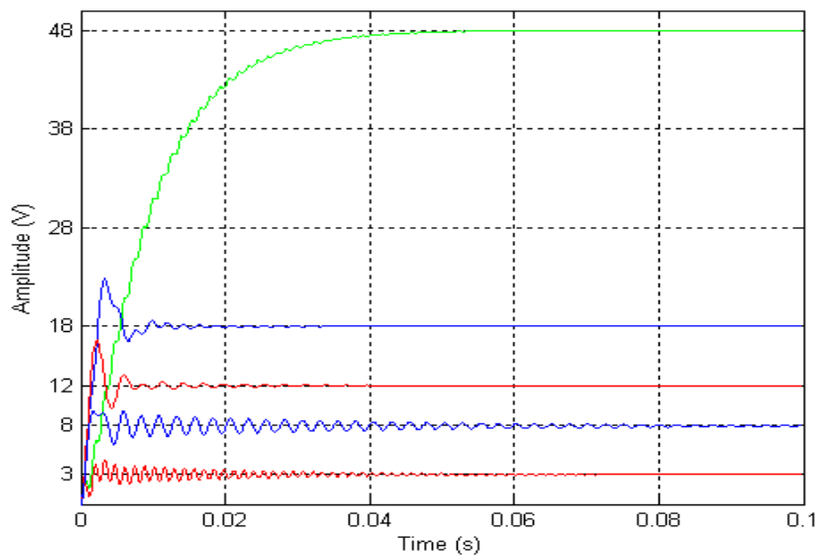

Figure (3.a): O/L Response at R_L= 2 Ohm.

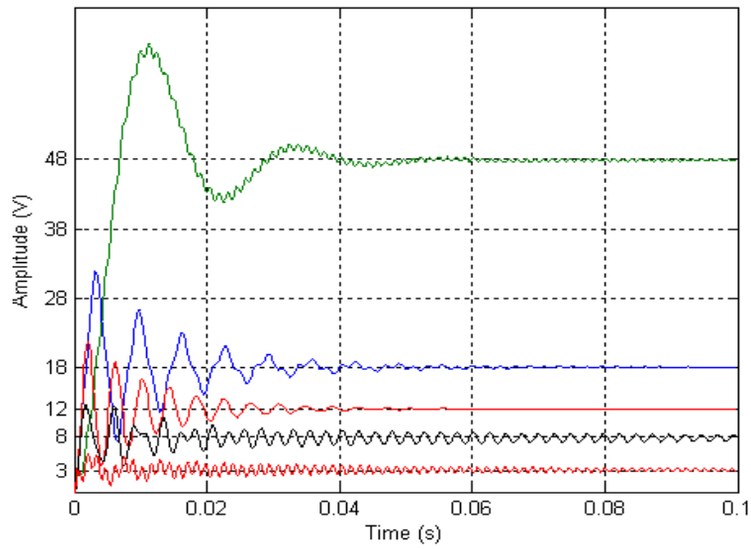

Figure (3.b): O/L Response at R_L= 10 Ohm.

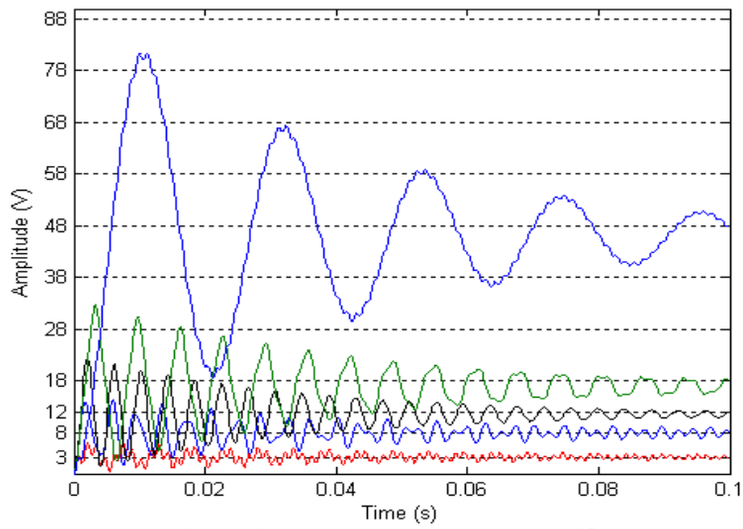

Figure (3.c): O/L Response at R_L= 45 Ohm.

7. Linear Quadratic Optimal Controller Design:

A traditional controller has been designed for the system in order to provide a background for evaluating the performance of the PSO controller to be designed.
The most general form for the quadratic criteria is:

$$J_{LQR} = \int_0^{\infty} x'Qx + u'Ru \qquad (7.1)$$

This controller has been designed by using the MATLAB/m.file programming, as follows:

```
Q=eye(4);
R=1;
K,U,V]=lqr(A,B,Q,R,N);
Ac=A-B*K
step (Ac,B,C,D)
```

The response of the closed-loop system with the LQR at the fifteen studied cases at the open-loop case are shown in the figure (3.1)and the closed-loop system response performance are listed in table (2.1).

8. Particle Swarm Optimization:

It is one of the very fast-spreading swarm intelligence optimization technique. It was invented by (Russell Eberhart) and (James Kennedy) at 1995. They inspired the principle of work from the social behavior of the individuals within the entire society as with the bird flocks and the fish schools. The theoretical basis is emerged simply from simulating the behavior of individuals (particles) in nature. It is that when a flock of birds flies looking for food, and each bird doesn't know where the food is, but it knows both the distance between it and the food, and between the entire flock and the food. In such a case, the best manner each individual may follow for getting the food is by following the nearest (best) individual in the flock. In the environment of the PSO each possible solution called "*particle*". Each particle in the "flock" will update its positions according to the private pest position. It may take (*pbest*). The global best position may be taken by a particle in the flock (*gbest*). This position updating will go ahead until reaching the desired position, which represents the best solution of the optimizer.[14] PSO differs from all the other evolutionary algorithms in the mechanism of updating its particles' positions, that it does not replace the elements of the (population) by other new produced elements.[15] Instead, it improves the performance of each element. This improvement take place by updating the positions of the particles according to the equation (8.1) or one of its improvements [16], this equation had been derived by Eberhart and Kennedy [14].

$$Vid = Vid + C_1 * RANDp*(Pid - Kid) + C_2 * RANDg*(Gd - Kid) \quad (8.1)$$

Where:

1. V: particle's velocity.
2. i : the sequence of the particle.
3. d : dimensions of the search space.
4. K : specific particle.
5. C1 : private constriction (learning) coefficient
6. C2 : global constriction (learning) coefficient.
7. RANDp : matrix of updating the particles' (private) speed.
8. RANDg : matrix of updating the swarms' (global) speed.
9. P : particle's (personal) best known position.
10. G: swarm's (global) best known position.

Many modifications have been being introduced since its invention, such as:

- Standard PSO:[14] It's the first version invented. Equation (8.1) represent this type.
- Weighted PSO:[15] This modification introduced by (Shi) and (Eberhart). They proposed a weighting inertia to slow down the convergence to the solution, in order to expand the ability of the optimizer to explore new zones of the search space. Equation (8.2) represent this type.

$$Vid = W*Vid + C_1 * RANDp*(Pid - Kid) + C_2 * RANDg*(Gd - Kid) \quad (8.2)$$

- Weighted PSO with Time-decreasing weighting Inertia:[16] This modification introduced by (Shi) and (Eberhart), they proposed a method to decrease the value of the weighting inertia from a starting maximum point to an ending minimum point. They aimed to equalize between the exploration and the exploitation of the optimizer.

$$W = Wmin + ((Wmax - Wmin) / (Max.iter))*(Current\ Iteration - 1) \quad (8.3)$$

This type of PSO is the one which has been used in this paper.

9. PSO Controller Design:

PSO is used to choose optimally the values of the state feedback controller gains for the system. The main features of the designed optimizer are as follows:

1. Number of Particles = 20 particle.
2. Decimal Encoding.
3. The initial values were chosen randomly, in the space interval between (0) and (1).
4. Fitness Function:[1] We used the principle of finding the integral absolute error (IAE) as a performance index to guide the search of the genetic algorithm, and attending to *minimize* this error during the selection and recombination of the mated individuals throughout all the generations.

$$IAE_{Min} = \int_0^T |e(t)|\, dt = \frac{1}{N}\sum_{k=1}^{N} abs(e_k) \qquad (9.1)$$

N: number of samples.

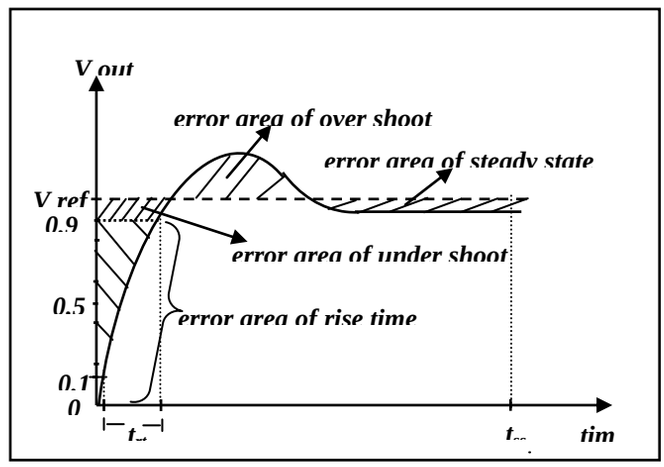

Figure (4) : the components of the fitness function.

5. $C_1 = C_2 = 2$. (positive and equal).
6. The PSO with Time-decreasing weighting Inertia were used, with maximum and minimum weighting inertia values more than 0.5, in order to pay more concentrate on the exploration, with making use of the essential equilibrium between exploration and exploitation produced by this method.
7. A three conditioned stopping criteria has been designed, as follows: stop the iterative computations if any three of the following four specifications have been realized, and take the particle realizes these results as the required (optimal) solution.

Condition(1): Steady state error = 0. Condition(2): Peak over shoot < 1%.
Condition(3): Settling time<0.0001 second Condition(4):Rise time<0.0001second.
If the condition did not meet, (END) after executing a specific number of generations.

10. Simulation Results and Discussion:

The responses of the system were taken for various values of loads (resistances) and different reference voltages. In order to check the performance of the optimizer at different operational situations. The figures (5_a,b,c), show the output signals at fifteen operating situations; three load resistances (2, 10 & 45)Ω with five reference voltages at each load consequently.

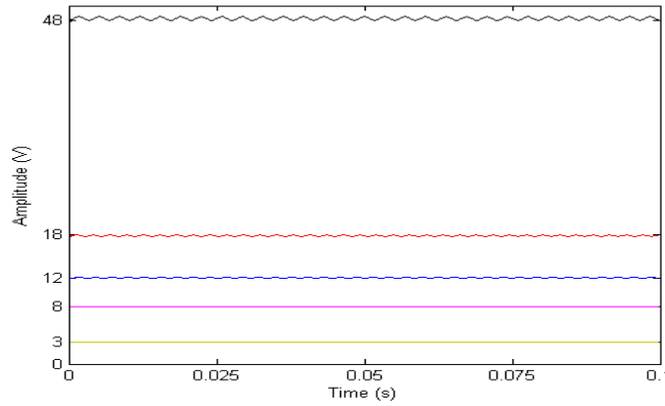

Figure (5.a): Closed-loop system responses with R_L = 2 Ohm and V_{ref} of: 3V, 8V, 12V, 18V, & 48V, consequently.

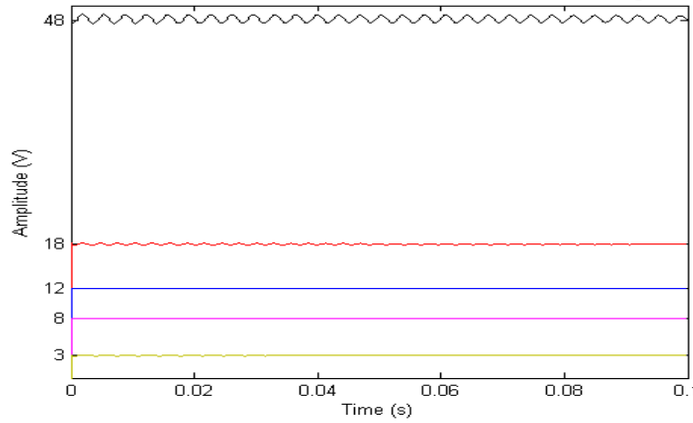

Figure (5.b): Closed-loop system responses with R_L = 10 Ohm and V_{ref} of: 3V, 8V, 12V, 18V, & 48V, consequently.

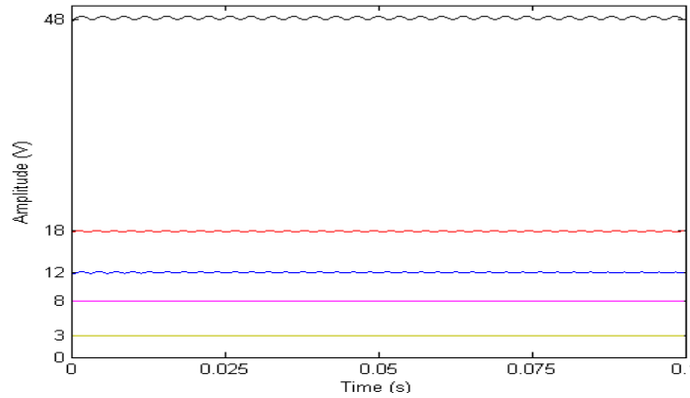

Figure (5.c): Closed-loop system responses with R_L= 45 Ohm and V_{ref} of: 3V, 8V, 12V, 18V, & 48V, consequently.

The closed-loop system response performance is listed in table (2) and table (3).

Table (2): System Performance with an LQR and a PSO controller at V_{ref} of: 3V,8V at three different loads (2, 10 & 45) Ω for each.

Vin=12V		Vref = 3V			Vref = 8V		
RL(Ω)	**Performance**	**(O/L)**	**LQR**	**PSO**	**(O/L)**	**LQR**	**PSO**
2	**Tr. (s)**	0.0016	0.0022	0.00008	0.0008	0.0017	0.00005
	Ts. (s)	0.0617	0.0073	0.00011	0.0752	0.0057	0.00007
	P.O.S (%)	50.3394	14.3535	0	19.1287	19.4344	0
	Elapsed Time(s)			24.55			24.15
10	**Tr. (s)**	0.0015	0.0015	0.00008	0.0007	0.0014	0.00005
	Ts. (s)	0.1682	0.0250	0.00010	0.1856	0.0149	0.00006
	P.O.V (%)	71.9688	42.5908	0	62.7130	34.9249	0.0861
	Elapsed Time(s)			10.33			11,87
45	**Tr. (s)**	0.0018	0.0015	0.00008	0.0006	0.0014	0.00007
	Ts. (s)	0.2463	0.0433	0.00010	0.3145	0.0168	0.00009
	P.O.V (%)	69.0139	48.7	0.6971	81.1840	36.3819	0.2907
	Elapsed Time(s)			9.37			37

Table(3): System Performance with a PSO controller at V_{ref} of: 18V, & 48V at three different loads(2, 10 & 45)Ω for each.

Vin=12V		Vref = 18V			Vref = 48V		
RL(Ω)	**Performance**	**(O/L)**	**LQR**	**PSO**	**(O/L)**	**LQR**	**PSO**
2	**Tr. (s)**	0.0020	0.0022	0.00006	0.0018	0.0062	0.00009
	Ts. (s)	0.0121	0.0025	0.00008	0.2463	0.0078	0.00012
	P.O.V (%)	26.9985	1.4432	0	69.0139	0	0
	Elapsed Time(s)			18			19.31
10	**Tr. (s)**	0.0014	0.0023	0.00007	0.0061	0.0066	0.00008
	Ts. (s)	0.0525	0.0026	0.00009	0.0451	0.008	0.00010
	P.O.V (%)	77.1583	1.1346	0.9804	35.1131	0	0.5234
	Elapsed Time(s)			11.92			16.39
45	**Tr. (s)**	0.0017	0.0023	0.00007	0.0050	0.0066	0.00007
	Ts. (s)	0.1746	0.0026	0.00009	0.1611	0.008	0.00010
	P.O.V (%)	92.6204	1.1458	0.5954	76.2821	0.0197	0.0501
	Elapsed Time(s)			15.2			16.94

Particle swarm optimization is an extremely simple algorithm that is effective for optimizing a wide range of problems and problem variations. The study of the results shows that there is a great enhancement, which involves the whole performance, as follows:

1. Peak over_shoot: its values were very high at the open loop system, with a great difference between the upper and the lower values for the different operational situations, table (2). The traditional controller didn't enhance the cases of reducing the voltage considerably. While, its values were too low with the PSO controller (realized the stopping condition p.o.s < 0.1%). Although the stopping criteria was set to suffice by the percentage of 1% of p.o.s, all the overshoots at 2Ω load and two at 10Ω were zeros. The maximum recorded p.o.s was (0.98 %) with consecutively low execution time. The difference between the maximum and minimum recorded p.o.s was too little as compared with the open loop one, but it is similar to it in that there is no distinct relation between the recorded value on one hand and the value of the load or the reference voltage on the other hand. Although the maximum p.o.s recorded at 45Ω load (0.7%) was at the maximum output, and the minimum one (0.05) was at the minimum output voltage, but this relation is not constant along the other intermediate loads. The maximum p.o.s was recorded with consuming a low execution time which is lower than four 2Ω cases , four 45Ω cases, but it is noticeable that the execution time at the cases of the same load was lower than the time of the

maximum p.o.s, at all the cases of the lower output voltage, without a considerable difference in the values of the rising and settling times.

2. Rising time: its values are between (0.0006) and (0.0360) second at the open loop cases with a great difference between these values according to both the duty cycle and the load. The closed loop cases with the traditional controller recorded values between (0.0014) and (0.0066) second. While, the recorded values by using the PSO controller were extremely better at all the cases, with a very tiny difference in the values recorded at the different situations. The maximum rising time at the closed loop system with the PSO controller was (0.00009) second, and the lower was (0.00005) second, with a maximum difference at the same output voltage with an alternating load does not exceed (3*10^-5) second, as shown in table (4).

Table (4): Maximum difference in the recorded rising time among three loads at the same reference voltage.

Output Voltage	3 (Volt)	8 (Volt)	12 (Volt)	18 (Volt)	48(Volt)
Max. difference in Tr. at the loads (2,10& 45)Ω. (second)	0 (stable at the three loads)	2* 10 ^ -5 (increases with the load)	3* 10 ^ -5 (decreases with the load)	1* 10 ^ -5 (increases with the load)	2* 10 ^ -5 (decreases with the load)

3. Settling time: it increases at the open loop system by increasing the load at the same output voltage, with a maximum recorded settling time of (0.3145) second at (45)Ω and (8)volt output voltage, and a minimum value of (0.0121)second at (2)Ω and (18) volt output voltage.(i.e. great difference between the maximum and minimum values). It improved by using the traditional controller to record values between (0.0025) and (0.0433) second. While, the worst recorded settling time at the closed loop system with the PSO controller was (0.00012) second which indicates a very great enhancement at the performance of the system. In addition, the difference between the minimum and maximum settling times along the fifteen cases doesn't exceed (4*10^-5) second, as shown in the table(5) with the advantage that the system overcame the problem of increasing settling time by increasing the load. This problem disappeared at the closed loop system.

Table (5): Maximum difference in the recorded settling time among three loads at the same reference voltage.

Output Voltage	3 (Volt)	8 (Volt)	12 (Volt)	18 (Volt)	48 (Volt)
Max. difference in Ts. at the loads (2,10& 45)ohms. (second)	1* 10 ^ -5 (decreases with the load)	3* 10 ^ -5 (increases with the load)	4* 10 ^ -5 (decreases with the load)	1* 10 ^ -5 (increases with the load)	2* 10 ^ -5 (decreases with the load)

4. The elapsed times at the computational processing operations have the advantage that it doesn't waste a large time to obtain the optimal solution (24.55 second maximum).

Conclusion:

A mathematical representation for the modified Cuk convertor was derived. The open loop response was taken at fifteen operational conditions of three resistance loads and fife reference voltages for each. The study of the open loop performance showed that there were disadvantages related with the peak over_shoot which recorded 93.2 % in a certain operational condition and a high rising and settling time which were (0.0360 & 0.3145)

second consequently in two different operational conditions. In addition, the open loop performance suffered from the obvious load dependence drawback. A state feedback controller has been designed by using a traditional algorithm, then by using the particle swarm optimization for improving the performance of the system. The weighted PSO with time-decreasing weighting inertia was used for optimally choosing the state feedback gains for the system. Further testing and verification for the implementation of a PSO intelligent controller upon the electronic Cuk voltage converter was introduced in this article. The simulation results showed that the proposed control technique succeeded in improving the response of the system for a wide range of operational conditions, and that the PSO controller is considerably better than the traditional controller. That the peak over_shoot didn't exceed 0.98% in all the operational conditions. Rising time and settling time didn't exceeded (0.00009 & 0.00012) second. Also, the responses' values showed a great stability at the different cases that the difference between the higher and the lower values was too small. The drawback of the load dependency was eliminated by using the proposed controller. Finally, the proposed controller didn't waste a long time for finding the various solutions

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ANN-Based Speed Control Of DC Motor Using FPAA

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Abstract

In this work a field programmable analog array (FPAA) has been implemented in building and constructing the artificial neural network (ANN) controller system via programming using anadigm Designer 2 simulator software. The constructed ANN controller was used to control the speed of separately excited dc motor which rotating a dc generator coupled together. The controller effect has a control on both armature voltage and armature current of the dc motor to reject load effect that has been applied on the dc generator as electrical load. The realized ANN controller has been built in analog devices utilizing the facilities belong to the chosen FPAA where the proposed control system is totally in the analog domain signal processing. The analogue ANN was trained successfully using supervised learning rule like single layer perceptron learning rule and delta learning rules. The results show good fulfillment of a ANN with FPAA Chip and verifying the learning rules to train network. This has the advantage of producing simpler systems over those in digital microcontrollers.

Keywords: Analogue neural network, BP learning rule, FPAA Chip, Perceptron learning rule and software anadigm designer 2.

اعتماد الشبكة العصبية الاصطناعية على التحكم بسرعة محرك التيار المستمر باستخدام شريحة المصفوفات التناظرية القابلة للبرمجة حقلياً

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ألمستخلص

في هذا البحث تم استخدام شريحة المصفوفات التناظرية القابلة للبرمجة حقلياً(FPAA) لبناء وتركيب مسيطر الشبكات العصبية الاصطناعية(ANN) من خلال برنامج المحاكاة Anadigm Designer 2. استخدام شبكة ANN بوصفها كمسيطر للتحكم بسرعة محرك التيار المستمر منفصلة الاثارة والتي تعشق محوره مع محور دوران مولد التيار المستمر لأجل التحكم في مقدار الحمل المسلط على المحرك. وان مسيطر ANN المقترح يسيطر على كل من فولتية المنتج وتيار المنتج للمحرك لأجل رفض تأثير الحمل المسلط عليه (الحمل الكهربائي) من خلال مولد التيار المستمر المعشق مع محوره. تم تحقيق وبناء مسيطر شبكة ANN المقترح باستخدام الدوائر التناظرية في شريحة FPAA دون غيرها لأنها تتعامل مع معالجة الاشارات في الحيز الزمني او الحيز التناظري. تم تدريب شبكة التناظرية ANN بنجاح باستخدام قوانين التعلم بإشراف مثل خوارزمية بيرسيبترون وخوارزمية التعلم الانتشار العكسي. إذ تبين النتائج بأن أداء الشبكة التناظرية المحققة في شريحة FPAA احسن وأكفأ من الشبكة العصبية المحققة في المتحكمات الرقمية.

1- Introduction

The neural network is an intelligent technique which can be used as a Controller, and can be applied in signal processing, signal conditioning and signal recognition fields. It may be implemented and realized by different methods, one of them is the digitally which realized by high level Software like MATLAB, another method is by analogue which can be realized by using reconfigurable operational amplifier in FPAA.

A field programmable device has taken another recent direction that is the Field Programmable Analog Arrays (FPAA).It is Similar to the FPGA, but The FPAA is a programmable integrated circuit that can be used to implement analog circuit functions in many applications. In general the FPAA is an array of identical Configurable Analog Block(CAB) which includes operational amplifiers, comparators, filters and switched programmable capacitors. The FPAA can be programed to perform a basic programmable analog electronic circuit (like filters or PID controllers..) devices or elements constructed by configurable Analog Blocks (CAB).The advantages of this programmable IC, it is more efficient, and economic than using individual op-amps, comparators and discrete components. By choosing suitable instruction in programming facilities it can be used to change component values and interconnections, It has more benefits like, fast changes can be made in FPAA while they are operating in a system [1]. Anadigm's FPAAs introduces the ability to translate complex analog circuit to a simple set of low-level function, and thus gives designers the analog equivalent of FPGA. FPAAs are based on switched-capacitor technology. Switched capacitors take the place of resistors in switched capacitor circuits. An effective resistance can be defined for switched capacitors; its value depends on the capacitance but changes according to the sampling frequency. The designer can design complex analog design, test and modify the design and finalize them in few hours using FPAA technology. Currently, FPAA's are available and can be configured in real time that allows the designers to modify their analog design in real time[1].

Anadigm's FPAA elevates the design and implementation process of analog design to high levels of abstraction. Dynamic configurability adds to these capabilities by allowing analog functions to be updated in real time using automatically generated C-code. With analog functions under the control of the system processor, new device configuration can be loaded on the fly, allowing the device's operation to be "time-sliced," or to manipulate the tuning or the construction of any part of the circuit without interrupting operation of the FPAA, thus maintaining system integrity [2].

The literature on the implementation of the FPAA are with different applications .The authors of paper [1] mainly deal with the design of path-tracking robot with movable arm using a field programmable analog array technology in addition to other necessary supporting electronic circuits. An FPAA based controller is designed to control a path tracking robot. Two methods were applied; the first method was a conventional PI controller, while an ANN controller was presented in the second method. The ANN performance was evaluated by comparison with the PI controller. They concluded practical results that the ANN controller is more sensitive due to its fast response to correct the error with that of the conventional PI controller. Besides it was observed that robot motion with ANN controller was smoother than that with PI controller, especially at the bent tracks.

The work presented in [3] explores description and the design, simulation, and hardware implementation of self-tuning PID controller based on FPAA for DC motor speed control and it was successfully realized. The FPAA provides flexible, easy and fast circuit modification, comparatively low cost for a complex circuitry and rapid. Practically proved that it provides a fast response with high accuracy of control. A genetic algorithm(GA) implemented in Visual

C++ language for self-tuning PID controller. The GA has been used online as an active method to solve the problem of finding the accurate gain values of the PID controller.

In this work, Anadigim field programmable analog array (FPAA) technology has been implemented and programmed in building the artificial neural network (ANN) controller system utilizing simulator software (Anadigm Designer 2) to control speed of the separately excited DC motor driving a DC generator. In addition the built ANN controller controls both the armature voltage and armature current for the dc motor to attain a reject of load applied to DC generator mounted to DC motor rotating shaft.

2- The Anadigm Product Of FPAA

Anadigm offers dynamically programmed Analog Signal Processors and development systems that share the same input/output structure. The development kit is ideal for development and prototyping in conjunction with AnadigmDesigner2 software. This type of FPAA includes AN231E04, AN220E04 and AN221E04.

Anadigm also offers statically reconfigurable FPAA that shares the same input/output structure and requires a reset before loading a new configuration bit stream. This type of FPAA includes AN120E04, AN121E04 and AN131E04 [4].

3- AN221E04 Overview

A typical package and block diagram for an AN221E04 FPAA are shown in Fig. 1.

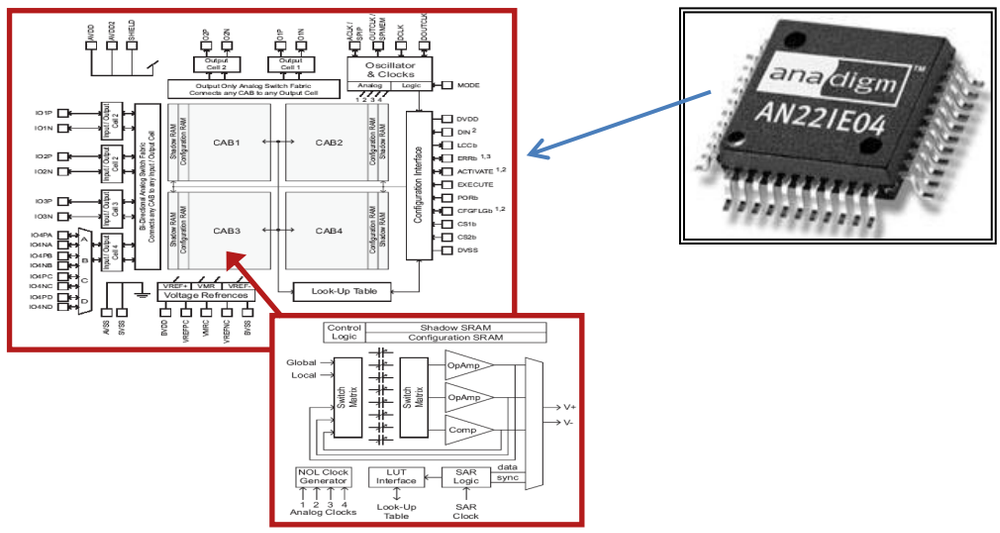

Fig. (1): Device package and block diagram of the AN221E04

This device has four CABs arranged in a 2 x 2 matrix and includes the associated logic and other resources for initial programming and reconfiguration. When you program the FPAA, the data goes into the on-chip random-access memories (RAMs) associated with each CAB via the configuration interface. These memories allow reconfiguration data to be loaded while the old configuration is active and running. The shadow RAM stores the new configuration data without disturbing the current configuration until the proper time for it to be transferred into the configuration RAM, which stores the current configuration data. This permits any changes or adjustments in circuit design to be accomplished while the FPAA is

operating in a system without disturbing the system operation. This is called dynamic reconfiguration. Configuration data can be generated from a computer running the development software when the FPAA is initially programmed. Data for configuring the device can also be generated from an external EPROM that stores the configuration program, or reconfiguration can be controlled by a microprocessor, called a host processor, embedded in the system in which the FPAA is operating. The FPAA device can generate its own clock for internal timing, or it can accept an external clock signal. DC voltages can be generated internally for use in certain types of circuits that require reference voltages. The look-up table (LUT) in the FPAA is a type of memory that stores data for certain predetermined configuration functions. It contains storage space for 256 bytes of data. Each byte of storage space has a specific address that uniquely defines it. Analog input signals are connected to the device with the configurable input/output (I/O) cells. Output signals can also be routed through the input/output cells. An I/O cell can accept a differential or common-mode input signal and can contain a programmable filter and amplifiers for improving input signal quality [5]. There are four CABs in the AN221E04 device. A circuit design is programmed into the CABs using development software with a library of analog functions, such as integrators, differentiators, filters, comparators and other types of circuits as shown in Fig. 2.

4- FPAA Architecture

The programmable features of an FPAA include the CAB, the interconnection network and the input/output (I/O) blocks. A typical CAB consists of one or more op-amps, a bank of capacitors, and an array of switches, as indicated in Fig. 1.

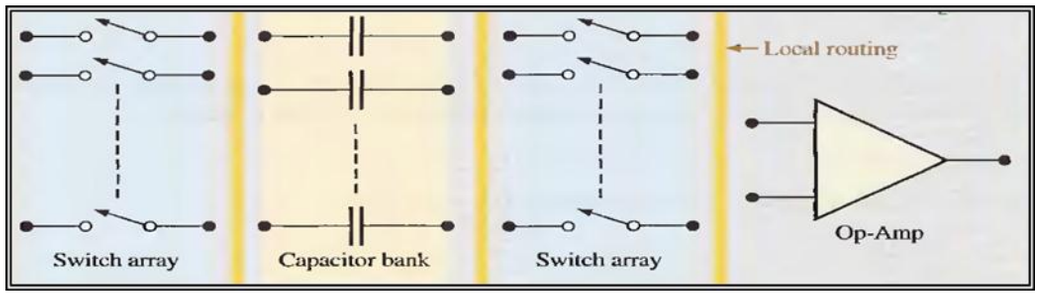

Fig. (2): A simplified CAB block diagram with MOSFETs switches[1]

The interconnection network includes global routing, which connects to other CABs and to the outside world, and local routing, which connects within the CAB. Using these features, many analog functions (such as amplifiers, integrators, differentiators, and filters) that can be made with individual op-amps and conventional passive components (resistors and capacitors) can be implemented at a lesser cost, in a much smaller size, and with increased reliability and component stability. All FPAAs require a software development package that allows you to enter an analog circuit design on your computer, test it by simulation, and download it to the FPAA chip using a standard interface.

The programmable CABs and the interconnection network are controlled by on-chip clock sources, a memory, a shift register, and other logic. The software program performs the necessary operations to add the required analog functions, to make appropriate interconnections, and to properly configure the switched-capacitor networks to produce circuit values and parameters for achieving specified performance characteristics in the FPAA device [6]. Switched-capacitor circuits are used in FPAA arrays to implement various analog circuits on an IC chip using only capacitors. A capacitor can be implemented on a chip more easily than a resistor. Capacitors also offer other advantages such as no power dissipation.

When a resistance is required in a circuit, a switched capacitor can be made to emulate the resistor. Reprogramming switched-capacitors can readily change resistor values and more accuracy and table resistance can be achieved. The resistor (R) value can be given as [7].

$$R=T/C \quad (1)$$

This equation shows that the effective emulated resistance is directly related to T (time) and inversely related to C (capacitance value). In an FPAA, the switching frequency (f) is a programmable parameter for each emulated resistor and is selected to achieve a precise resistor value . Since T = 1/f, the resistance in terms of frequency is:

$$R=1/(f\,C) \quad (2)$$

Typically, switched-capacitor circuits implemented in an FPAA consist of MOSFET switches as shown in Fig. 2. Their ON and OFF times are controlled by timing signals with frequencies that are programmable. The two timing signals that turn the MOSFETs ON and OFF are square waves that are 180° out of phase so that when one transistor is ON the other will be OFF and vice versa, with no overlap. Fig. 3 shows the switched-capacitor implementation for the input resistor [7].

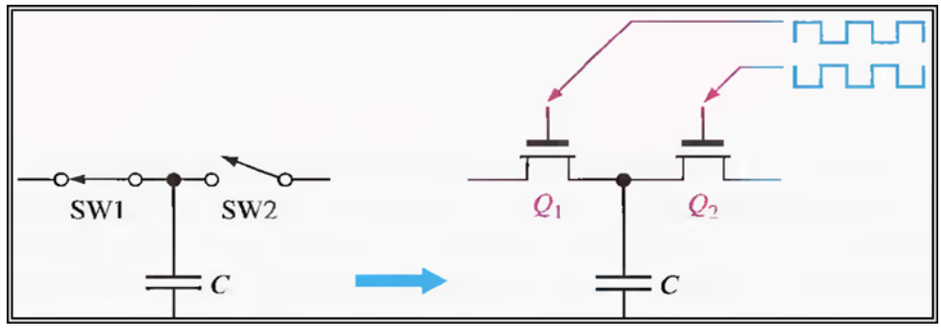

Fig. (3): A switched-capacitor with MOSFET

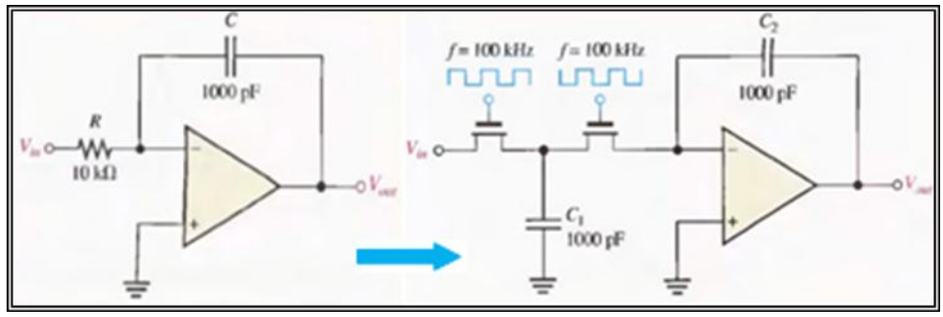

Fig. (4): Amplifier with switched-capacitor emulation of input resistor

Feedback resistors, such as those used in differentiators, inverting and non-inverting amplifiers and certain types of filters, require a variation in approach. The switched-capacitor implementation for the input resistor used in the integrator of Fig. 3 is impractical for emulating a feedback resistor of the op-amp in Fig. 4-a. Because the two transistor switches can never be ON at the same time, the feedback path would never be closed and proper operation would be presented. To avoid this, the switched-capacitor configuration for the feedback loop in the amplifier in Fig. 4-b can be used. Q1 and Q3 are ON at the same time. Q1 allows C1 to charge to the input voltage and C2 discharges through Q3. When Q2 turns ON the sampled input voltage stored on C1 is applied to the input of the op-amp and charges C2.The voltage gain is [7]:

$$Av = -\frac{R_f}{R_i}$$

$$Av = -\frac{\left(\frac{1}{f C_2}\right)}{\left(\frac{1}{f C_1}\right)} = -\frac{\left(\frac{1}{C_2}\right)}{\left(\frac{1}{C_1}\right)}$$

$$Av = -\frac{C_1}{C_2} \qquad (3)$$

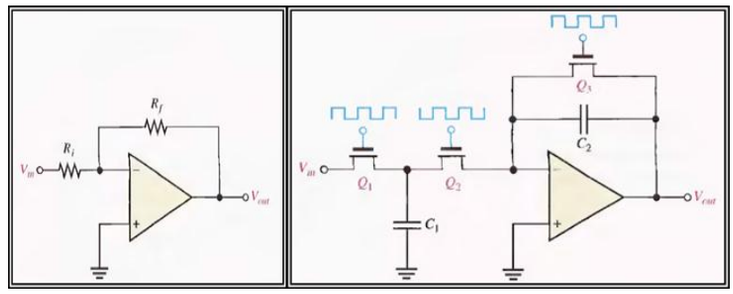

Fig. 5: Amplifier with switched-capacitor emulation of input and feedback resistors.

5- Programming With A Specific Development Software

Development software is provided for entering a circuit design on the computer, simulating the design to make sure that it operates as expected, and downloading the design to the FPAA chip. A flow chart showing the general programming procedure is given in Fig. 6 [4]. An excellent example of FPAA development software is the Anadigm Designer 2.

This software provides the selection, placement, wiring and simulation of one or more sub circuits called CAMs. The CAMs are the "building blocks" for analog designs and are pre-constructed analog functions that can be adjusted for desired parameter values.

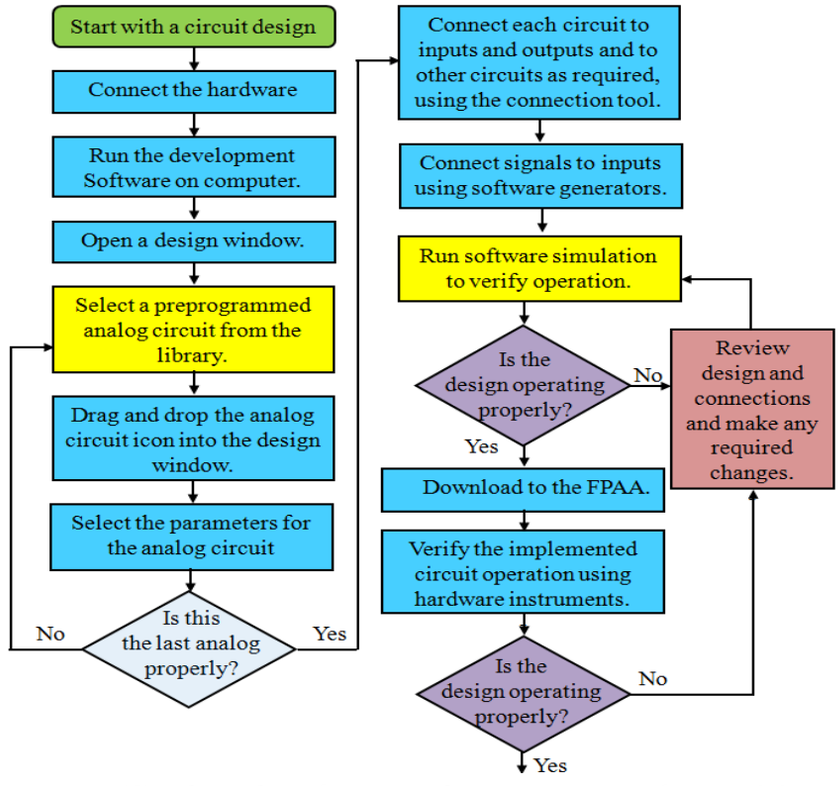

Fig. (6): Flow chart for general programming of an FPAA

6- Realization Of Ann In FPAA

To explain how to realize and implement ANN in FPAA chip via Anadigm Designer 2 software, as an example , the ANN based on XOR gate has been realized in AN221E04 FPAA chip, then the ANN with size (2-1) has been trained in computer via MATLAB program, the weights and biases of this ANN has been produced after training network in MATLAB, then introducing these weights and biases via Anadigm Designer 2 software to the reconfigurable component in FPAA chip such as gain invertor(Gaininv) and summer device(SumIntegrator) as shown in Fig. 7, it represents the output of this analog ANN when both inputs are similar and different.

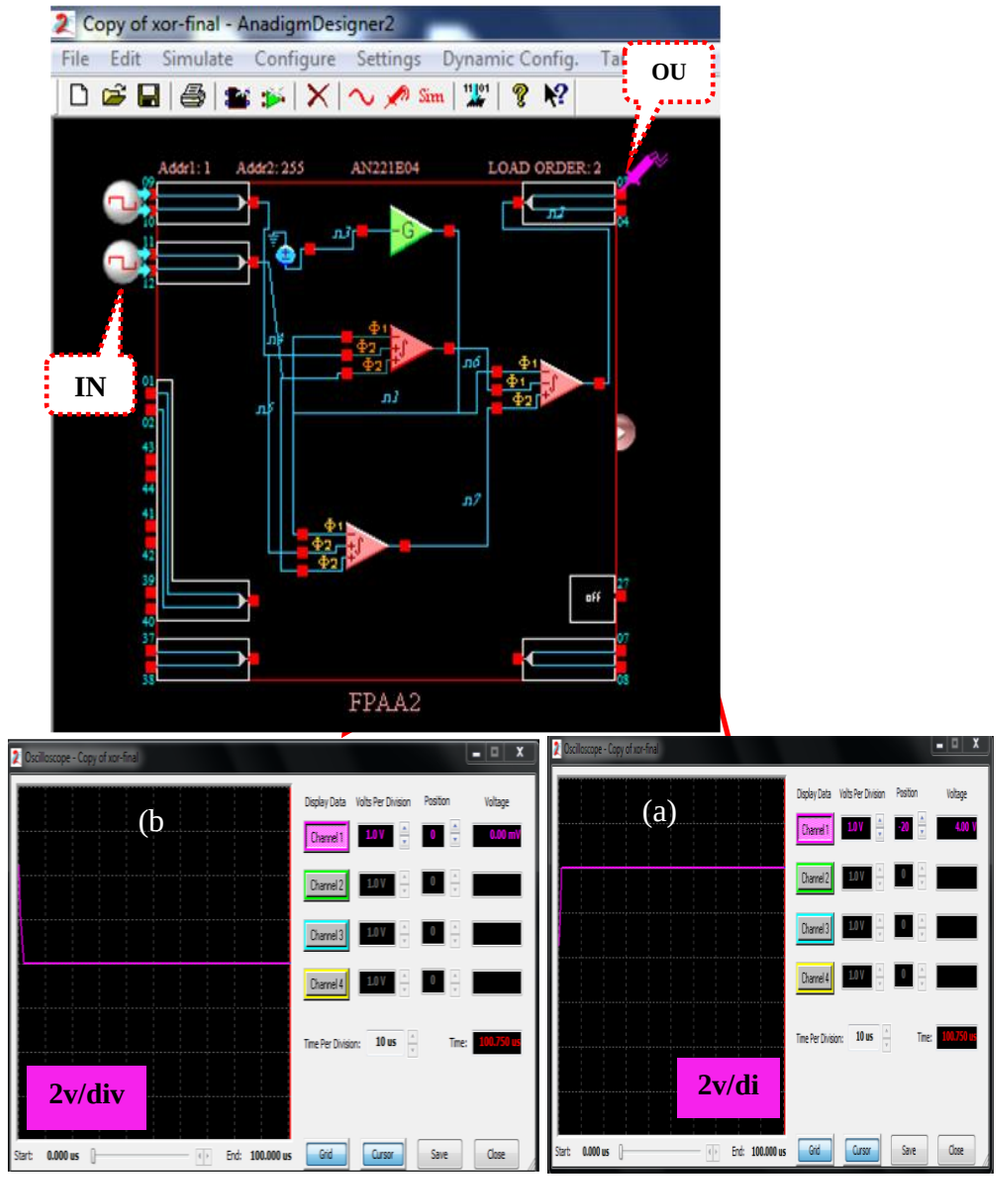

Fig. 7: Single layer artificial neural network(ANN Like XOR gate)
(a) Output the ANN when inputs are different
(b) Output of the ANN when both inputs are similar.

The ANN Like XOR gate has been realized by the reconfigurable analog hardware devices such as operational amplifier and implemented in AN221E04 FPAA chip by downloading this design which was constructed via Anadigm Designer 2 software as shown in Fig. 8.

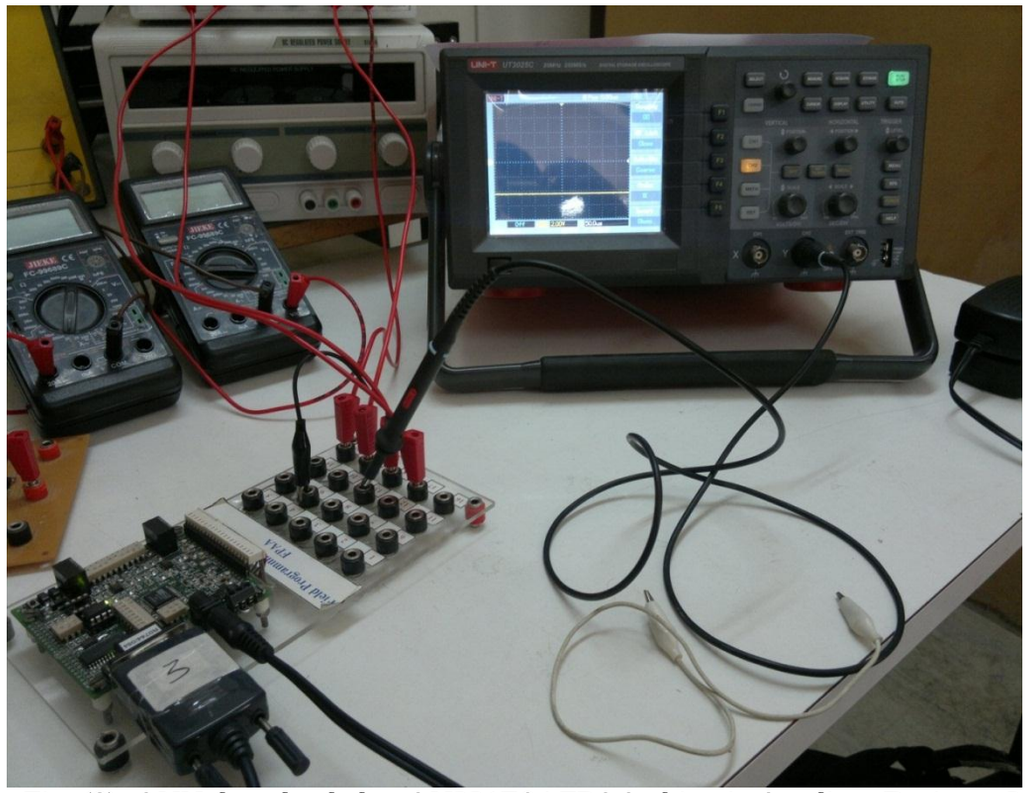

Fig. (8): ANN downloaded to AN221E04 FPAA chip via Anadigm Designer 2

Practically, Fig. 9. represents the ANN based on XOR gate has been realized and implemented in FPAA board via Anadigm Designer 2 software, Fig. 9-a shows the output of this network when both inputs(two inputs) are the same value, and Fig. 9-b represents the output when the inputs for this ANN are different values.

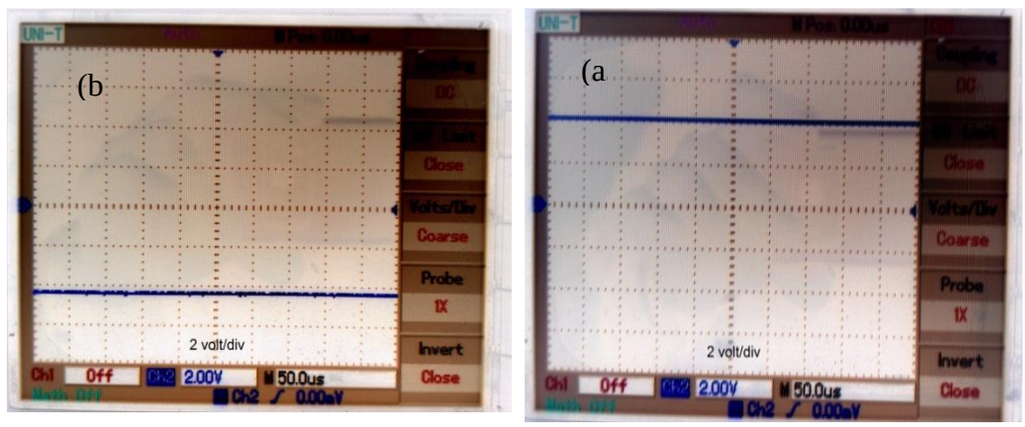

Fig. (9): ANN Like XOR gate implemented practically in FPAA chip

a) Output the ANN when inputs are different values
b) Output the ANN when both inputs are similar values

The sigmoid neuron activation function(NAF) for any analog neural network has been realized and implemented practically in AN221E04 FPAA chip via Anadigm Designer 2 software by using look up table(LUT) within size 256 Byte inside each FPAA chip to store data. This is shown in Fig. 10.

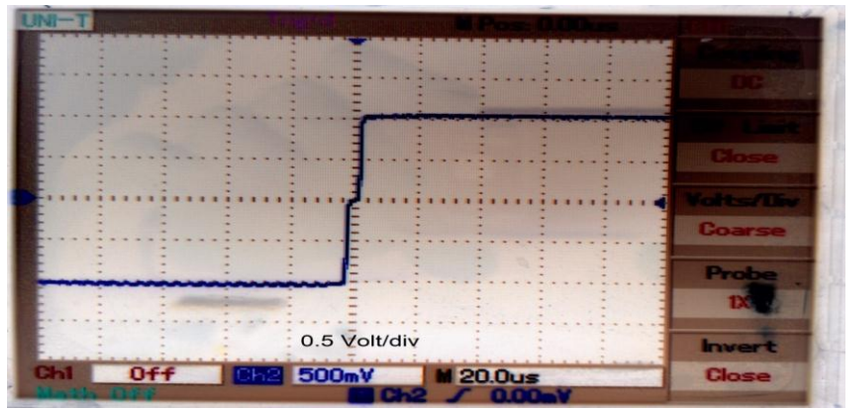

Fig. (10): Sigmoid NAF

Fig. 11. represents the ANN within size(5-1) has been realized via Anadigm Designer 2 software in seven FPAA board to speed control of separately excited dc motor.

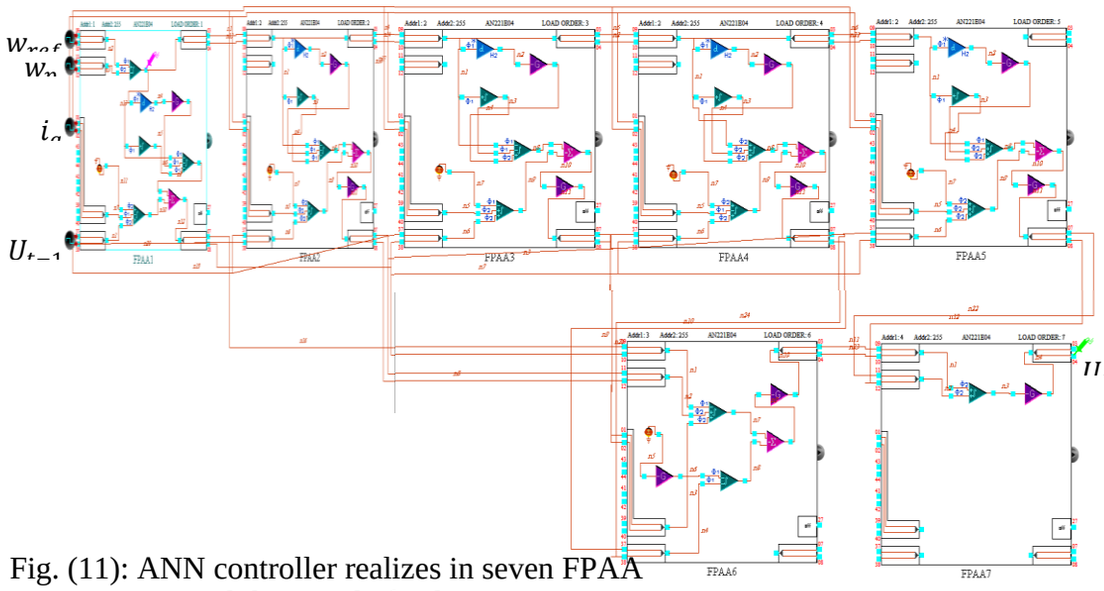

Fig. (11): ANN controller realizes in seven FPAA to control the speed of a dc motor

In order to verify effectiveness of the proposed control system, The previous analog ANN was implemented digitally in computer via data acquisition card (DAC) utilizing GUI monitoring in MATLAB program[8]. Then comparing between the performance of analog ANN which has been realized in FPAA and the performance digital ANN which has been realized in computer via DAQ. Fig. 12. shows the Photograph of the overall experimental system.

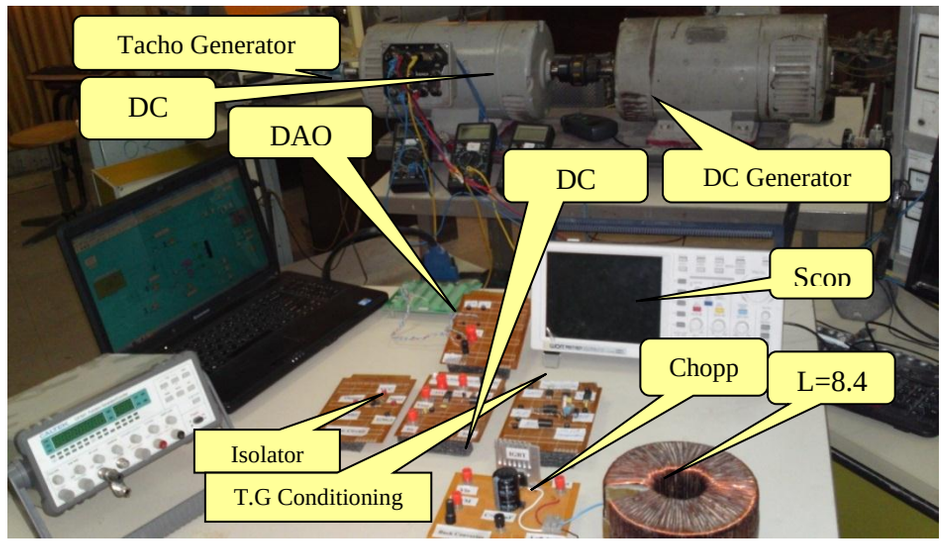

Fig. (12): Photograph of the overall experimental control

The block diagram shown in Fig. 13 represents the overall experimental control system to control the speed of a dc motor by using digital ANN utilizing DAQ card. The GUI monitoring has been designed in MATLAB program to observe or to control speed of dc motor via DAQ card utilizing ANN controller as shown in Fig. 14.

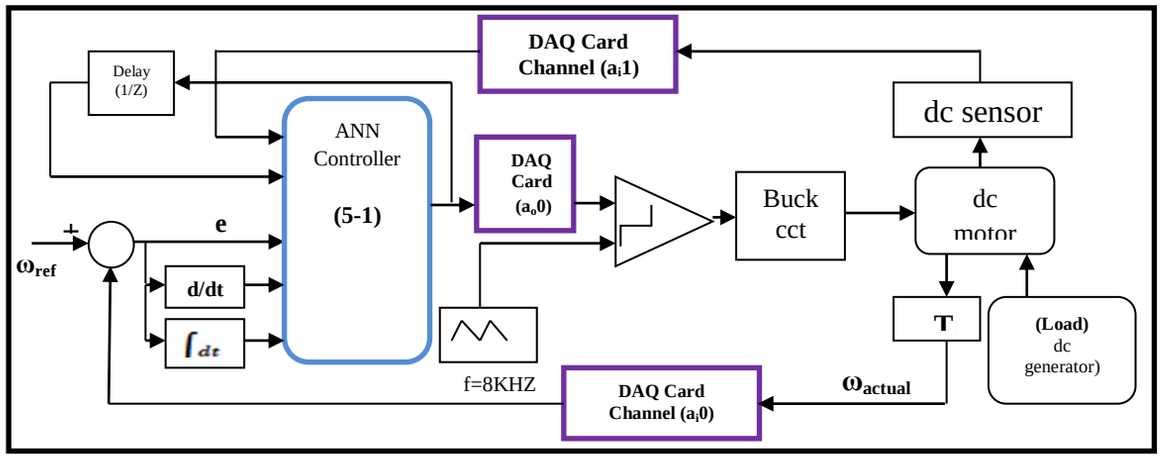

Fig. (13): Block diagram of closed loop control system by using ANN controller with size(5-1)

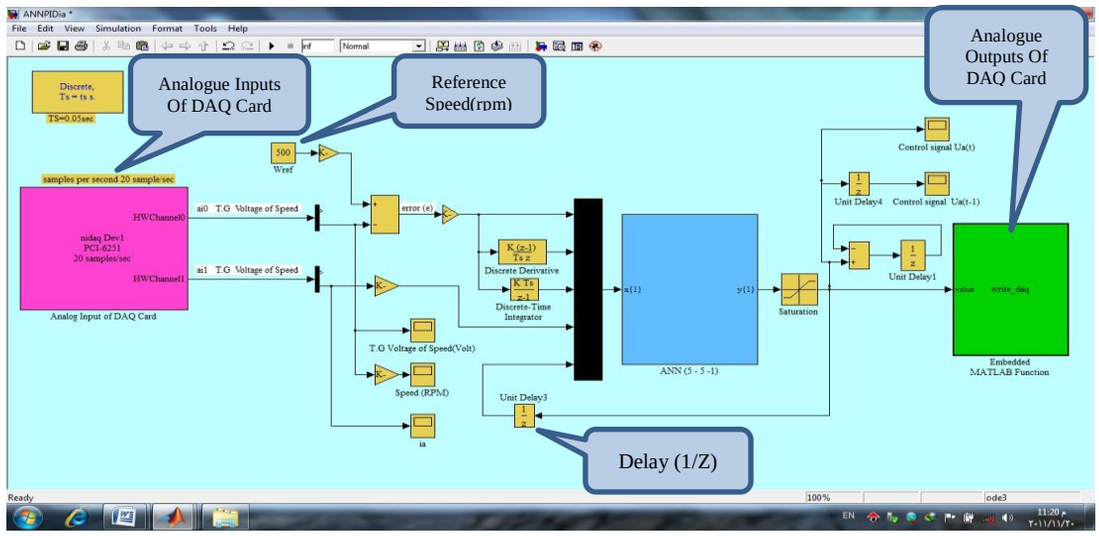

Fig. (14): GUI monitoring design in MATLAB program to control speed by using ANN

7- Results And Discussion

In order to train the analog ANN realized by FPAA. The digital ANN controller which has been designed for speed control of dc motor connected as an open loop without controller. Then the measured samples of data for different setting speed values of dc motor has been recorded in open loop connection, these values are shown in table 1.

Table (1): A samples from data for work behavior of practical control system

Motor Speed (rpm)	Armature Voltage (Volt) (V_a)	Armature Current (A) (I_a)	Tacho Generator Voltage (Volt)	dc level form PC (DAQ)	Duty ratio %	Apply load through dc Generator (A)
250	32	0.72	2.42	0.575	14	0
500	68	0.77	3.1	0.97	22	0
750	100	0.785	4.2	1.47	31	0
1000	134	0.8	5.3	1.9	39.5	0
1250	166	0.85	6.8	2.45	50	0
1500	208	0.88	8.1	3	61	0
500	78	2.1	3.5	1.2	28	2
1000	166	2.35	5.84	2.2	45	2

Practically, the response of the closed loop control system by using ANN controller when reference speed is 500 rpm with applying a load to the motor acting on dc generator about 2A as shown in Fig. 15. Then we have observed a reject of load effect to dc motor motion. Fig. 16 shows the control signal taken out from computer via DAQ card to drive dc motor through buck convertor circuit.

Fig. (15): Speed response of dc motor by using ANN controller

Fig. (16): Control signal U_a produced from control unit(computer) via DAQ card

Fig. 17 as represents the control signal (U_a) taken out from ANN control unit which was designed and constructed from seven FPAA board as shown in Fig. 11 via Anadigm Designer 2 software to speed control of dc motor.

Fig. (17): Control signal (U_t) output from seventh FPAA was realized in Anadigm Designer 2 to control the speed of a dc motor

8- Conclusions

The ANN can be implemented and realized like reprogrammable operational amplifier in FPAA chip which is not very expensive devices and available anywhere. The practical circuit has been built in this work for very simple five input neural network, where only one chip of operational amplifiers and a little component are used. This network is useful and easy so it can be implemented generally for any neural network. This work describes the design, implementation and performance for control speed of the separately excited dc motor using a field programmable analog array technology in addition to other necessary supporting electronic circuits. The AN221E04 FPAA chip is chosen to build the proposed control system because the signal processing is totally in the analog domain. This has the advantage of producing simpler systems than those in digital domain. The speed of the DC motor is used as a feedback and according to the difference between the set point speed and the present speed the error signal will be calculated. Depending on the error signal the ANN controller will make a decision if this error is low and acceptable or not. The output signal of the ANN controller will change the duty cycle of the PWM, which is given as switching pulses to the buck converter. The FPAA provides the capability for interfacing with PC for the execution of modern intelligent algorithms and implementing complex systems in analog manner. Some thoughts can be suggested either to develop this work or to make it more useful in other fields. Such thoughts can be implemented Speed and direction control of rotation of dc motor by FPAA based PID controller with H-bridge circuit.

9- References

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Hybrid Genetic Algorithm/Bacterial Foraging Techniques Based Single Phase Induction Motor Speed Control

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Abstract

This paper deals with the analysis and design of a speed controller for the single phase induction motor. It uses an evolution programming based on hybrid genetic algorithm bacterial foraging techniques. The proposed technique is used to minimize the error area for the output response. A variable–voltage, variable-frequency (VVVF) control scheme is used (voltage-frequency control strategy) to obtain wide range of speed variations. The controller provides optimize voltage-frequency supply to single phase induction motor through drive circuit. The analysis and simulation results obtained show that the proposed controller designed reduces the computation time in design of speed controller compared to genetic algorithm for same conditions, and it gives a very satisfactory response performance.

Keywords: Bacterial Foraging (BF), Genetic Algorithm (GA), Single Phase Induction Motor(SPIM).

السيطرة على سرعة محرك حثي أحادي الطور بتهجين تقنيتي الجينية وتغذية البكتريا

د. علي حسين أحمد **محمد عبد الجليل سلطان**

الخلاصة

يتناول هذا البحث تصميم وتحليل مسيطر سرعة محرك حثي احادي الطور باستخدام البرمجة المتطورة بالاعتماد على تهجين الخوارزمية الجينية – تغذية البكتريا .التقنية المقترحة تم استخدامها للتقليل من مساحة الخطأ لاستجابة الاخراج .تم استخدام التحكم على الفولتية – التردد المتغير (VVVF) للحصول على مدى واسع من السرع المتغيرة. المسيطر يوفر افضل فولتية– تردد لتغذية المحرك الحثي الاحادي الطور خلال دائرة المسوق. نتائج التحليل والمحاكاة تظهر بأن المسيطر المقترح المصمم يقلل من الوقت اللازم للحساب في تصميم مسيطر السرعة مقارنة بالخوارزمية الجينية لنفس الظروف. وانه يعطي اداء استجابة مرضية للغاية.

1-Introduction

In last few decades, evolutionary algorithms strategies were being used for optimization of various engineering problems. In control systems they were used for reducing the effects of adverse conditions, uncertainties and performance parameters such as: stability, rise-time, overshoot, settling time, steady state tracking etc. Most of the processes are complex and nonlinear in nature, then resulting in poor performance response control by traditional techniques. Single phase induction motors as one of the common systems are widely used in domestic and industrial application (washing machines ,clothes dryers, garbage disposals etc.)[1]. Due to their ruggedness, reliability, low cost and ease electrical installation . Most of the above applications are requiring variable speed drives .In which a single phase induction motors are normally used. The speed of AC squirrel cage motor can be controlled by two methods either by changing the frequency of the supply or its voltage. There are many research works which were dealing with the speed control of such a motor. Each one used a different techniques for example [2] has used Cycloconverter to control the speed of SPIM by applying variable frequency the control system is construct through design calculation to drive the motor in open loop control, the paralleled single phase induction motors driven by VSI based fuzzy was applied by[3] to control the speed of this type of motors .The evolution programming techniques were used by[4] to control SPIM based Frog-Jumping algorithm technique to track the reference speed[5]. Has use Variable voltage-frequency control to drive motor by SHEPWM inverter. The enhancement of conventional genetic algorithm is investigated by[6,7,8] for improving the learning and speed of convergence of the optimization in control system engineering by hybridization with bacterial foraging algorithm .The genetic algorithm used to estimate the parameter of fuzzy PID controller to control the speed of three phase induction motor[9]. The present work proposes a direct hybrid GA-BF technique that mentioned in[6,7,8] to control the speed of SPIM due to lack research works in the field of speed control for this type of motors.

2-System block diagram

The system block diagram is shown in Fig.1. It consists of power converter, single phase induction motor, and controller .

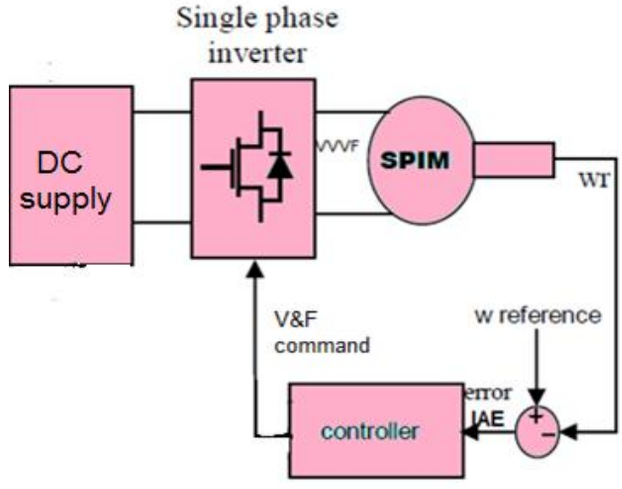


Fig. (1): System block diagram

2-1 Power converter

The power converter consists of DC supply which provide constant voltage level to the inverter from rectifier or battery. The inverter controls the voltage and frequency of the motor supply and feeds the SPIM. The power circuit topology of a single phase full bridge inverter is shown in Fig. 2.

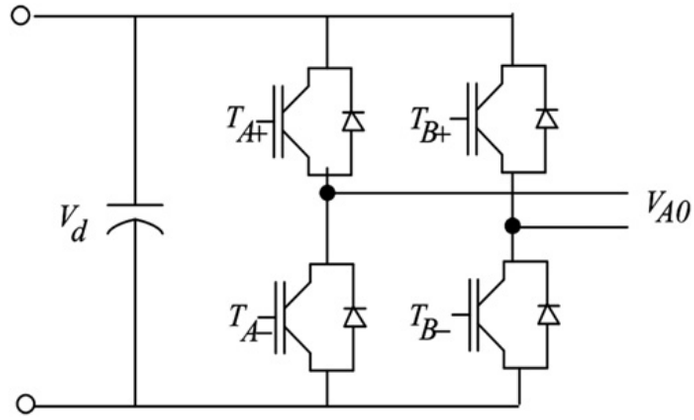
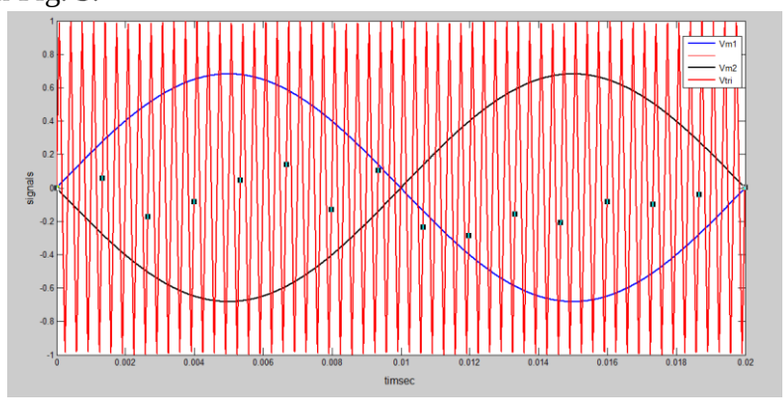


Fig. (2): Single phase inverter

The SPWM technique has been implemented in full bridge inverter by comparing modulating signals with the high frequency triangular carrier wave. The fundamental frequency of the output is decided by the frequency of the modulating signals, the waveforms of inverter is shown in Fig. 3.

(a)



(b)

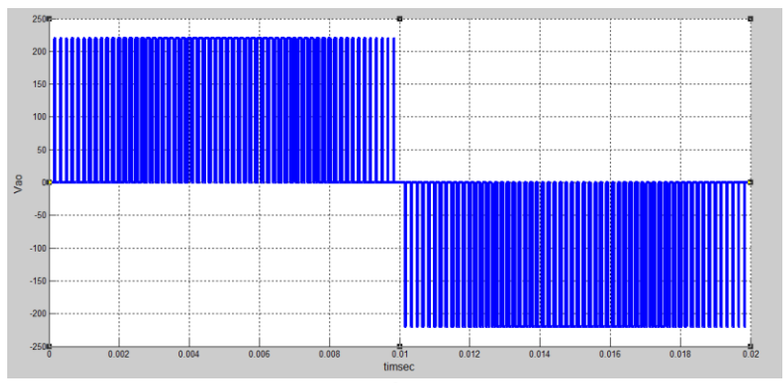


Fig. (3): PWM inverter waveforms. (a) Generation Method
(b) Inverter output voltage

2-2 Single phase induction motor

There are several types of SPIMs .They are split phase, capacitor start, capacitor run, and capacitor star-run motors. This motor has main and an auxiliary stator windings displaced by 90 degrees. The capacitor which is connected for improvement in the operation mode[1]. The motor schematic diagram is shown in Fig. 4.

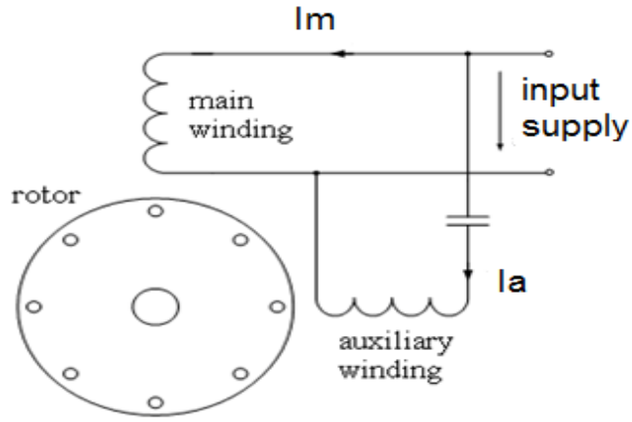


Fig. (4): Single phase induction motor

Mathematical model which describes the motor equation is similar to the unsymmetrical two-phase induction motor with simple modification to describe its behavior[1]. A schematic cross section of a single-phase induction motor is shown in Fig. 5.

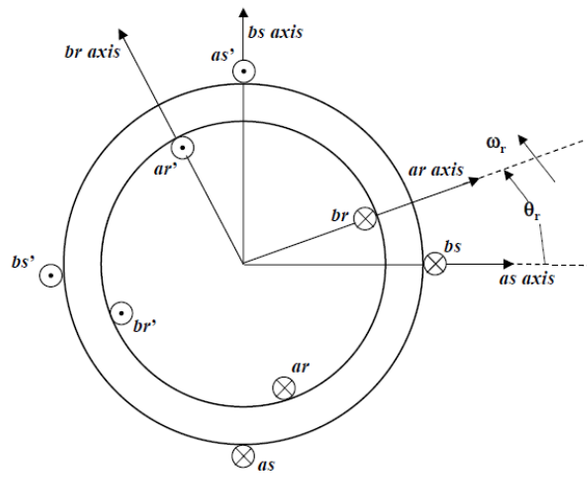


Fig. (5): A schematic cross section of SPIM

The stator and rotor voltage Equations of SPIM are given as[1]

$$v_{as} = r_a i_{as} + p\lambda_{as} \quad (1)$$

$$v_{bs} = r_b i_{bs} + p\lambda_{bs} \quad (2)$$

$$v_{ar} = r_r i_{ar} + p\lambda_{ar} \quad (3)$$

$$v_{br} = r_r i_{br} + p\lambda_{br} \quad (4)$$

The SPIM voltage equations in the q-d stationary reference frame given by:

$$v_{qs} = r_{qs} i_{qs} + p\lambda_{qs} \quad (5)$$

$$v_{ds} = r_{ds} i_{ds} + p\lambda_{ds} \quad (6)$$

$$0 = r'_{qr}\, i'_{qr} - N_{qd}\omega_r\, \lambda'_{qr} + p\,\lambda'_{dr} \quad (7)$$

$$0 = r'_{dr}\, i'_{dr} + N_{dq}\omega_r\, \lambda'_{qr} + p\,\lambda'_{dr} \quad (8)$$

where

$$N_{qd} = \frac{N_q}{N_d} \text{ and } N_{dq} = \frac{N_d}{N_q} \quad (9)$$

The torque and rotor speed are related by:

$$T_e = J\left(\frac{2}{P}\right)p\omega_r + T_L \quad (10)$$

And electromagnetic torque is given as.

$$T_e = \frac{p}{2}(N_{dq}\lambda'_{qr}i'_{dr} - N_{qd}\lambda'_{dr}i_{qr}') \quad (11)$$

Applying 4th-order Rung Kutta method the D.E of single phase induction motor has been solved. The flowchart of the algorithm as shown in Fig. 6.

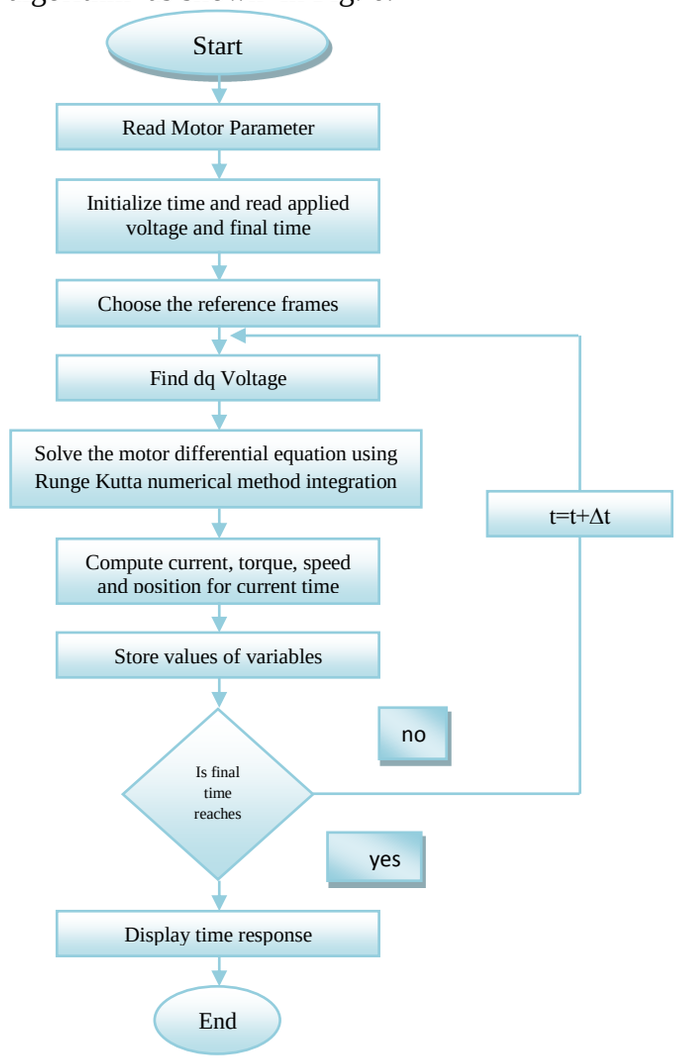
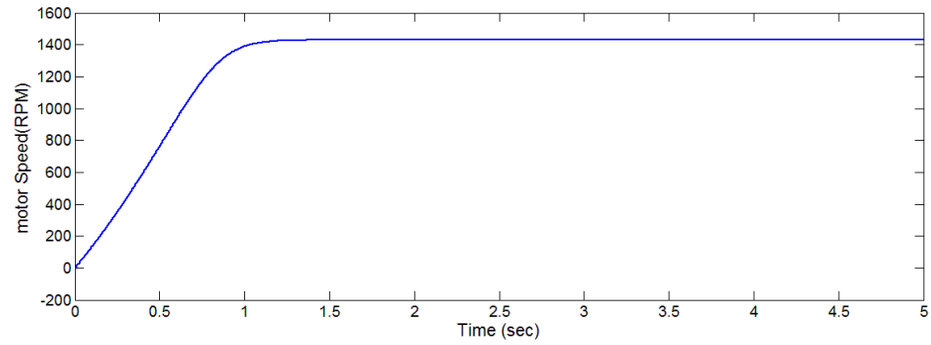
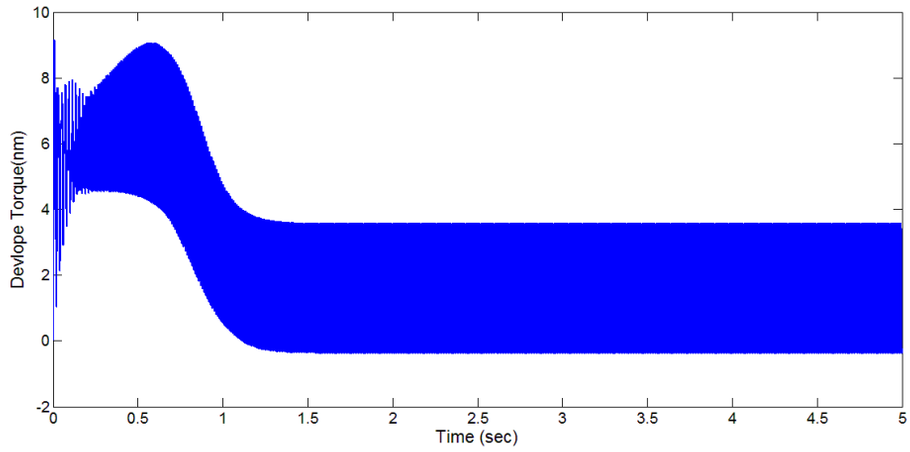


Fig. (6): Rung-Kutta solution of motor equation

The motor responses are shown in Fig.7. Fig.7a shows the motor speed, and Fig. 7b shows the developed torque for the motor (supply voltage = 220 V, supply frequency = 50 Hz, TL = 1.6 N.m)



(a)



(b)

Fig. (7): Motor response at rated load (a) Speed, (b) Develop torque

2-3 Controller

The object of the controller to match between power converter and the motor to meet the requirements . The present work uses an evolution programming technique developed from the hybridization of the genetic algorithm and bacterial foraging. Genetic algorithms are most popular technique in evolutionary programming research. It uses Darwin's theory in natural selection to simulate biological evolution[11]. Due to some limitation of genetic algorithm such as large number of iterations to give the best solution of the problem .The bacterial foraging technique selected to perform the hybridization .The bacterial foraging technique depends on the principle of the Escherichia coli (E-coli) bacteria behaviors ,and consists of four principle mechanisms namely chemotax is, swarming ,reproduction and elimination dispersal[10].

4-Controller Design

The motor speed controller is designed on the bases the error minimization of the output response with respect to the reference. The error is calculated as the performance index, which indicates the "goodness" of the system performance. A control system is considered as an optimal if the values of the parameters are chosen such that the selected performance index is minimum. Integral absolute-error criterion (IAE) is selected as an object function in the controller design which include the performance (rise time, settling time, steady state error) to be optimized.

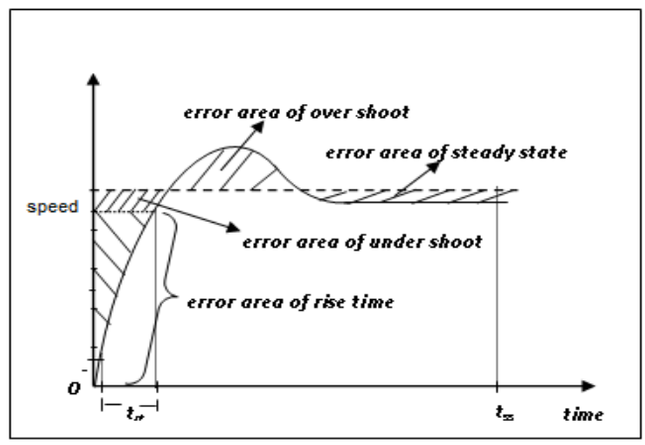


Fig. (8): Area of error for optimization

Where IAE is given by:

$$IAE = \int_0^{tsim} abs(e(t))dt \qquad (12)$$

Then the evolution programming is used to minimize the areas indicated in Fig.8.

In this paper the motor speed controller has been designed in two steps:

3-1-Genetic algorithm controller design

The design procedure using GA can be summarized in the following steps[11]:-

1- Random generation of initial population (search space of solution)
2- Compution of the fitness value for each individual in the current population (IAE for each individual)
3- Selection of certain number of individuals that scored better performance than others according to a specified selection mechanism
4- Generation of new populations from the selected individuals applying genetic operators such as crossover or mutation
5- Repeat from step 2 until a termination criterion is verified (maximum generation or tolerance reached). The flowchart of GA is shown in Fig. 9.

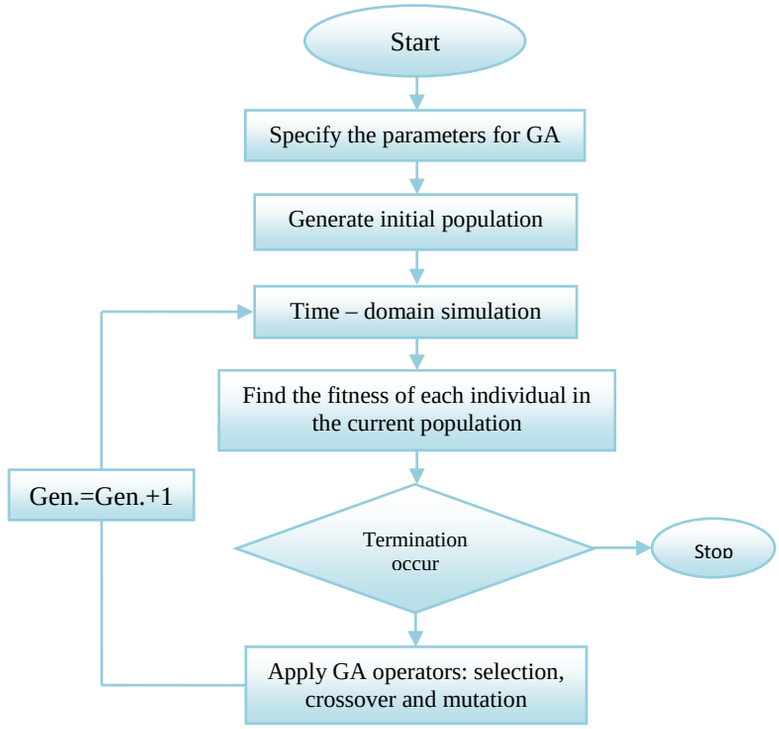


Fig. (9): Flowchart of genetic algorithm

The controller design parameters using GA is shown in table 1.

Table (1): Controller Design Parameters

Reference speed	Load torque	Best voltage	Best frequency	IAE	Population size	Number of generation	Actual speed
1100	0	180	36.81	0,0745	40	20	1095
1100	1	180	38.0644	0.1329	40	20	1094
900	0	160	29.9568	0.0763	40	20	899
900	1	160	31.2337	0.1507	40	20	894
Number of Computing IAE in worse case 800							

The problems of the conventional genetic algorithm is the large number of fitness calculation (number of solution test) and not sure convergence. The fitness calculation indicate to the elapsed time during design calculation.Fig.10 show the effect the number of generation and individuals on elapsed time.

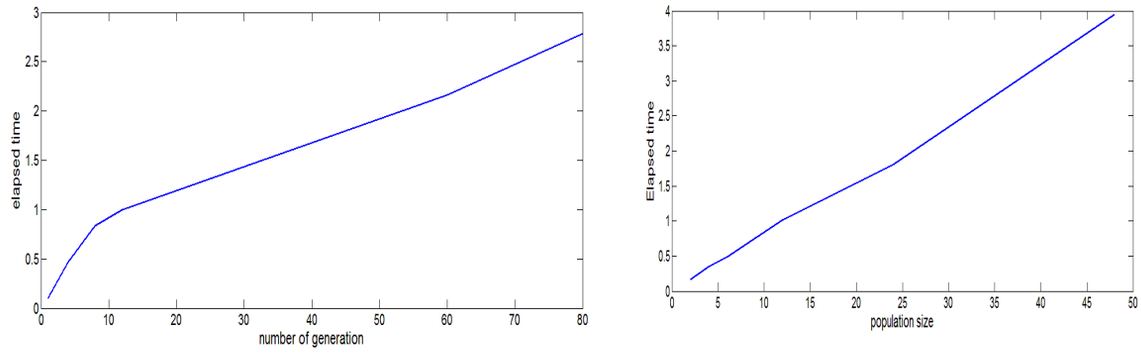


Fig. (10): a) Elapsed time vs number of generation
b) Elapsed time number of individuals

3-2 Hybrid Genetic algorithm -Bacterial foraging

One of the limitation of genetic algorithm is finding the exact global optimum and requirement large number of fitness function evaluations[10]. The Hybrid controller based on GA_BF to make the area of response error as small as possible and tracking the set point with less computional time and mathematic operation and obtain sure convergence optimize data.

The flow chart of proposed hybrid controllers design is shown in Fig.10.

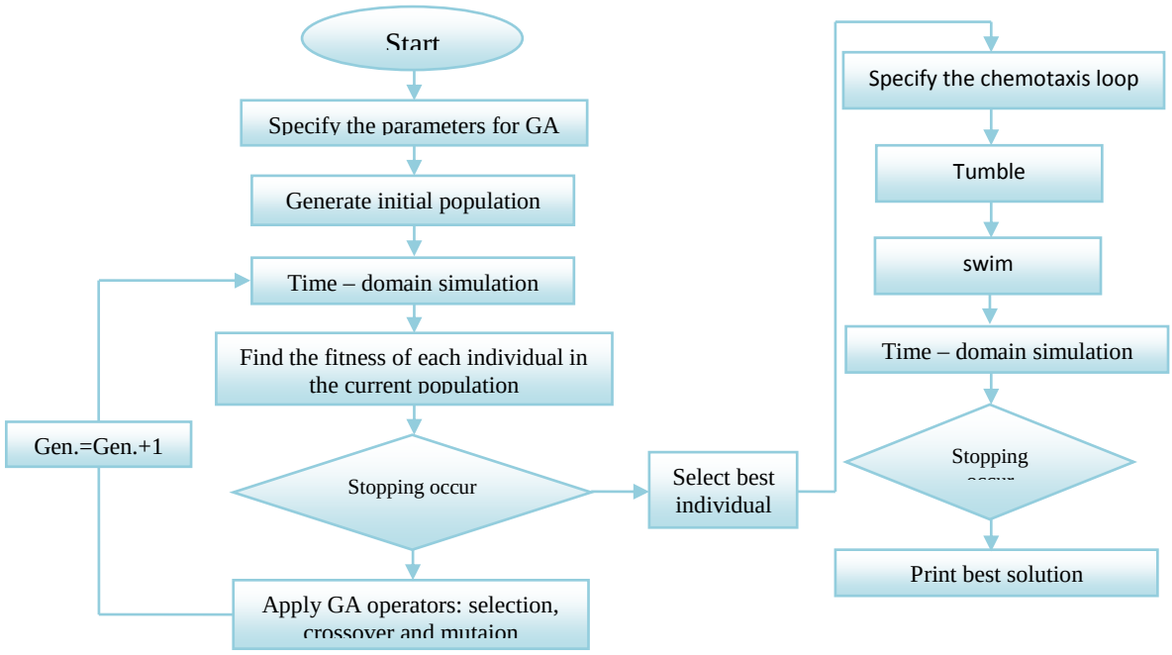


Fig. (10): Flowchart of hybrid controller

In hybrid controller the number of generation and number of individuals in design calculation reduced .The same result in table.1 obtained with reduced the number of generation (No. generation=10) and the number of individuals (No. individuals=15) then the number of computing IAE in worse case for GA-BF controller design equal 190.

Although the simplicity of the basic idea the real time application of evolutionary algorithms for optimization requires dealing with several challenging problems, because it harnesses trial and-error controller directly on the actual process to be controlled. The procedure in real-time by directly commanding the physical hardware can be extremely complex then this type of algorithms in speed controller design in term of real time implementation can used optimized look-up table of the optimized results and it is used to the real time system implementaion[9].

And others used logic protection circuit for this purpose of damage prevention to the physical hardware[7].

4-Result Discussion

This section presents the simulation results of the closed loop control system. The hybrid genetic algorithm-bacterial foraging controller sure convergence optimize data (v,f) supplied to motor through the drive circuit for tracking the speed reference. is shown in Fig.11. The steady state error has been obtained less than (2%) for all values of the speed reference of the SPIM. Fig.12 shows the

response of the motor when the controller processing begin after steady state time compared to starting tracking .

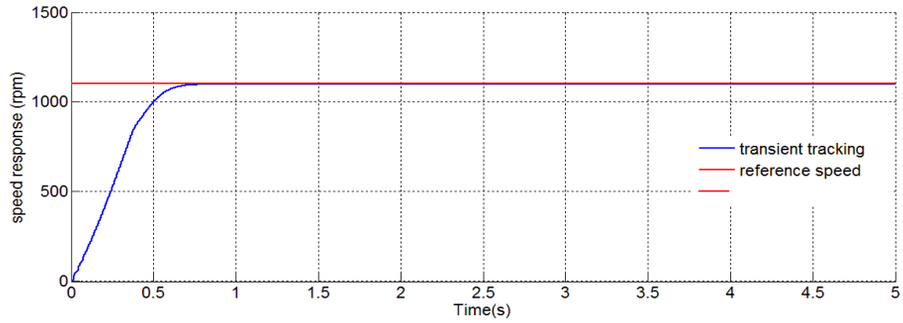


Fig. (11): Closed loop system tracking reference speed

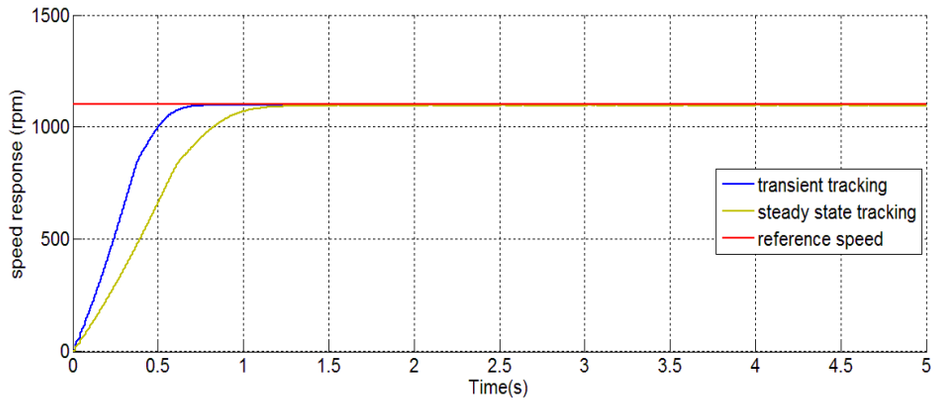


Fig. (12): Processing of controller at different times

Fig.13 and fig.14 shows the two actions of speed controller during different set points and motor subjected to different loads. It is clear there is a very good tracking of the actual speed to the reference speed (1100,900 RPM). Fig.14 shows the speed response of the motor subjected to the different loads . And the controller overcome effect the action to regulate the speed.

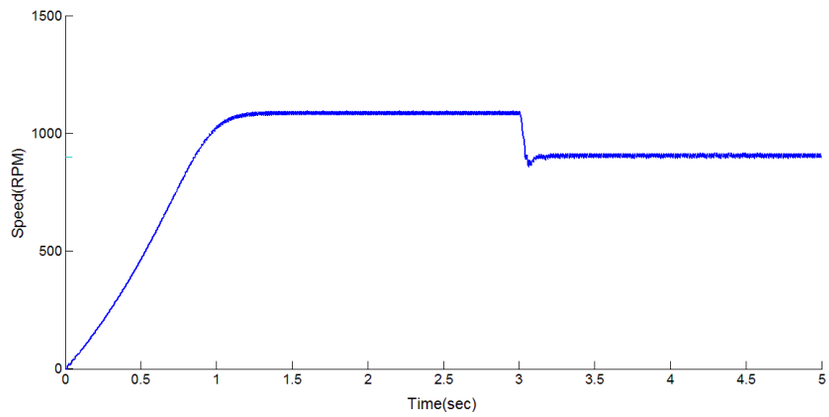


Fig. (13): Change in reference speed (1100 -900 RPM)

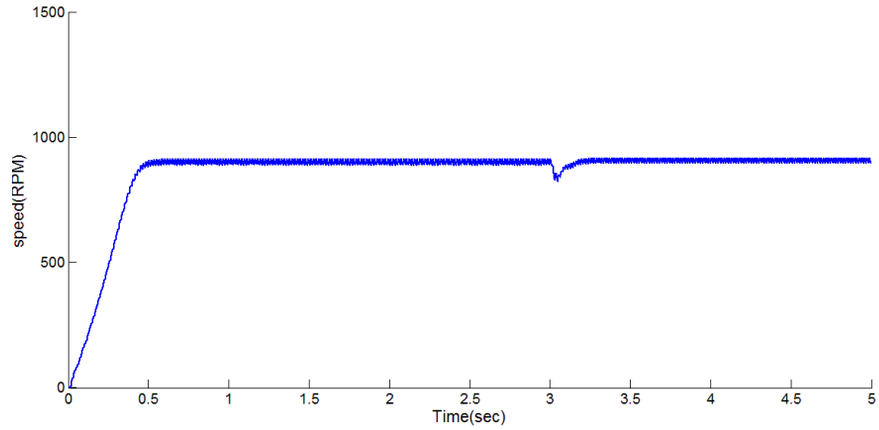


Fig. (14): Motor speed response subjected to load
(900 RPM,1N.m loaded)

6- Conclusion

This paper deals with the design of two types of controllers based on the evolution strategies {genetic algorithm and hybrid genetic algorithm-bacterial foraging} optimization. Applying this technique in the speed control of A SPIM drive system. According to the results of the computer simulation, presented a satisfactory response transient and steady state performances (rise time, settling time Steady state error) has been done as function of error area (IAE). The closed loop system with the proposed controller give good tracking to set point. And the motor operation with variation in loads and reference speed was well regulated too by proposed controller. Due to this hybridization in optimization techniques. improved in genetic algorithm have been investigated, for sure speed convergence to the optimize solution and least time of calculation design.

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Nomenclature

Im	main winding current
Ia	auxiliary winding current
Vm1&Vm2	modulation signals
Vtri	carrier signal
IAE	Integral absolute-error
VAO	inverter output voltage
p	differentiation with respect to time
abs	absolute value
tsim	time of simulation
ra	a-phase stator winding resistance
r_b	b-phase stator winding resistance
r_r	rotor winding resistance
T_e	Electromagnetic torque
T_L	Shaft mechanical torque
J	moment inertia
ω_r	Electrical angular velocity
P	Number of pole pairs
N_q	equivalent turns of phase a-stator
N_d	equivalent turns of phase b-stator
'	denote quantities are referred to the stator
γ	fluxes (stator,rotor)
Gen	generation counter

Robust Controller Design For A DC Motor With Uncertain Parameters

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Abstract

This paper presents to use of artificial intelligence to design the robust control of a DC motor using H_∞/μ controller .The proposed paper deal with parametric uncertainty of DC motor. There was analyzed influence of uncertainties of the motor parameters on the model behavior. There was designed an H_∞/μ controller via Matlab functions. The behavior of the obtained controller was analyzed on the step responses and observer of the closed loop with the nominal system and the system with perturbed parameters. Simulation results of H_∞/μ controller show an allow for wide range of change in parameters uncertainty of DC motor while the system remain stable.

Keywords: Robust, H∞/μ controller, D.C motors, Speed control, Uncertain parameters.

تصميم مسيطر متين لمحرك التيار المستمر مع عناصر عدم الدقة

د. فراس أحمد الدرزي **نغم حكمت النعيمي**

مستخلص

يتناول هذا البحث استخدام الذكاء الاصطناعي في تصميم سيطرة متينة لمحرك التيار المستمر باستخدام المسيطر H_∞/μ. يتعامل البحث المقترح مع عناصر عدم الدقة لمحرك التيار المستمر. تم تحليل عناصر عدم الدقة لمحرك التيار المستمر وتأثيرها على سلوك النموذج للمحرك. تم تصميم مسيطر H_∞/μ باستخدام برامجيات ماتلاب وتحليل سلوك المسيطر المستخدم على استجابة الخطوة للنموذج وملاحظة نظام الحلقة المغلقة بعناصره الاسمية وكذلك بتغيير تلك العناصر. أظهرت نتائج المحاكاة للمسيطر H_∞/μ إمكانية التغيير لمدى واسع في عناصر عدم الدقة لمحرك التيار المستمر مع بقاء النظام في حالة استقرار.

Introduction

One the most considerable advantages of electrical machines is the ability of speed control. Machines with control speed is widely used in industry.[1]

Parameters are one of the main problems with mathematical models of DC motor that cannot be determined with absolute accuracy and this can arise from many different factors. The values of parameters may change with time or various effects. Uncertainty is differences between the essential system and system model .Where the essential system parameters may change during operation. In this case, the linear model is no represent the essential system and yet causes practical problems.

A robust controller is needed to stabilize these types of systems for the range of expected variations in the system parameters. In the DC motor, the electrical parameters R (armature winding resistance) and L (armature winding inductance) may be manufactured within a 10 percent tolerance. The mechanical constants J (equivalent moment of inertia of the motor and load referred to the motor shaft) and B (equivalent friction coefficient of the motor and load referred to the motor shaft) may vary even more greatly as the operating conditions of the system change [2].

A lot of research works have been done in the field of position control of DC motor and prepared several methods to control speed of such motors. Some authors designed a position controller of a DC motor by selection of PID parameters using genetic algorithm (GA) once and secondly by using Ziegler and Nichols method of tuning the parameters of PID controller. They found that the first method gives better results than the second one [3], A genetic algorithm was used to find the optimum tuning parameters of the PID controller by taking integral absolute error as fitting function[4], H_∞ optimal control and Particle Swarm Optimization techniques have been used to design a robust DC motor speed controller based on the concept of fixed-structure robust controller and a mixed sensitivity method [5], Some authors designed controller to control DC motor with uncertainty parameters using H-infinity controller. It was proved that the controller is able to stabilize even the most degraded model within the given uncertainty range [6].

In this paper a robust controller has been designed using H_∞/μ controller of a DC motor speed to ensure both the stability and the performance of the system under the perturbed conditions.

DC Motor Model

A simple motor model is shown in Fig.1. The armature circuit consist of a resistance (R) connected in series with an inductance (L), and a voltage source (eb) representing the back emf (back electromotive force) induced in the armature when during rotation. [7] .

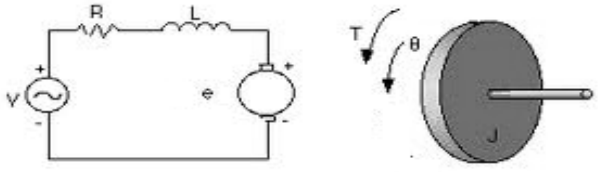

Fig (1): DC motor model

From Fig. 1 DC motor model is based on well-known description:

$$\frac{di}{dt} = -\frac{R}{L} i - \frac{K_E}{L} \omega + \frac{1}{L} v \quad (1)$$

$$\frac{d\omega}{dt} = -\frac{1}{J} B\omega + \frac{1}{J} K_T i \quad (2)$$

There are several different ways to describe a system of linear differential equations. The plant model will be introduced in the form of state-space representation and given by the equations:

$$\dot{X} = Ax + Bu \quad (3)$$

$$y = Cx + Du \quad (4)$$

The state space model will be:

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & -\frac{K_E}{L} \\ \frac{K_T}{J} & -\frac{B}{J} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} u \quad (5)$$

$$y = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \quad (6)$$

Where $x_1 = i$, $x_2 = \omega$, and $u = v$.

The meaning of particular terms is following : K_T is the torque constant, J is the Dc motor inertia, B is coefficient of viscous friction, i is the instantaneous value of the electrical current, ω is the instantaneous angular velocity of the shaft, K_E is the voltage constant (inverse speed constant), R is the armature resistance, L is the armature inductance and finally u is the instantaneous value of a supply voltage.

The values of the terms are for the Model No. - 6312S001-R1 (Pittman Express) following:
$J = 5.2 \times E{-}7$ kgm2, $R = 7.75\ \Omega$, $L = 0.00405$ H, $K_T = 0.0131$NmA−1, $K_E = 0.0131$ Vs rad−1 and $B = 4.9E\text{-}7$ Nms rad−1 [8].

System Uncertainty Description and Representation on Interconnection Matrix

Four physical parameters (R ,L ,J ,B) may be considered .The exact values of the above parameters are normally unknown. To represent the uncertainty parameters we add the $\delta\Delta$ to each physical parameter: where δ is parameter uncertainty weight and Δ equal to 1 or -1. Fig .2 is represent the procedure inputting uncertainty element (L). The introduced perturbations are $\delta\Delta_R$, $\delta\Delta_L$, $\delta\Delta_J$, $\delta\Delta_B$. The sketch $(1+\delta\Delta)$ can be added to the selected parameters of the system to represent the uncertainty variations. The system developed block diagram with uncertainty is given in Fig. 3.

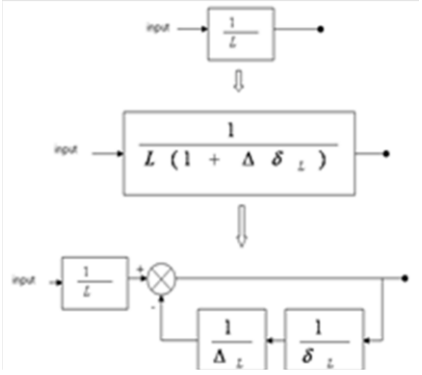

Fig (2): Block diagram represents the procedure inputting uncertainty element (L).

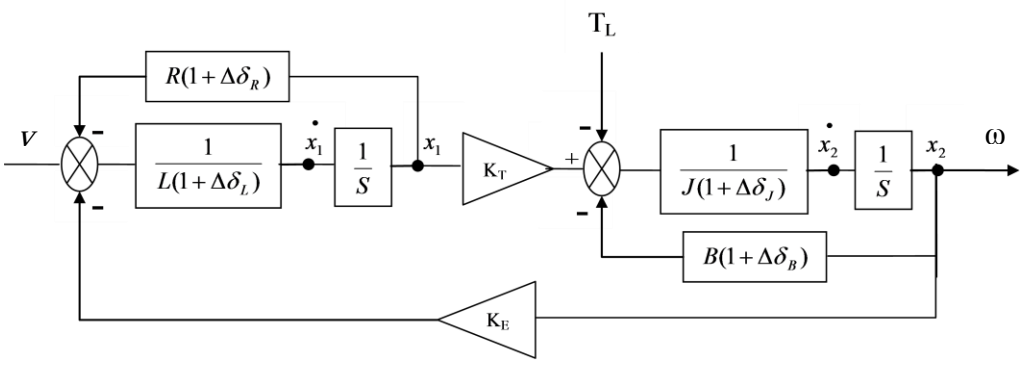

Fig (3): DC motor block diagram with uncertainties parameters.

H_∞ /μ Synthesis Theory

The control synthesis procedure described here is H_∞/μ synthesis, which consists of H_∞ optimal control synthesis, μ-analysis, and D-scaling, nested in an iterative scheme .The description is intended as an overview of the motivation behind the procedure known as μ-synthesis. First, the synthesis setup, which consists of a state space model, is used to compute an H_∞-optimal controller [9].

Structure Singular Value and μ -Based Controller

a. Structure singular value and μ synthesis

The general framework of μ analysis and synthesis [10]shown in Fig. 4, is based on the Linear Fractional Transformations (LFTs). (Any hear interconnection of inputs, outputs and commands along with perturbations and a controller can be viewed in this context and rearranged to match this diagram). For the purpose of analysis, controller *K* is obtained into plant *P* to form the interconnected matrix structure shown in "Fig.4-b",

$$\Delta \approx \{diag(\delta_i I_{ri},...,\delta_s I_{rs},\Delta_i,...,\Delta_F);\delta_i \in C,\Delta_i \in C^{m_i \times m_s}\} \quad (7)$$

$\Delta = \{\Delta \in \Delta / \bar{\sigma}(\Delta) \le 1\}$ [10].

For *a* system described in the complex matrix, $M \in C^{m\times n}$, the structural singular value μ is defined as:

$$\mu_\Delta(M) = 1/\min\{\bar{\sigma}(\Delta) : \Delta \in \Delta, \det(I - M\Delta) = 0\} \quad (8)$$

Thus, $\mu_{\Delta}(M)$ is a measure of the smallest structured Δ that causes instability of the constant matrix feedback loop shown in "Fig.4-b" .Given a desired uncertainty level, the purpose of this design is to look for a control law, which *can* bring down the closed loop system μ level and ensure the stability of *the* system for all possible uncertainty descriptions.

The performance and stability conditions for a system in the presence of structured uncertainty in terms of μ arc given as:

1. Robust stability (RS)

$$F_u(M,\Delta) stable \forall \Delta \in B\Delta \quad iff \quad \sup_{\omega} \mu(M_{11}(j\omega)) \le 1 \tag{9}$$

2. Robust performance (RP)

$$F_u(M,\Delta) stable \;\; \& \;\; \left\| Fu\;(M,\Delta) \right\|_{\infty} \le 1 \;\; \forall \Delta \in B\Delta \tag{10}$$

$$iff \; \sup_{\omega} \mu(M_{11}(j\omega)) \le 1$$

In other words, the performance and stability of the closed loop system *M* is a μ test. The synthesis problem is represented by the structure in "Fig.4-c". The control error e' can be expressed as the following LFT.

$$e' = F_L(P,K)v' = [P_{11} + P_{12}K(I - P_{22}K)^{-1}P_{12}]v'$$

Ideally, the goal is to find a controller *K* such that:

$$\left\| F_L(P,K) \right\| \mu \le 1$$

However, as there is no effective technique to which this *K* may be obtained directly, indirectly it is calculated scaling matrix *D*.

$$\min_{K} \inf_{D} \left\| DF_L(P,K)D^{-1} \right\|_{\infty} \le 1 \tag{11}$$

$$D = \{ diag(d_1 I, d_2 I, ..., d_0 I) \uparrow d_i \in R_+ \}$$

During minimization process, fixing either *D* or *K* is called especially D-K iteration .It has no significal that practically and may widely used [11].

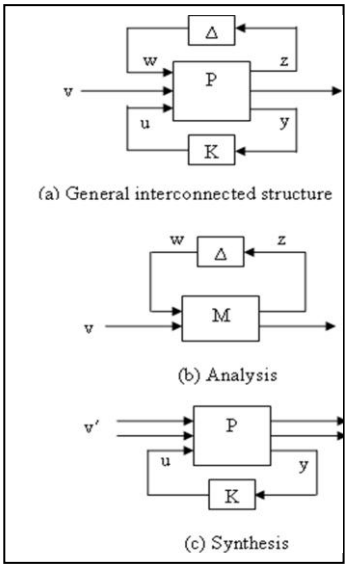

Fig. (4): μ analysis and synthesis

The objective of the Controller design in an interconnected of DC motor model is regulate of the speed i.e. on the stability of the overall model for all admissible uncertainties. Thus, speed of DC motor (ω) is considered as controller inputs. The first step in designing of the μ -based controller is to formulate design problem into the μ general framework. The state-space model along with uncertainties will be separated as:

$$P_0 = \begin{cases} \dot{x} = A_0 x + B_0 u_1 + B_1 w \\ z = C_z x + D_z u_1 \\ y = Cx \\ w = \Delta z \end{cases} \quad (12)$$

Where matrix Δ is given by :

$$\Delta = \{diag(\delta_1 I_2, ..., \delta_2 I_2, \delta_i); \delta_i \bullet R, \|\Delta\| \le 1\}$$

The design problem formulation for the μ general structure is shown in Fig.5. In this block diagram, P_o is the interconnection of nominal plant and all parametric uncertainties. In order to take modeling error into account, an additional input multiplicative uncertainty is considered by weighting function *Wc* . The *Wp* indicates the system performance specifications[12] .

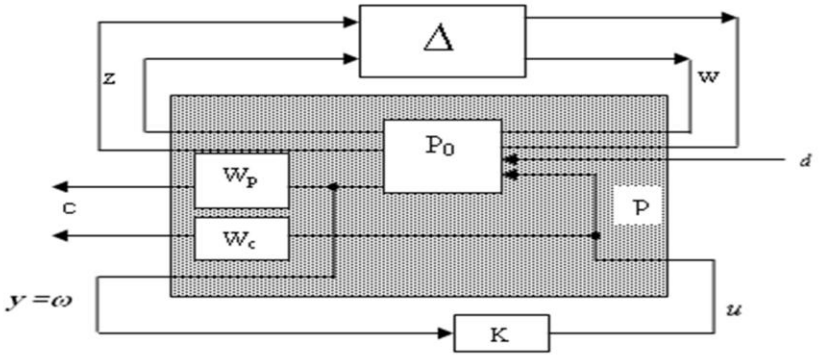

Fig (5): Formulation of μ based controller design [11]

b. Robust performance of the uncertain system

After representing the structured uncertainty of the system parameters, some performance parameters must be added to the system like input and output uncertainties as shown in Fig.6.

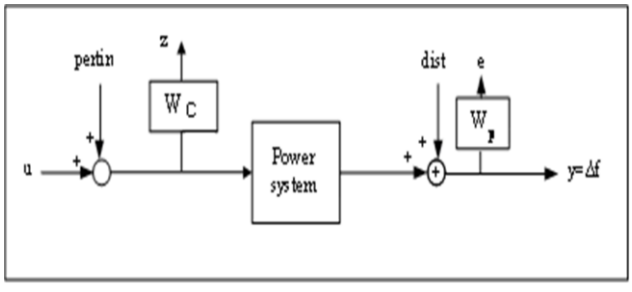

Fig. (6): Input output uncertainty representation

where, Wc input uncertainty weight. Wp output uncertainty weight.
Pertin perturbation input , dist disturbance

H_∞/μ Synthesis Algorithm

Step 1: Initial data: system state space realization .

Step 2: Define the interconnection structure(matrix P).

Step 3:H∞ controller design and minimize of the $\|\cdot\|_\infty$ norm of F(P,K), over the controller variable K.

F(P,K), = G F(P,K) = G (13)

The command **hinfsyn** in the matlab package function designs a (sub)optimal H_∞

Step 4: μ -Analysis of H_∞ design

In this step The H_∞ design is analyzed with respect to structured uncertainty using μ.

μ-synthesis implies the minimization of the following criteria [13] [14] :

$$\mu = 1/\min_{K} \inf_{D\in\underline{D}} \sup_{\omega} \bar{\sigma}\left(DF(P,K)D^{-1}\right) \quad (14)$$

For a frequency domain μ-analysis of robust performance properties, the block structure consists of a 4 × 4 uncertainty block, and a 2 × 2 performance block as shown in:

$$\Delta = \left\{ \begin{bmatrix} \Delta_u & 0 \\ 0 & \Delta_p \end{bmatrix} : \Delta_u \in C^{12\times 12}, \Delta_p \in C^{2\times 2} \right\}$$

robust performance is achieved if and only if μ of the closed-loop system response is less than 1.

The μ-analysis command,**mu,**calculates upper and lower bounds for the structured singular value.

Step 5: If the μ value of the closed loop system is less than one ,then terminate the work. which mean system performance achieved robust performance, otherwise go to step 6 .

Step 6: μ-synthesis technique is applied here to a achieve a robustly stable power system(Ds-K) iteration is applied to find the optimal robust performance of DC motor model with uncertainties). The structure of Ds-K iteration can be shown in Fig.7.

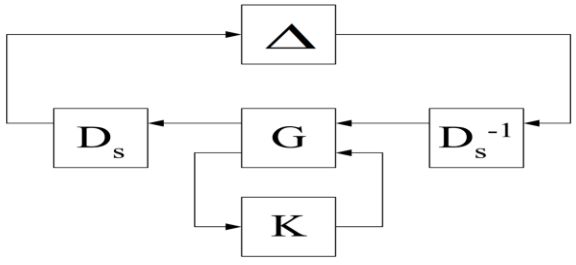

Fig. (7) : Structure of the Ds-K iteration

The procedure for μ-synthesis through Ds-K iteration involves several iterations. These iterations are numbered using the variable i=1,2,3,... Each iteration consists of the following four steps:

1- H_∞-synthesis:

H_∞-synthesis is applied on the generalized plant P matrix minimizing the H_∞-norm between (w,d) and (z,e).Which means that the performance variables used in the H_∞-synthesis are the combination of the original perturbation parameters and the original performance variables:

$\hat{d} = \begin{pmatrix} w \\ d \end{pmatrix}$ and $\hat{e} = \begin{pmatrix} z \\ e \end{pmatrix}$

2- μ-analysis:

Connecting the H_∞-controller found in the previous step to the generalized plant yielding G=F (P,K).

3-Ds-scale fitting:

The Ds-scales found in the μ-analysis step consist of a constant complex matrix for every point of the specified frequency grid.

4-Add the Ds-scales to P_{i+1} :

Construct the model for the P_{i+1} generalized plant by scaling the original P with the rational Ds-scale. The total system matrix P can be scaled by augmenting the Ds-scale with an identity matrix at the (u,y) variables:

$$P_{i+1} = \begin{bmatrix} D_s & 0 \\ 0 & I \end{bmatrix} \begin{bmatrix} P_{11} & P_{12} \\ P_{21} & P_{22} \end{bmatrix} \begin{bmatrix} D_s^{-1} & 0 \\ 0 & I \end{bmatrix}$$

Simulation Results:

In order to verify the validity of the H_∞/μ controller, several simulation tests are carried out using MATLAB/SIMULINK. The performance of H_∞/μ controller has been investigated and compared with the closed loop system. Simulation tests are based on the facts that whether the $H\infty/\mu$ controller is better and more robust than the closed loop system or not. For the comparison, simulation tests of the speed response were performed according to the nominal condition, uncertainties parameters variation of the DC motor .Fig.8 shows the speed responses control of the DC motor of closed loop system and H_∞/μ controller. According to the simulation results, H_∞/μ controller give the better performance compared to closed loop system without controller.

For high performance applications the proposed H_∞/μ controller should be robust to parameter variations. Changes in (R ,L ,J ,B) are investigated through simulations. The simulation studies are undertaken by changing one parameter at a time while keeping other parameters unchanged. The DC motor is commanded to accelerate from rest to reference speed under no torque load.

Fig.9 and Fig.10 show the DC motor responses of H_∞/μ controller approach when the armature resistance R and the armature inductance L are increased by 5% and 10% of there is original value .Fig.11 and Fig.12 show the DC motor responses of H_∞/μ controller approach when the DC motor inertia J and coefficient of viscous friction B are increased by 10% and 30% of there is original value.

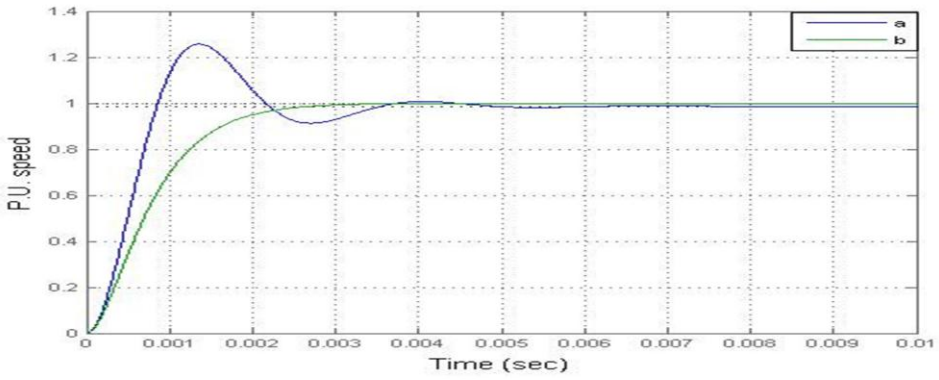

Fig. (8): DC motor speed responses a- closed loop system b- system with H_∞/μ controller

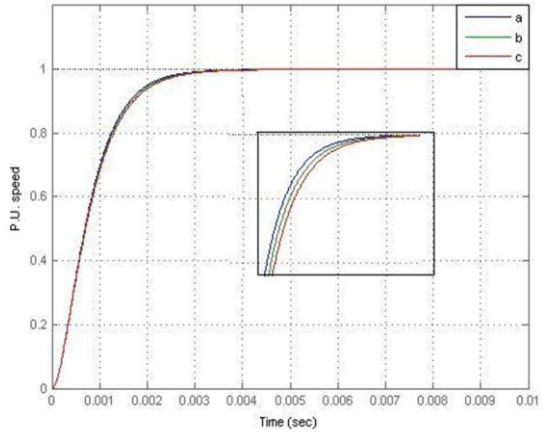

Fig 9 Speed control responses with H_∞/μ controller a- δ_R=0% b- δ_R=5% c- δ_R=10%

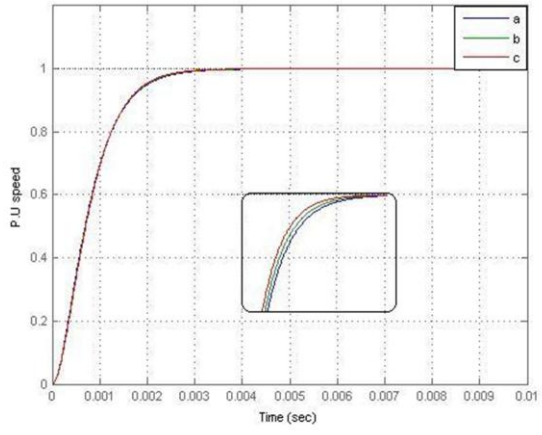

Fig 10 Speed control responses with H_∞/μ controller a- δ_L=0% b- δ_L=5% c- δ_L=10%

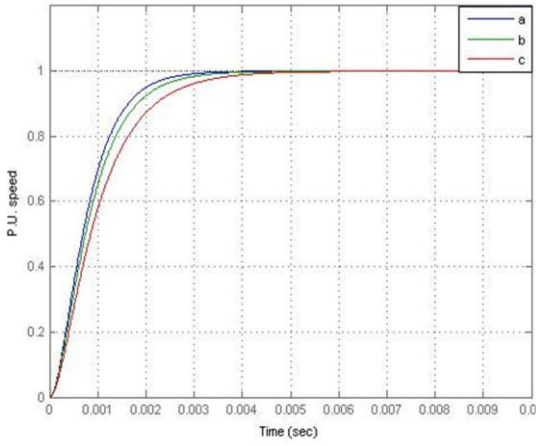

Fig 11 Speed control responses with H_∞/μ controller a- δ_J=0% b- δ_J=10% c- δ_J=30%

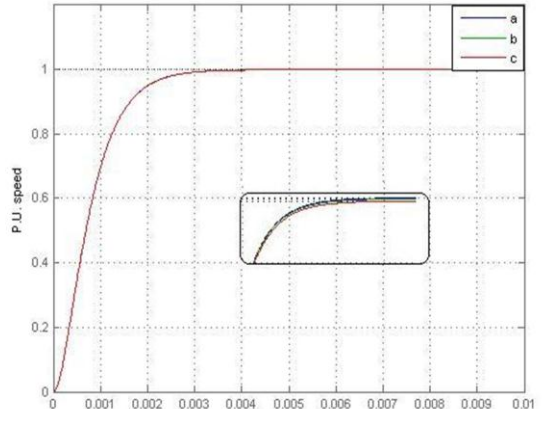

Fig 12 Speed control responses with H_∞/μ controller a- δ_B=0% b- δ_B=10% c- δ_B=30%

Keeping other parameters constant.The table gives system performance for closed loop system and H∞/μ controller. Based on the Table 1, H_∞/μ controller has the fastest settling time of 0.0025 sec and the slowest rise time 0.00142 sec , while closed loop system has the slowest settling time of 0.00415 sec and rise time 0.000571 sec .For the percent overshoot, H_∞/μ controller does not have overshoot and closed loop system has the greatest value of percent overshoot of 27.4 % (Fig 8). It is obvious that the change of uncertainty of parameter R and L are small impact on the model behavior Fig 9 and Fig 10 .The least impact on the model behavior has the uncertainty of the parameter B (Fig. 11). On the other hand uncertainty of the parameter J (Fig. 12) is changing the model behavior dramatically comparison with other parameters.

Table (1): Effect of change in each parameter alone on the system performance with keeping other parameters constant.

System	Change %	Closed loop system			System with H_∞/μ Controller		
		Overshoot %	Settling Time (sec)	Rise time (sec)	Overshoot %	Settling Time (sec)	Rise time (sec)
Without any change in parameters	0	27.4	0.00415	0.000571	0	0.0025	0.00142
δ_R and other parameter are constant	5	25.3	0.00335	0.000583	0	0.00258	0.00146
	10	23.4	0.00335	0.000595	0	0.00266	0.00149
	-5	29.5	0.00432	0.00056	0	0.00241	0.00138
	-10	31.7	0.0044	0.000549	0	0.00233	0.00134
δ_L and other parameter are constant	5	28.4	0.00436	0.00058	0	0.00244	0.0014
	10	29.3	0.00453	0.000588	3.91E-7	0.00239	0.00139
	-5	26.3	0.00326	0.000563	0	0.00255	0.00143
	-10	25.2	0.00318	0.000554	0	0.0026	0.00145
δ_J and other parameter are constant	10	25.4	0.0035	0.000611	0	0.00285	0.00159
	30	22	0.0038	0.00069	0	0.00353	0.00195
	-10	29.6	0.0041	0.000531	7.55E-6	0.00214	0.0124
	-30	34.7	0.00372	0.000449	0.431	0.00146	0.000917
δ_B and other parameter are constant	10	27.4	0.00415	0.000571	0	0.0025	0.00142
	30	27.4	0.00415	0.000571	0	0.0023	0.00140
	-10	27.4	0.00415	0.000571	0	0.0025	0.00142
	-30	27.4	0.00415	0.000571	0	0.0023	0.00140

Other simulation studies are undertaken by changing all parameters at the same time .The results are given in table (2). The closed-loop system and the system with H_∞/μ controller was tested at parameter variation = (10%,50%and 90%).It is clear from the table (2) that the percent

overshoot value as well as the settling time where minimum for the case of the H∞/μ controller. Fig.13 and Fig.14 show the DC motor responses of closed loop system and H∞/μ controller approach when the all parameters increased by 50% and 90% of there's original value. It is clear from Fig.13 and Fig.14 that the system is unstable when increased all parameters to 50% and 90% for closed loop system while the system remain stable using H_∞/μ controller. The results show that the system with proposed H_∞/μ controller is the best, and the system maintains its stability for a wide range of variations in parameters.

Table (2): Effect of change all parameter on the system performance .

System	**Change %**	**Closed loop system**			**System with H_∞/μ Controller**		
		Overshoot %	Settling Time (sec)	Rise time (sec)	Overshoot %	Settling Time (sec)	Rise time (sec)
Without any change in parameters	0	27.4	0.00415	0.000571	0	0.0025	0.00142
Change all parameter (δ_R, δ_L, δ_J ,δ_B)	10	31.7	0.00412	0.0005	0	0.002	0.001
	50	54.7	0.00412	0.00025	0.71	0.00081	0.0005
	90	88.1	0.00413	4.4e-5	5	0.00024	8.1e-5

Conclusion

The H_∞/μ controller design is based on uncertain model of the DC motor via Matlab functions. It can be applied to control the speed of a DC motor. The performance of the H_∞/μ controller and closed loop system are validated through simulations. The controller was tested and it was proved that the controller is able to `stabilize` model within the given uncertainty variation. One can conclude that H_∞/μ controller realises a good dynamic behaviour of the DC motor with a rapid settling time, no overshoot compared to closed loop system. The proposed controller can achieve robustness and good performance and it gives a reliable model for system to sustain its stability over a wide range of parameters variation.

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تحسين أداء مسوق المحرك الحثي المناسب للسيارة الكهربائية بالاعتماد على الخوارزمية الجينية

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الخلاصة

يقدم هذا البحث مقترحاً لاختيار نقطة عمل مثلى لتحسين كفاءة وأداء المحرك الحثي ثلاثي الطور نوع القفص السنجابي مع دائرة المسوق والمستخدم في السيارات الكهربائية. حيث يساهم البحث في تقليل الطاقة المستهلكة في المنظومة و هذا ينعكس ايجابيا على إمكانية زيادة المسافة التي تقطعها السيارة الكهربائية قبل إعادة شحن البطارية. تم في هذا البحث مقارنة عمل المحرك الحثي لحالة تشغيل معينة تتناسب مع طبيعة السيارة الكهربائية كحمل من ناحية أعظم كفاءة أو أعظم عامل قدرة أو أعلى عامل انتفاع للقدرة، وبالاعتماد على الخوارزمية الجينية. يتم تحديد قيم كل من الفولتية و التردد اللازمين لإنجاز حالة التشغيل. إن النتائج التي تم الحصول عليها من خلال التحليل و التمثيل ترجح استخدام أعظم عامل انتفاع للقدرة كمعيار للحصول على قيمتي كل من الفولتية و التردد اللازمين. و قد تم تحقيق ذلك من خلال مقارنة بين النتائج باستخدام الخوارزمية الجينية والنتائج باستخدام طريقة السيطرة التقليدية E_1/F_S وباستخدام مسوق مغير فولتية و تردد يعتمد على تضمين عرض النبضة لتقليل تأثير التوافقيات و الذي يساهم بدوره أيضا في تقليل استهلاك الطاقة.

الكلمات الدالة: أعظم انتفاع للقدرة، تضمين عرض النبضة الجيبي SPWM، الخوارزمية الجينية، السيارة الكهربائية، السيطرة التقليدية E_1/F_S، المحرك الحثي ثلاثي الطور

Improving Performance of Induction Motor Drive Suitable for Electric Car Based on Genetic Algorithm

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Abstract

This paper presents a proposal of selecting an optimal operating point to improve the efficiency and the performance of the three phase squirrel cage induction motor with the drive circuit is used in the electric cars. The research will help in reducing the consumed power in the system and this will reflect positively on prolonging the distance taken before recharging. The performance of the induction motor is tested according to a certain operating situations corresponded with the electric car type as load with the largest efficiency, maximum power factor or maximum utilized power depending on the genetic algorithm. Torques and speeds are gained via the nature and manner of the application in which the values of voltage and frequency needed in a certain operating situations. The results, detected from analysis and simulation most probably, show the use of the maximum utilized power as a criterion of achieving the values of the wanted voltage and frequency. It is achieved by comparing between the result of genetic algorithm and the result of conventional E_1/F_S by using voltage source inverter drive which depends on pulse width modulation to reduce the effect of the harmonics which consequently contributes to reduce the dissipated power.

1. المقدمة:

بدأ الاهتمام الواسع بالسيارات الكهربائية في الآونة الأخيرة، بسبب ارتفاع أسعار النفط وكذلك الحاجة إلى المحافظة على البيئة من الانبعاثات الناتجة عن السيارات التقليدية. خلال العقود الأخيرة، قامت مصانع السيارات المشهورة بالعمل على السيارات الكهربائية وتطويرها. سنة بعد أخرى، بدأت مصانع السيارات بطرح إصدارات جديدة من نماذج السيارات الكهربائية. اعتمدت مصانع السيارات معظمها على استخدام المحرك الحثي ثلاثي الطور نوع القفص السنجابي كمحرك للسيارات الكهربائية، ذلك لامتلاكه للعديد من المميزات مقارنة مع المحركات الكهربائية الأخرى، وتشمل هذه المميزات : كونه رخيص الثمن، ذو وزن قليل وحجم صغير، ذو صيانة قليلة وذو بنية متينة وكفاءة عالية. هذه المميزات هي ملائمة عملياً في تطبيقات السيارات الكهربائية[2][1]، الشكل رقم (1) يبين بعض أنواع السيارات الهجينة الكهربائية Hybrid Electric Cars واستخدامها للمحركات [3]

شكل رقم (1) : بعض انواع محركات السيارات الكهربائية

تم صنع أول دراجة كهربائية في عام 1881 مكونة من ثلاث عجلات بمحرك DC بقدرة (0.1HP) ولكنها لم تلقى الاهتمام وذلك لعدم نضوج الفكرة للمركبة الكهربائية[1]، في عام 1916 قامت شركة General Motor (GM) بالعمل على السيارة الكهربائية نوع GMC Truck تعمل على بطاريات نوع lead acid، بعد ذلك تم العمل على السيارات ذات محرك الاحتراق الداخلي. في الأعوام ما بين 1960-1970 عادت شركة GM للعمل على السيارات

الكهربائية النقية والسيارات الكهربائية الهجينة. في الأعوام ما بين 1970-1980 لم يتم التوجه لتطوير السيارة الكهربائية لان النفط لم يكن المشكلة الرئيسية بالنسبة للسيارات التقليدية ذات الاحتراق الداخلي. وفي الأعوام ما بعد 1980 بدأت شركة General Motor بالاهتمام بتطوير السيارات الكهربائية، وفي عام 1990 تم صناعة سيارة كهربائية نوع Impact وذلك لارتفاع أسعار الوقود في الولايات المتحدة الأمريكية وكذلك للتقليل من التلوث الحاصل في البيئة، وهكذا تم العمل على تطوير السيارة الكهربائية من قِبَل شركة GM إلى أن تم صناعة سيارة كهربائية هجينة نوع Chevrolet Volt في عام 2011[4-5].

يمتلك المحرك الحثي كفاءة عالية نسبياً قد تصل إلى أكثر من80%، حيث يتم عادة تصميم المحرك الحثي بكفاءة عالية و عامل قدرة جيد عند القيم المقننة. تتأثر كفاءة المحرك الحثي مع تغير حالات عمل المحرك. يمكن تحسين الكفاءة وعامل القدرة للمحرك الحثي من خلال اختيار مستوى مناسب للفيض في المحرك مع تقليل خسائر المحرك والتي تشمل الخسائر النحاسية للملفات والحديدية للب المغناطيسي والخسائر الميكانيكية عن طريق تحسين كفاءة المحرك الحثي.

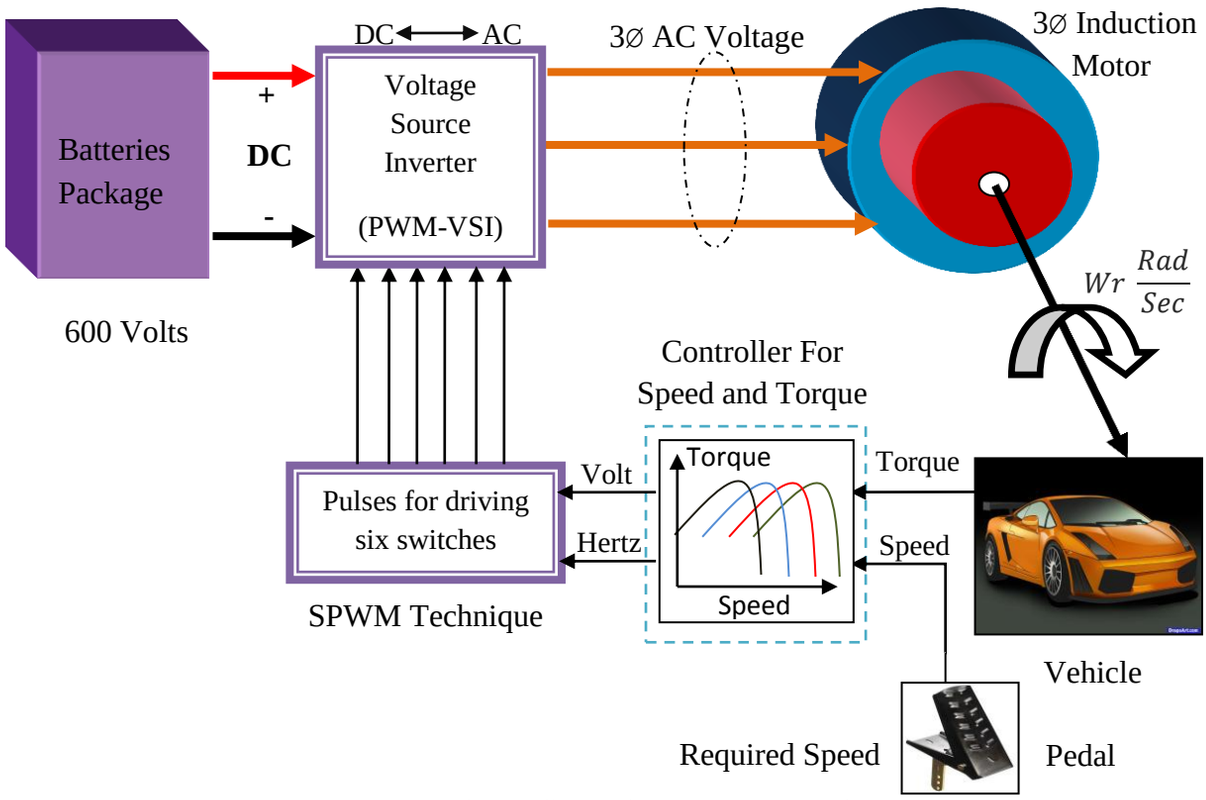
يوجد عدة استراتيجيات لمسوق المحرك الحثي لتحقيق الكفاءة المثلى وتقليل التيار عبر نبائط المسوق، يتم استخدام الاستراتيجيات لمسوق المحرك بما يتناسب مع أداء المحرك الكهربائي المستخدم في السيارات الكهربائية. في هذا البحث تم استخدام طريقة السيطرة Volt/Hertz وبنسبة مبنية على الخوارزمية الجينية (Genetic Algorithm) للحصول على اقرب ما يمكن لامثل كفاءة وامثل عامل قدرة ممكنة عند نقطة تشغيل معينة للمحرك الحثي والتي تتناسب مع طبيعة التطبيق.

قام الباحثون (C. Thanga Raj , P. Srivastava and Pramod Agarwal) بدراسة تطوير الكفاءة المثلى للمحرك الحثي ثلاثي الطور من خلال امثل الطرق للسيطرة على المحرك الحثي لتحسين كفاءته وامثل التقنيات لتصميم المحرك الحثي التي تتضمن بعض التعديلات على معدن المحرك[6]. كما قام الباحث (Hussien Sarhan) باستخدام طريقة سيطرة مبنية على إستراتيجية البحث على قيمة فولتية ملفات الجزء الساكن للحصول على الكفاءة المثلى لمسوق المحرك الحثي إضافة إلى استخدامه طريقة سيطرة (Slip Compensation) لتقليل الانزلاق عند الحمل الخفيف أو اللاحمل وعند الترددات القليلة للحصول على نقطة تشغيل مستقرة[7]. وقام الباحثون (Hussein Sarhan, Rateb Issa, Mohammad Alia and Jamal M. Assbeihat) باستخدام طريقة (Slip Compensation) معتمدة على نظرية السيطرة المضببة (Fuzzy Logic Control)، حيث استخدم نسبة الخطأ في السرعة ومعدل تغير الخطأ في السرعة كداخلات للمضبب ويكون الإخراج هو التردد ، وذلك للحصول على نقطة تشغيل مستقرة عند الترددات القليلة أو الحمل الخفيف[8]. كما قام الباحثون (Branko D. Blanuša, Branko L. Dokić and Slobodan N. Vukosavić) باستخدام طرائق للسيطرة على المحرك الحثي (Simple State Control, Loss Model Control and Search Control) للحصول على أعظم كفاءة للمحرك الحثي لتقليل القدرة المتطلبة لتشغيل المحرك الحثي[9].

2. الوصف العام لمنظومة السيارة الكهربائية

يبين الشكل رقم (2) منظومة مسوق محرك السيارة الكهربائية، حيث تتكون المنظومة من مجموعة بطاريات والتي تربط إلى مسوق للمحرك الحثي ثلاثي الطور مع دائرة السيطرة على السرعة والعزم للسيارة الكهربائية. المسوق هو مغير مصدر الفولتية (VSI) ثلاثي الطور والذي يتكون من ترانزستورات قدرة عدد ستة[10-11]. يربط دايود معاكس على التوازي لكل ترانزستور قدرة نوع ثنائي فائق الرجوع (Fast Recovery Diode)، يعمل على حماية الترانزستور ويعمل على إرجاع القدرة من المحرك الحثي إلى البطاريات بسبب الطبيعة الحثية للحمل وكذلك إعادة شحن البطاريات من خلال عملية إعادة التوليد Regenerative.

تم استخدام طريقة القدح للمغير (VSI) بالاعتماد على تقنية تضمين عرض النبضة (SPWM) (Sinusoidal Pulse Width Modulation) ، وذلك من اجل الحصول على فولتية وتردد متغيرين. يبين الشكل رقم (3) طريقة قدح نبائط المغير، وموجات الفولتية والتيار الإخراج للمغير، حيث تم اختيار تردد الموجة الحاملة(F_c = 750Hz) وتردد موجة الإخراج الأساسية (تردد الموجة المرجعية (F_r= 50Hz)) وذلك للحصول على عامل تردد التضمين (m_f) عدد فردي صحيح ومن مضاعفات العدد ثلاثة للتخلص من تأثير تردد الموجة الحاملة وظهور فقط التوافقيات الفردية ذات الرتب العالية نسبياً والتي لا تقبل القسمة على ثلاثة لفولتية الإخراج. يتم التحكم بفولتية الإخراج الأساسية عن طريق عامل التضمين (m_a) وذلك بمقارنة قيمة الموجة المرجعية (A_r) مع قيمة الموجة الحاملة (A_c) [11-13].



شكل رقم (2): منظومة المسوق للسيارة الكهربائية

$$m_f = \frac{F_c}{F_r} \qquad (1)$$

$$m_a = \frac{A_r}{A_c} \qquad (2)$$

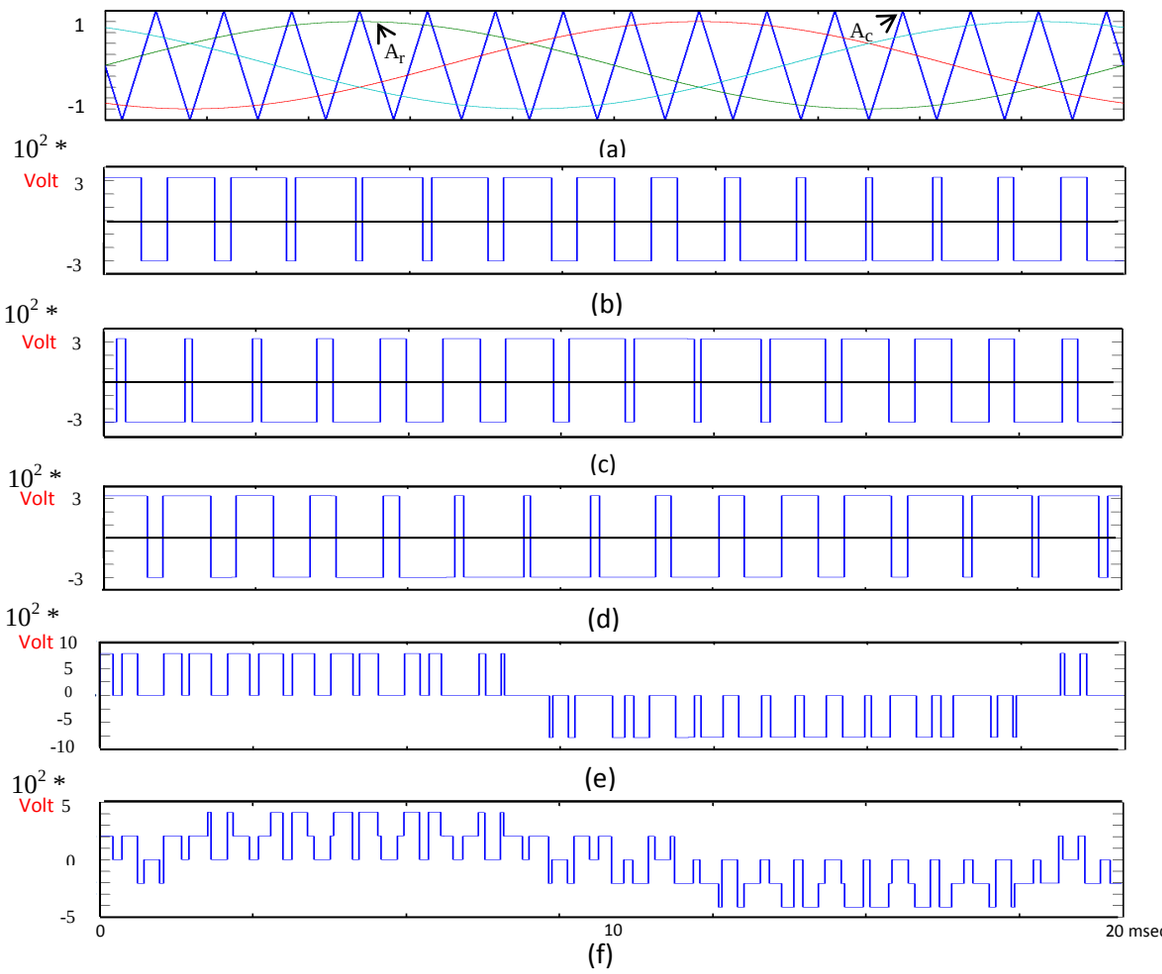
3. خصائص المحرك الحثي

المحرك الحثي ثلاثي الطورشائع الاستخدام في مسوقات ضبط السرعة. إن طريقة السيطرة على المحرك الحثي نوعا ما تكون معقدة وذلك لأن سلوك المحرك الحثي غير خطي. الشكل رقم (4) يمثل الدائرة المكافئة للمحرك الحثي، من خلال الدائرة المكافئة للمحرك الحثي يمكن ايجاد الممانعة الكلية للمحرك الحثي وكما في المعادلة رقم (3).

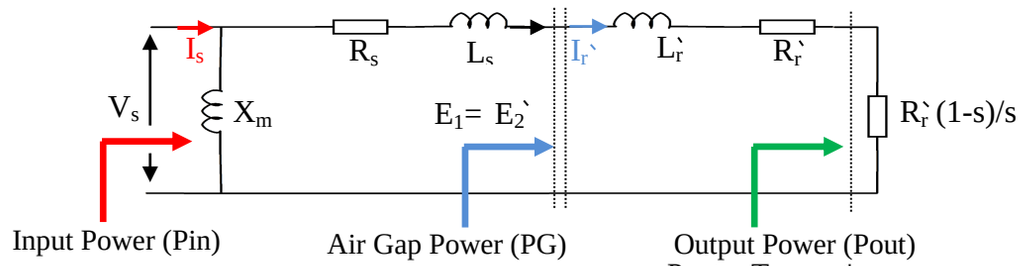
$$Z_{eq} = \left[\frac{Xm^2 * \left(Rs + {Rr'}/{s}\right)}{(Xm+Xs+Xr')^2 + \left(Rs + {Rr'}/{s}\right)^2}\right] + j\left[\frac{Xm * \left[\left(Rs + {Rr'}/{s}\right)^2 + (Xs+Xr)*(Xs+Xr+Xm)\right]}{(Xm+Xs+Xr')^2 + \left(Rs + {Rr'}/{s}\right)^2}\right] \qquad (3)$$

حيث يمثل s معامل الانزلاق، Rr′ و Xr′ تمثلان مقاومة ومفاعلة ملفات الجزء الدوار على الترتيب ومنسوبتين إلى الجزء الثابت، Rs و Xs تمثلان مقاومة ومفاعلة ملفات الجزء الساكن على الترتيب وتمثل Xm المفاعلة المتبادلة.

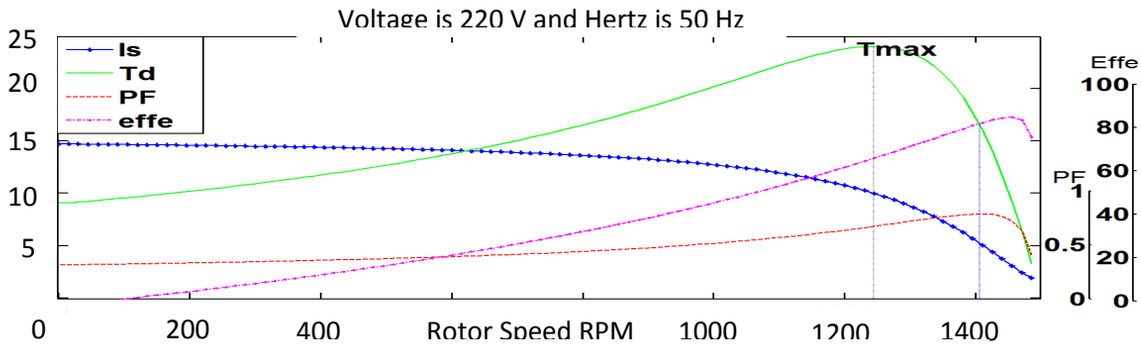
إن خصائص المحرك الحثي مبينة في الشكل (5)، نلاحظ بان المحرك يسلك سلوك غير خطي، وان أعظم عامل قدرة (PF) وأعظم كفاءة (Effe) للمحرك يكونان قريبان عند القيم المقننة للمحرك الحثي . ولكن الحال سيتغير عند تغير في القيم المقننة سواء كان في قيمة السرعة أو العزم أو التردد.



شكل رقم (3) يبين : (a) طريقة القدح، (b,c,d) فولتية الاخراج الطورية للمغير ، (e) فولتية الاخراج الخطية للحمل، (f) فولتية الاخراج الطورية للحمل



شكل رقم(4): الدائرة المكافئة التقريبية للمحرك الحثي لكل طور



شكل رقم (5) : يبين علاقة العزم ، تيار الادخال، الكفاءة وعامل القدرة مع السرعة

4. السيطرة على المحرك الحثي بطريقة E_1/F_S عند نقطة تشغيل اقرب ما يمكن لأعظم كفاءة وعامل قدرة:

من المعادلة رقم (4) نلاحظ بان الفيض (Flux ϕ) هو يتناسب طردياً مع الفولتية المحتثة للساكن(E_1) وعكسي مع التردد(F_S).

$$\phi \ \alpha \ \frac{E_1}{F_s} \qquad (4)$$

في حالة تثبيت الفولتية (E_1) عند القيمة المقننة لها، مع تقليل التردد عن القيمة المقننة للسيطرة على سرعة المحرك الحثي فأن الفيض (ϕ) سوف يزداد، وهذا يؤدي إلى أن عمل المحرك عند منطقة تشبع الفيض المغناطيسي (gab flux) والذي يصاحبه زيادة مفرطة لتيار المحرك، وفي هذه الحالة تكون غير مناسبة وتؤثر سلبياً على جميع مقننات وخصائص المحرك الحثي[10].

أما في حالة زيادة تردد المصدر وبقاء قيمةE_1 ثابتة فأن الفيض سوف يقل ولكن على حساب قيمة العزم والكفاءة كما مبين في المعادلة (5)، علما أن قيم عناصر المحرك تتأثر بقيمة التردد وقيمة الفيض بالنسبة لمُنحني المغنطة.

$$\mathrm{Te} = \frac{3\ \mathrm{Vs}^2\ \mathrm{Rr}'/s}{\mathrm{w_s}\left[\left(\frac{\mathrm{R_r}'}{s} + \mathrm{R_s}\right)^2 + (\mathrm{X_s} + \mathrm{X_r}')^2\right]} \qquad (5)$$

لذا يتطلب الحفاظ على أن يكون عمل المحرك عند قيمة للفيض تقع عند منطقة الركبة لمنحني المغنطة (B-H curve). ويتم ذلك بتغير كل من فولتية أطراف المحرك و التردد (V_S/F_S) بحيث يبقى قيمة الفيض و موقعه عند أفضل حالة تشغيل لمدى واسع من السرع و العزوم.

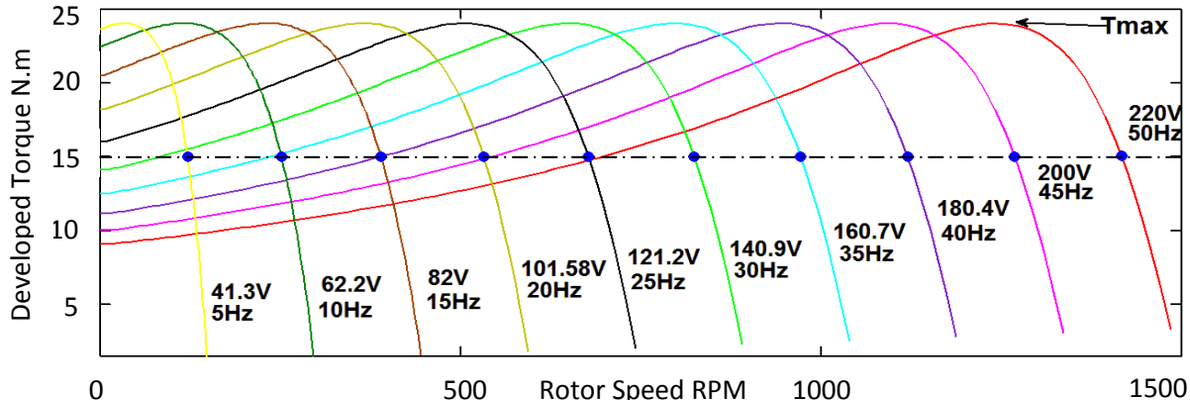
لتحسين اداء مسوق المحرك الحثي، يتم اختيار حالة التشغيل عند اقرب نقطة تكون فيها عامل القدرة للمحرك الحثي أو كفاءة أو عامل انتفاع للقدرة (Power Utilized Ratio) أعظم ما يمكن.

حيث ان أعظم انتفاع للقدرة هو النسبة بين قدرة الإخراج الميكانيكية للمحرك الحثي على اقل قدرة ظاهرية (apparent power) لازمة لتشغيل المحرك الحثي وكما مبين في المعادلة رقم (6):

$$Utilized\ Power\ Ratio = \frac{Tl * W_m}{3 * V_s * I_s} * 100\% \qquad (6)$$

حيث ان:

$Tl = Load\ Torque\ Included\ Mechanical\ Torque\ loss\ N.m$, $W_m = Rotor\ Speed\ (\frac{Rad}{Sec})$,
$Vs = Phase\ Input\ Voltage\ (r.m.s)$, $Is = Phase\ Input\ Current\ (r.m.s)$.



شكل رقم (6): خصائص المحرك الحثي في حالة استخدام السيطرة نوع volt/hertz بتثبيت أعظم عزم

تم الحصول على النتائج والمبينة في الشكل رقم (6) بالاعتماد على قيم عناصر المحرك الحثي (ملحق I) من خلال تثبيت العزم عند أعظم قيمة له ولجميع حالات التشغيل، حيث تم ايجاد أعظم عزم (Tmax) عند الفولتية والتردد

المقننين(Vs,Fs) وبذلك يكون أعظم عزم هو ثابت في حالة تغير السرعة للمحرك الحثي. كما تم تسليط عزم حمل ثابت مقداره 15 Nm لجميع حالات التشغيل وكان أعظم انتفاع للقدرة كما هو موضح بالجدول رقم (1).

جدول رقم (1): يبين نتائج استخدام طريقة التحكم بـ E_1/F_S التقليدية للسيطرة على سرعة المحرك الحثي

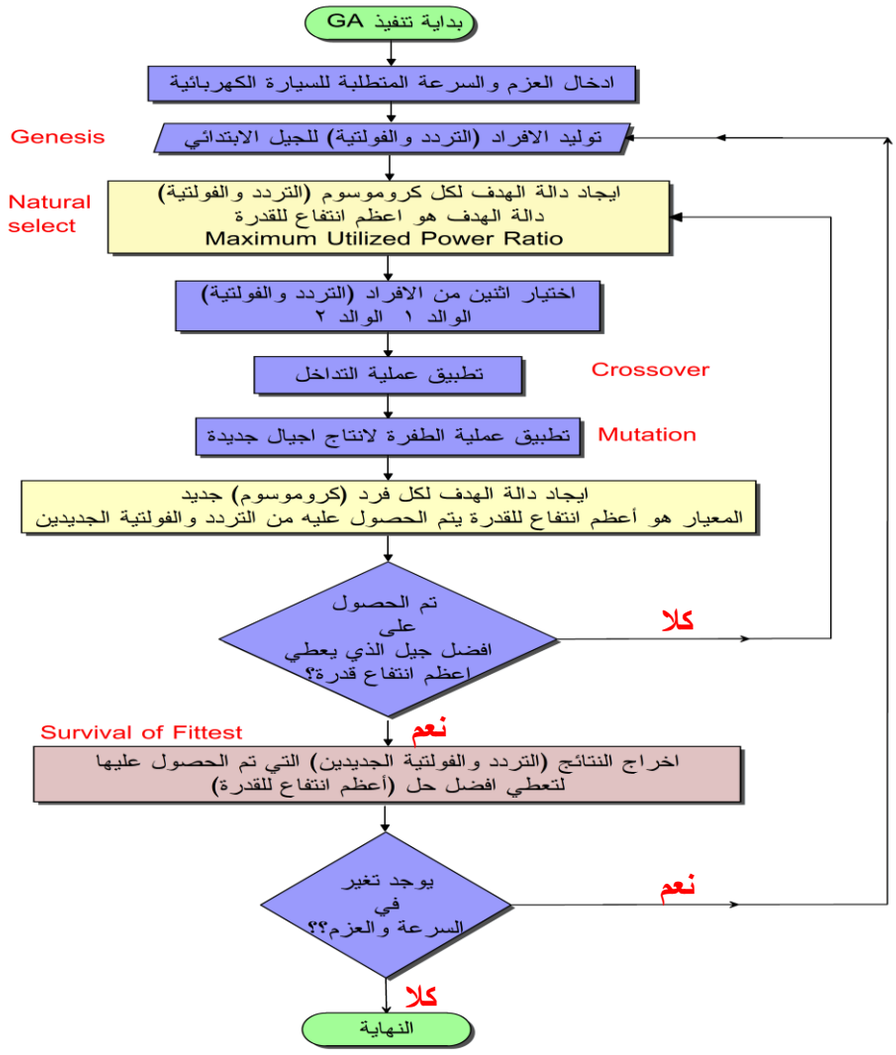
Speed (RPM)	Supply Voltage (r.m.s)	Supply Frequency (Hz)	Ns (RPM)	Load Torque (N.m)	Stator Current (r.m.s)	Power Factor	Efficiency %	power Utilized Ratio %
1417.3	220	50	1500	15	4.7485	0.8022	84.4	67.70
1268.7	200.2	45	1350	15	4.715	0.8015	82.98	66.5
1120	180.42	40	1200	15	4.697	0.8006	81.203	65
971.85	160.66	35	1050	15	4.66	0.799	79.05	63.16
824.25	140.35	30	900	15	4.614	0.7966	76.33	60.80
677.6	121.24	25	750	15	4.55	0.7923	72.833	57.70
532.35	101.58	20	600	15	4.463	0.7843	68.12	53.42
389.5	81.95	15	450	15	4.34	0.7673	61.42	47.12
251.5	62.19	10	300	15	4.16	0.7218	50.94	36.76
121.25	41.26	5	150	15	4.133	0.5644	27.4	15.46

5. استخدام الخوارزمية الجينية للحصول على امثل النتائج:

الخوارزمية الجينية (Genetic Algorithm) هي بحث إرشادي لإجراء عملية التقييم. يمكن أن تطبق في عمليات البحث للحصول على أفضل قيمة للحل، وتعد طريقة الخوارزمية الجينية (GA) إحدى الطرائق الفرعية ضمن طريقة الخوارزميات التطورية التي تستخدم آليات ملهمة من علم الأحياء ونظرية البقاء للأصلح (Survival of The Fittest) بشكل متكرر من اجل انتقاء امثل حل.الخوارزمية الجينية هي طريقة بحث عشوائية تعتمد طريقة عملها على مبدأ النمو والتطور الطبيعي للوصول الى الحل الأمثل وتحتوي الخوارزمية الجينية على كروموسومات (Chromosomes)، جينات (Gene)، مجموعة اجيال (Set of Population)، اللياقة (Fitness)، دالة اللياقة(Fitness Function)، التداخل (Crossover)، الطفرة (Mutation) والاختيار(Selection) [14]. تم استخدام الخوارزمية الجينية (GA) للحصول على نقطة تشغيل مثلى عند أعظم انتفاع للقدرة(Maximum Utilized Power) وضمن المنطقة المستقرة لخصائص العزم مع السرعة للمحرك الحثي وذلك لتحسين من اداء مسوق المحرك الحثي عند جميع حالات التشغيل المختلفة للمحرك. يبين الشكل رقم (7) المخطط الانسيابي لتطبيق برنامج الخوارزمية الجينية-16] [15، حيث يبين المخطط الانسيابي بان الخوارزمية الجينية مكونة من عدة خطوات وهي :

- توليد الافراد (الكروموسومات) للجيل الجديد.
- ايجاد دالة الهدف لكل فرد.
- تعين شرط لإيقاف عملية الحصول على امثل حل.
- الاختيار Selection.
- عرض النتائج للمتغيرات التي تعطي امثل حل.
- التداخلCrossover.
- الطفرة Mutation.
- ايجاد دالة الهدف لأفراد الجيل الجديد.

من الخطوات يتبين بان الخوارزمية الجينية هي طريقة عشوائية في البحث للوصول الى الحل الافضل او الامثل.



شكل رقم (7) : المخطط الانسيابي لتطبيق برنامج الخوارزمية الجينية للسيطرة على المحرك الحثي

6. خطوات الخوارزمية الجينية المستخدمة في البحث:

6.1. تهيئة الجيل الابتدائي(Initial Populations):

المعنى الحقيقي لتوليد الجيل الابتدائي هو عدد الافراد او الكروموسومات في الجيل الواحد، ويعتمد عدد افراد الجيل الابتدائي على صعوبة المشكلة، وافراد الجيل الابتدائي تعطي بعض المعلومات عن فضاء البحث، من الناحية المثالية ينبغي ان يكون اول جيل يمتلك عدد كبير من الجينات من اجل الحصول على اكتشاف فضاء البحث بالكامل ولكن هذا على حساب الزمن[17]. في هذا البحث تم استخدام حجم الجيل هو (50) وذلك من اجل تقليل عدد الاجيال اللازمة لتحقيق القيمة المثلى لأعظم إنتفاع للقدرة.

6.2.اختيار دالة الهدف (Fitness Function):

دالة الهدف هو تحديد الهدف لكل كروموسوم (تحديد الهدف لكل من التردد والفولتية) وتستخدم لتوجيه البحث، حيث تحدد قيمة اللياقة لكل كروموسوم بالاعتماد على قيمة دالة الهدف[14]. نتائج دالة الهدف تعطي احتمالية اختيار الكروموسوم لتوريث خصائصة. بواسطة دالة الهدف نستطيع ان نختار الكروموسومات التي تعطي افضل حل والغاء او حذف الكروموسومات غير الصالحة. تم استخدام دالة الهدف في هذا البحث هو أعظم انتفاع للقدرة والممثلة في المعادلة رقم (6) لحساب أعظم إنتفاع للقدرة بالاعتماد على نسبة القدرة الحقيقية للأخراج على القدرة الظاهرية للإدخال لمحرك الحثي، وبذلك يكون عدد المتغيرات المستخدمة في هذا البحث هو التردد والفولتية المطلوب ايجاد قيمتهما لتحقيق المتطلبات من سرعة وعزم.

$Fitness\ Function:\ Max\ Power\ Utilization\ Ratio\ as\ given\ in\ equation\ (6)$

6.3. القيود أو الشروط (Constraints):

متغيرات الخوارزمية الجينية لها عدد ما لا نهاية من القيم المحتملة، لذلك يتم استخدام حدود أو القيود المثلى، وبدون هذه القيود يسمح للمتغير لأخذ أي قيمة. تضمن القيود المثلى بأن يكون المتغير في حالة مساواة وعدم مساواة في دالة الهدف، وبذلك تكون نتائج الخوارزمية الجينية بالاعتماد على القيود المثلى[14]. في حالة كل الكروموسومات لم تحقق شروط القيد المثلى فأنه يتم تكرار العملية لأكثر من جيل[17].

تم استخدام القيود المثلى في هذا البحث لضمان أن يكون مجال البحث عن أفضل حل هو ضمن المنطقة المستقرة لخصائص العزم مع السرعة، وذلك عن طريق اشتقاق معادلة العزم مع السرعة للمحرك الحثي كما في المعادلة رقم (7).

$$\frac{dTe}{dNr} = \frac{90}{\pi} * \left(\frac{V_s}{N_s}\right)^2 * Rr * \left(\frac{s * \left[\left(Rs + \frac{Rr}{s}\right)^2 + (Xs + Xr)^2\right] - 2 * Rr\left(Rs + \frac{Rr}{s}\right)}{s^3 * \left[\left(Rs + \frac{Rr}{s}\right)^2 + (Xs + Xr)^2\right]^2} \right) \quad (7)$$

حيث أن

$$s = \frac{N_s - N_r}{N_s}, \quad N_r = Rotor\ Speed\ (r.p.m), \quad N_s = Synchronous\ Speed\ (r.p.m),$$

$$N_s = \left(120 * \frac{Fs}{P}\right)$$

عندما يكون عزم الحمل ثابت مع تغير السرعة، فأن مشتقة عزم الحمل بالنسبة لسرعة المحرك الحثي يساوي صفر، اذا فأن مشتقة العزم الذي يولده المحرك الحثي يجب أن يكون اقل من صفرللحصول على نقطة عمل في المنطقة المستقرة. أو بشكل عام، لضمان أن تكون نقطة العمل مستقرة يجب أن تتحقق العلاقة الآتية:

$$\frac{\mathrm{d}Te}{\mathrm{dNr}} \leq \frac{\mathrm{dTL}}{\mathrm{dNr}} \quad (8)$$

6.4. دالة الاختيار(Selecting Function)

عملية اختيار آباء من الكروموسومات في الجيل(اختيار كل من التردد والفولتية التي تعطي نتائج مثلى)لإنتاج نسل جديد (New Offspring)، وتتم عملية الاختيار بالاعتماد على معيار في التقييم للكروموسومات، أي تكون عملية الاختيار على حسب لياقة الكروموسومات التي تم تقيمها مسبقا، حيث تختار الخوارزمية الجينية الكروموسومات عالية اللياقة لتوليد جيل جديد يمتلك حلول مثلى، في هذا البحث تم العمل على طريقة عجلة روليت(Roulette wheel)، في هذه الطريقة يتم اختيار الآباء على أساس اللياقة، وأفضل لياقة للكروموسوم يمتلك أكثر من فرصة ليكون أب، وهذه الطريقة شائعة الاستخدام لاختيار اللياقة المناسبة. يتم تعين كل فرد في شريحة دائرية لعجلة روليت، وحجم الشريحة يتناسب مع اللياقة للكروموسومات[14].

6.5. التداخل الإبدالي(Crossover)

عملية التداخل الإبدالي هي عملية اختيار الجينات من كروموسومات الأصل (Parent) (فولتية وتردد قديمين) لإنتاج نسل جديد (Offspring)(فولتية وتردد جديدين) يحمل صفات وراثية مشتركة من كروموسومات الأصل[14-19]، في حالة عدم وجود عملية تداخل ابدالي فأن الجيل الجديد سوف يكون نسخة طبق الأصل من الجيل القديم. في هذا البحث تم استخدام التداخل الإبدالي نوع الإرشادي(Heuristic Crossover) وذلك لأن هذا النوع من التداخل الابدالي يستخدم مع الخوارزمية الجينية المستمرة، وتستخدم قيم اللياقة في حساب اتجاه البحث وتنتج نسل واحد. يكون عمل الطريقة الإرشادية هو استخدام قيم اللياقة لكلا الأبوين من الكروموسومات لمعرفة اتجاه البحث.

6.6. الطفرة (Mutation)

عملية الطفرة تحدد كيفية إجراء الخوارزمية الجينية تغيرات صغيرة على مقطع الكروموسوم في الجيل وتكوين كروموسوم جديد يمتلك حلولاً عديدة، وتوفر الطفرة تنوع جيني وتمكن الخوارزمية الجينية للبحث في فضاء أوسع[20]. في الخوارزمية الجينية المستمرة يتم اختيار الكروموسوم عشوائيا لتطبق عليه الطفرة.

7. نتائج الخوارزمية الجينية

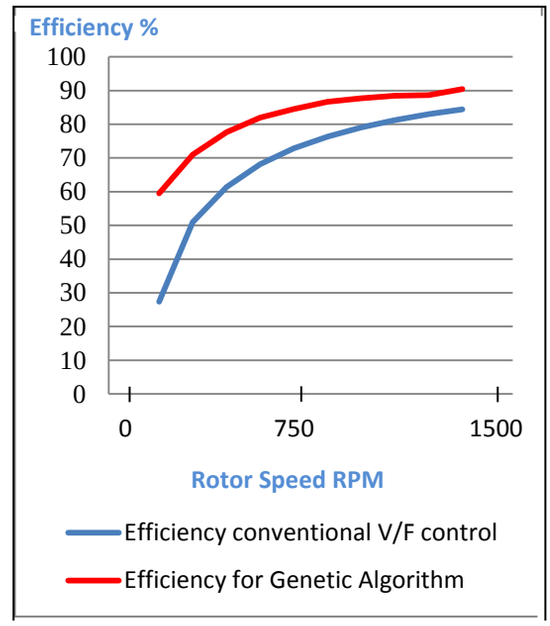
تم الحصول على نتائج الخوارزمية الجينية كما هو مبين في الجدول رقم (2)

جدول رقم (2) : يبين نتائج استخدام الخوارزمية الجينية للسيطرة على سرعة المحرك الحثي

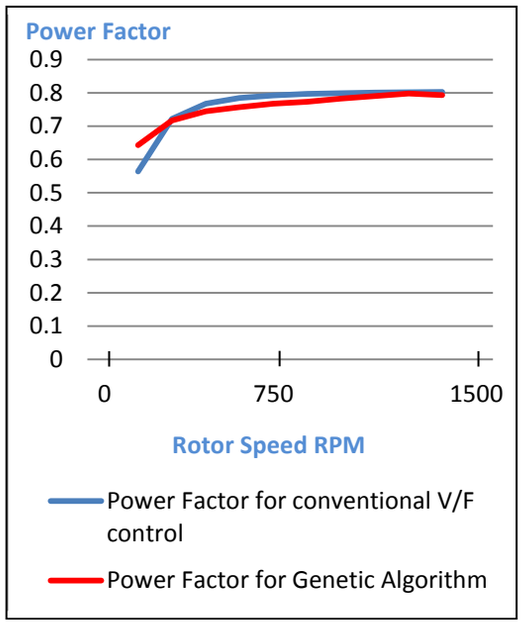
Speed (RPM)	Supply Voltage(r.m.s)	Supply Frequency (Hz)	Ns (RPM)	Load Torque (N.m)	Stator Current (r.m.s)	Power Factor	Efficiency %	power Utilized Ratio %
1417.3	232.72	49.55	1486.5	15	4.445	0.7932	90.4	71.73
1268.7	205.5	44.78	1343.4	15	4.568	0.7976	88.69	70.75
1120	190	39.59	1187.7	15	4.416	0.7902	88.42	69.86
971.85	171.59	34.5	1035	15	4.32	0.7827	87.66	68.61
824.25	151.95	29.4	882	15	4.27	0.7733	86.67	67.03
677.6	129.66	24.5	735	15	4.21	0.7678	84.51	64.89
532.35	107.7	19.5	585	15	4.17	0.7569	81.96	62.04
389.5	84.79	14.7	441	15	4.16	0.7446	77.66	57.82
251.5	62.07	9.9	297	15	4.15	0.7196	71.01	51.1
121.25	41.74	4.93	147.9	15	4.13	0.5423	67.8	36.77

العلاقة بين الكفاءة، عامل القدرة، تيار الإدخال والانتفاع في القدرة للمحرك الحثي مع السرعة باستخدام طريقة E_1/F_S وباستخدام طريقة Genetic Algorithm موضحه في الأشكال (8-11) على التوالي.

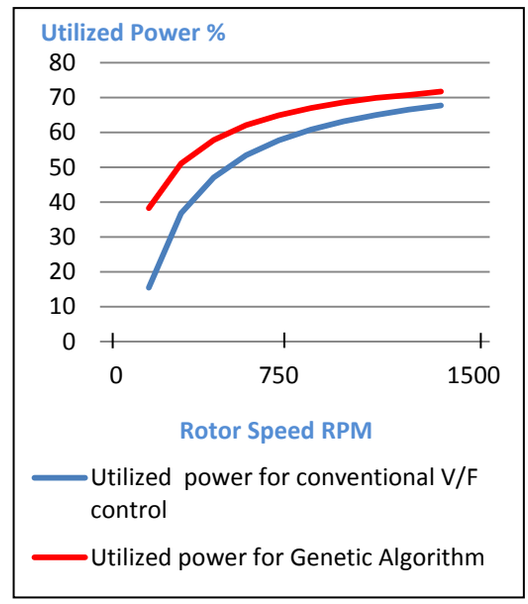
يبين الشكل (12)، الطاقة المسحوبة من البطارية (عند استخدام المسوق) لمدى واسع من السرع وباستخدام طريقة السيطرة نوع E_1/F_S وطريقة الخوارزمية الجينية للحصول على أعظم انتفاع للقدرة. حيث تم حساب الطاقة المسحوبة من البطاريات عن طريق ضرب التيار الأني والفولتية الأنية وذلك للحصول على القدرة الأنية المسحوبة من البطاريات لفترة زمنية معينة كما هو موضع في المعادلة رقم (9).



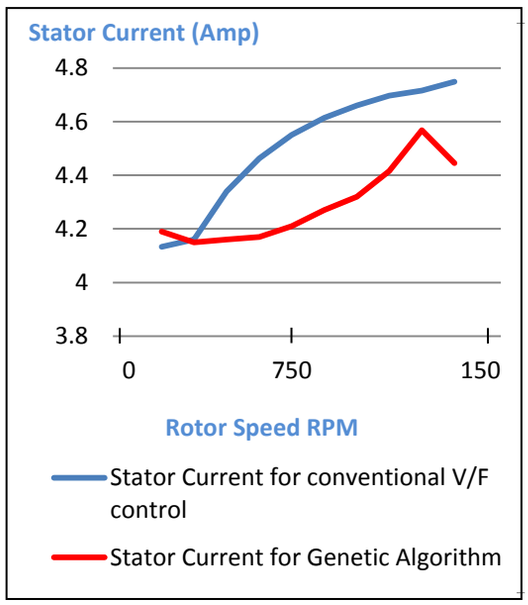
شكل (8) : يوضح العلاقة بين الكفاءة للمحرك الحثي مع السرعة باستخدام طريقة E_1/F_S وطريقة الخوارزمية الجينية



شكل (9) : يوضح العلاقة بين عامل القدرة للمحرك الحثي مع السرعة باستخدام طريقة E_1/F_S وطريقة الخوارزمية الجينية



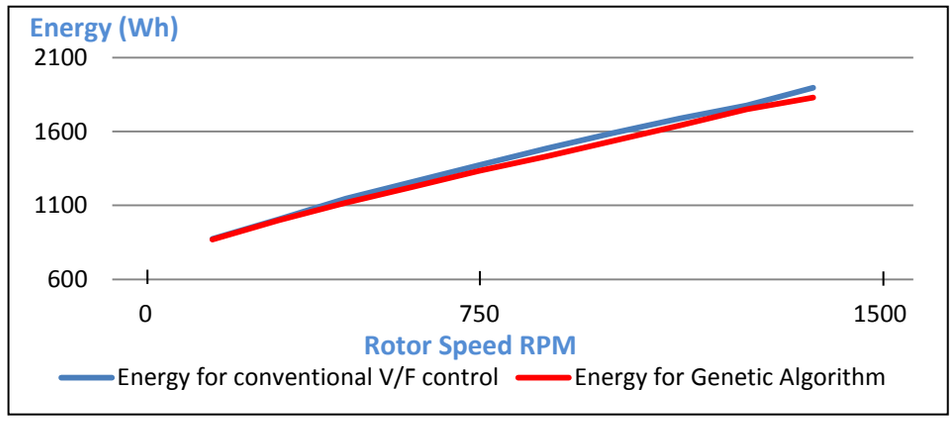
شكل (10) : يوضح العلاقة بين أعظم انتفاع للقدرة باستخدام طريقة E_1/F_S وطريقة الخوارزمية الجينية



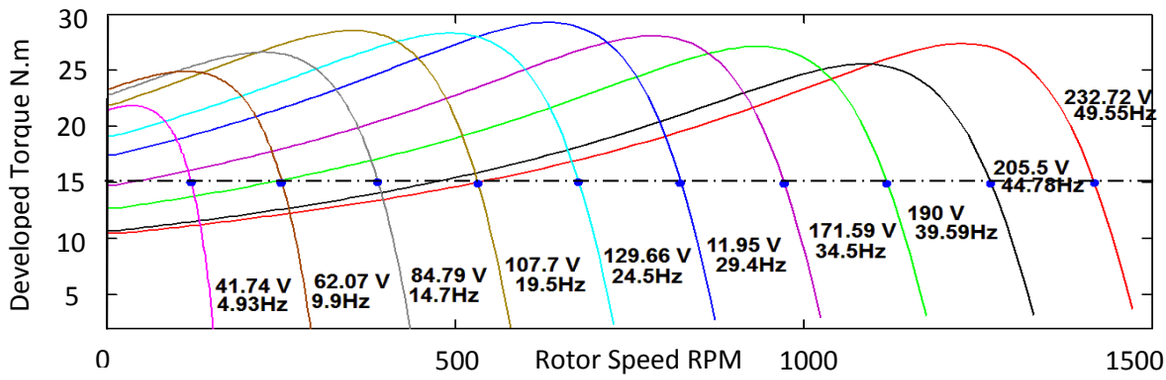
شكل (11) : يوضح العلاقة بين تيار الادخال باستخدام طريقة E_1/F_S وطريقة الخوارزمية الجينية

$$Energy\ (wh) = \int v_{(t)}\, i_{(t)}\, dt \qquad (9)$$

يبين الشكل (13) خصائص العزم مع السرعة للمحرك الحثي باستخدام الخوارزمية الجينية بتتبع أعظم انتفاع للقدرة لجميع نقاط التشغيل.



شكل (12) : يوضح العلاقة بين الطاقة المسحوبة من البطارية مع السرعة للمحرك الحثي باستخدام طريقة E_1/F_S وطريقة الخوارزمية الجينية



شكل (13): خصائص المحرك الحثي في حالة استخدام الخوارزمية الجينية

8. الاستنتاجات

استخدم مغير مصدر الفولتية VSI ثلاثي الطور للتحكم بقيمة الفولتية والتردد من اجل السيطرة على سرعة المحرك الحثي ثلاثي الطور وحسب الاستراتيجية المتبعة، كما تم استخدام تقنية تضمين عرض النبضة الجيبي SPWM لسوق المغير VSI وتقليل تأثير التوافقيات الناجمة عن استخدام المغير VSI والذي يساهم بدوره أيضا في تقليل استهلاك الطاقة استخدم في هذا البحث الطريقة التقليدية E_1/F_S تارة، وطريقة الخوارزمية الجينية للحصول على أعظم انتفاع للقدرة للسيطرة على المحرك الحثي ثلاثي الطور تارة أخرى وتمت مقارنة النتائج للطريقتينلحالة التشغيل التي تتناسب مع طبيعة السيارة الكهربائية كحمل. حيث تبين بأن طريقة السيطرة باستخدام الخوارزمية الجينية أفضل من الطريقة التقليدية E_1/F_S من حيث أعظم انتفاع للقدرة واقل خسائر للطاقة المسحوبة من البطاريات، وهذا يساهم في خزن الطاقة في البطاريات لفترة أطول وهذا ينعكس ايجابيا على إمكانية زيادة المسافة التي تقطعها السيارة الكهربائية قبل إعادة شحن البطارية مرة أخرى.

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الملحق I

محرك حثي ثلاثي الطور بقدرة 3.25 HP
نوع الربط نجمي ، تردد 50 Hz.
الفولتية الخطية المقننة 380 Volt، عدد الاقطاب 4.
الشركة المصنعة :ELPROM HARMANLI.
البلد المصنع: Bulgaria.

قيم عناصر الماكنة الحثية:

Rs =3.20 ohm/phase , Ls =2.5mH/phase, Rr'= 2.75 ohm/phase, Lr' =2.5mH/phase, Lm= 41mH/phase.

Performance Enhancement Of DC Motor Speed Control By Using Model Reference Adaptive ANN Control

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Abstract

In this paper adaptive Artificial Neural Network(ANN) has been implemented to control both the speed and armature current of separately excited DC motor with chopper as drive circuit. The ANN controller strategies which has been used in the implementation are Model Reference Adaptive Control (MRAC), Nonlinear Auto Regression Moving (NARMA_L2) and ANN based on Proportional-Integral (PI) controller. Prior controller the plant identification of a DC motor has been trained. The constructed ANN controller reject the effect of load on the shaft of the motor and the nonlinearity in the drive system. The performance of these new controllers has been verified through simulation using MATLAB/SIMULINK package, the results show good and high performance in time domain response, and fast reject of the disturbance affected on the system as compared with conventional PI controller. The sharpness of the speed output with minimum overshoot defines the precision of the proposed drive. The settling time has been reduced to a label of 0.2 sec.

Keywords: DC motor, ANN, PI Controller, NARMA-L2 Controller and MRAC Controller

تعزيز أداء وتحديد السرعة لمحرك التيار المستمر باستخدام النموذج المرجعي التكيفي لمسيطر الشبكات العصبية الاصطناعية

شامل حمزة حسين

قسم الهندسة الكهربائية / جامعة الموصل

المستخلص

في هذا البحث تم تنفيذ الشبكات العصبية الاصطناعية التكيفية للتحكم في كل من السرعة وتيار المنتج لمحرك التيار المستمر منفصلة الاثارة مع استخدام دائرة لسوق المحرك. استراتيجيات الشبكة العصبية التي تم استخدامها في هذا البحث هي الشبكة العصبية الاصطناعية ذات سيطرة الاشارة المرجعية التكيفية (MRAC)، وذات الارتداد الالي المتنقل الغير الخطي وذات السيطرة المستندة على مبدأ مسيطر التناسبي–التكاملي. تم تمثيل وتدريب الشبكة العصبية للتطابق التام لمحرك تيار المستمر من خلال برنامج المحاكاة الماتلاب وكان اداء الشبكة العصبية المقترحة جيد للرد على تأثير الحمل المسلط على استجابة المحرك وتأثير عامل اللاخطية في دائرة السوق للمحرك. في هذا البحث إذ تبين نتائج استخدام الشبكة العصبية الاصطناعية التكيفية جيدة جداً وذات اداء عالي للمحرك في استجابة الحيز الزمني، والرد السريع للعوائق الخارجية التي تؤثر على المنظومة مقارنة مع استخدام المسيطرات التقليدية. وحصلنا على استجابة جيدة لسرعة المحرك مع الحد الادنى من قيمة التذبذب لا شارة السرعة والذي يحدد دقة اختيار دائرة السوق، وحصلنا على زمن الثبوت (زمن الاستقرار) اقل ما يكمن بحدود 0.2 sec عند استخدام مسيطر الشبكات العصبية المبنية على النموذج المرجعي التكيفي.

1- Introduction

The separately excited direct current (DC) motors are widely implemented in industries as open loop and closed loop speed control in other words, tracking of the command speed is the most important aim in industrial tools with fast and good dynamic performance. The conventional Proportional-Integral (PI) speed controller is widely implemented to attain the speed control, but they suffer from poor performance specially if there are uncertainty in the parameters and nonlinearity in this system. This controller can be easily implemented but it is found to be highly effective reject if the load changes are small[1]. The main construction of the closed loop speed control system are drive circuit and the controller. They must be designed and chosed such that to reduce energy consumption with high efficiency and high performance[2]. The recent and more beneficial drive circuit is the static converters which enhance the performance of the system, like Buck converter.

The speed of separately excited DC motor can be controlled by types of adaptive ANN controller and up to rated speed using chopper as a converter, the chopper firing circuit receives signal from controller and then the chopper gives variable voltage to the armature of the motor for achieving desired command speed[3]. The recent controllers was used by authors the intelligent controllers such as Expert system, Neural network and Fuzzy controller. Then the adaptive ANN controller was implemented to real time speed control of a DC Motor [4][5]. The artificial intelligent controller which emulate the human being brain using neural network applications may take the form of intelligent PI controllers has been applied for speed control of the motor[6]. Besides the controller, the neural network can be used as an identification of the plant and control of a dynamical systems and as special case DC Motor speed control[7]. The adaptive neural network controller is another branch of the intelligent control which is self-adapted to reject any perturbation on the system due to nonlinearity in system and when there are such uncertainty in the system parameters.

The adaptive neural network with multilayer can be applied as two strategies, one of these strategies the identification of the plant and the is the construction of the neural network controller. The main three typical commonly used adaptive neural network controllers are model predictive control, NARMA-L2 control, and model reference control, these controllers are representative of the variety of common ways in which multilayer networks are used in control systems [7].

The authors of paper [8] mainly deal with controlling DC motor speed using chopper as power converter and PI as speed and current controller, they show that the results of the PI based speed control has many advantages like fast control, low cost and simplified structure.

In this work the artificial neural network ANN has been implemented as adaptive neural network controller, models are model reference adaptive controller (MRAC) and Nonlinear auto regression moving (NARMA_L2) for both speed and current controller based on PI Controller. The training method of these controllers depended on priorly plant identification and deduced the neural network controller which has been forecasted from the system training behavior. in addition the drive circuit which has been implemented is a Buck converter with IGBT power transistor as switching network such that the constrained peak to peak ripples current and voltage has been verified.

2- Chopper Converter

A chopper is a static power electronic device that converts fixed dc input voltage to a variable dc output voltage. A Chopper may be considered as dc equivalent of an ac transformer since they behave in an identical manner. As chopper involves one stage conversion, these are more efficient, Chopper systems offer smooth control, high efficiency, faster response and regeneration facility, The power semiconductor devices used for a chopper

circuit can be force commutated thyristor, power BJT, MOSFET and IGBT. GTO based chopper are also used. These devices are generally represented by a switch. When the switch is off, no current can flow. Current flows through the load when switch is "on". The power semiconductor devices have on-state voltage drop of 0.5V to 2.5V across them. For the sake of simplicity, this voltage drop across these devices is generally neglected [2].

In this work buck converter (DC chopper) has been implemented that represented a step down the voltage converter , The buck converter consists of a switch network that reduces the dc component of voltage, and a low-pass filter that removes the high-frequency switching harmonics. The power transistor type IGBT (Isolated Gate Bipolar Transistor) which used a switch network depended on the duty cycle of the PWM signal coming from controller circuit, The block diagram as shown below Fig.1 represented the construction of the buck converter.

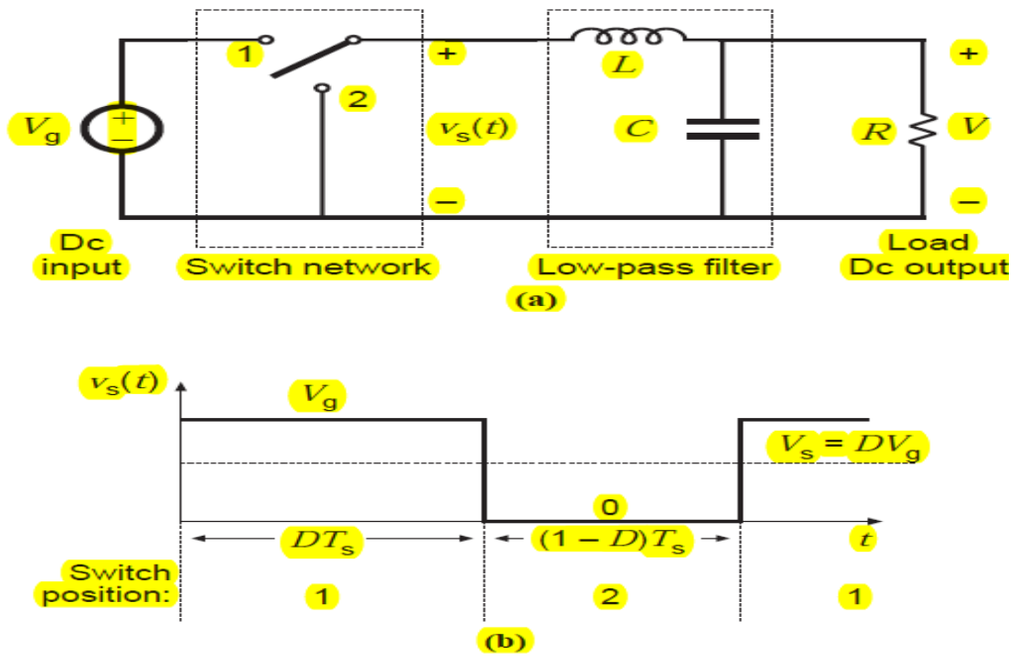

Fig. (1): Block diagram of the buck converter
a) Schematic b) Switch voltage waveform

The buck converter reduces the dc voltage and has conversion ratio $M(D)=D$. This converter produces an output voltage V that is smaller in magnitude with the input voltage V_g. The Fig.2. as shown below refers to DC conversion ratios $M(D) = V/V_g$. of the buck converter.

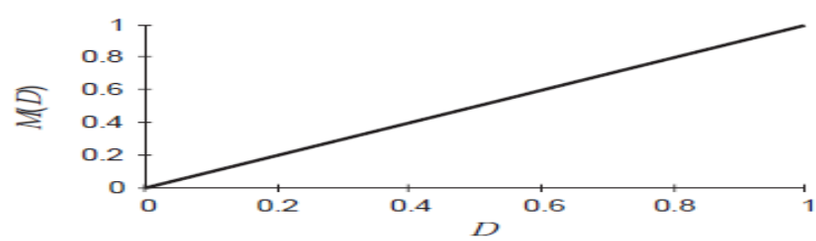

Fig. (2): DC conversion ratios $M(D) = V/V_g$ of buck converter

The Buck converter transfer function has been calculated by two parts the first part when switch is ON (D=1) of IGBT power transistor and the other part when switch is OFF (D=0) of its power transistor.

When D=1.0

$$\frac{di(t)}{dt} = \frac{D}{L} vg - \frac{1}{L} vc \quad (1)$$

$$\frac{dvc(t)}{dt} = \frac{1}{c} iL - \frac{1}{Rc} vc \quad (2)$$

When D=0.0

$$\frac{di(t)}{dt} = -\frac{1}{L} vc \quad (3)$$

$$\frac{dvc(t)}{dt} = \frac{1}{c} iL - \frac{1}{Rc} vc \quad (4)$$

The state space model formula $\dot{X} = AX + BU$ and output $Y = CX$ of this converter has been represented as shown below.

$$\begin{bmatrix} IL \\ VC \end{bmatrix} = \begin{bmatrix} 0 & -1/L \\ 1/c & -1/Rc \end{bmatrix} \begin{bmatrix} iL \\ vc \end{bmatrix} + \begin{bmatrix} D/L \\ 0 \end{bmatrix} \text{vg} \quad (5)$$

The parameters of the Buck converter as shown below: vg=220volt, L=8.5Mh and C=220μf. This parameters has been chosen depending on peak to peak ripple current of the inductance as shown in equation (6) and peak to peak ripple voltage of the capacitance as shown in equation (7).

$$\Delta IL = \frac{Vg * D(1-D)}{f * L} \quad (6)$$

$$\Delta VC = \frac{Vg * D(1-D)}{8 * L * c * f^2} \quad (7)$$

The switching frequency which has been used in this work equal to 8KHZ that gives the required peak to peak ripple current and required peak to peak ripple voltage respectively $\Delta IL = 0.808$, $\Delta VC = 0.0575$, the factor $\frac{\Delta IL}{I_o} = 11.5\%$ which is allowable range $\frac{\Delta IL}{I_o} \leq 15\%$.

Then the transfer function of Buck converter as shown in equation (8) [12].

$$\frac{Vo}{Vg} = \frac{5.348e005}{s^2 + 1818s + 5.348e005} \quad (8)$$

3- Modeling of DC Motor Load Connected System (transfer function approaches)

During the starting of separately excited D.C. motor, its starting performance is affected by its nonlinear behavior. For controlling the speed of DC motor, PI control strategy is applied with current controller and speed controller.

The modeling of DC machine, the transfer function model of DC chopper converter controlled DC motor drives and conventional PI controllers for the speed control of a DC motor has been reported in literature. The ANN based controller is also useful for improving the performance of the motor over PI controllers. A simulink model has been developed to test

the performance of the ANN controller approach and conventional PI controller mode on DC motor drive. The transfer function model of motor and load are shown below Fig.3 [9].

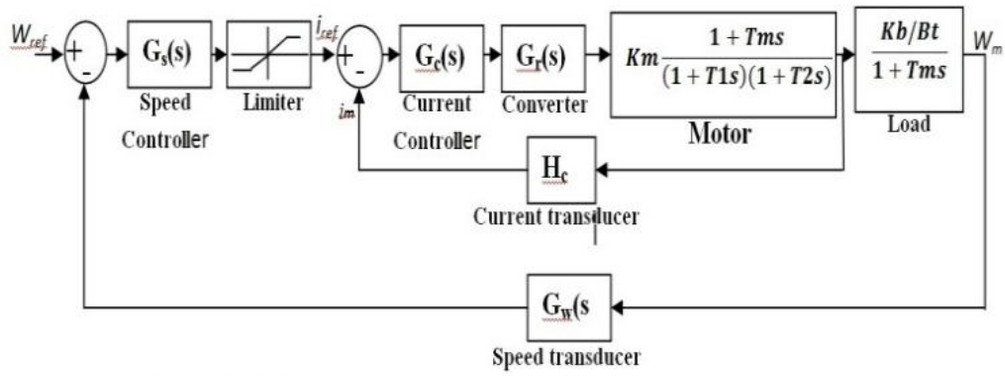

Fig. (3): Block diagram of the motor-load coupled drives (A transfer function model)

The Tacho-generator (speed transducer) has the transfer Function as shown in equation (9).

$$G_w = \frac{1}{1+0.002s} \quad (9)$$

The speed reference voltage has a maximum of 220V. The maximum current permitted in the motor is 20 A and other specification of a DC motor was used in this paper are shown in appendix A. The separately excited DC motor is described by the following equations:

$$KFw_p = R_a i_a(t) - L_a \frac{di_a(t)}{dt} + V_t(t) \quad (10)$$

$$KFi_a(t) = J\frac{dw_p(t)}{dt} + Bw_p(t) + T_L(t) \quad (11)$$

Where,

$\omega_p(t)$ - Rotor speed (rad/s)
V_t (t) - Terminal voltage (V)
$I_a(t)$ - Armature current (A)
$T_L(t)$ - Load torque (Nm)
J - Rotor inertia (Nm^2) = 0.04 Nm^2
KF - Torque & back e.m.f constant (NmA^{-1}) =1.4NmA^{-1}
B - Viscous friction coefficient (Nms)=0.0005 Nms
R_a - Armature resistance (Ω)=2.5 Ω
L_a - Armature inductance (H)=37.2mH.

From these above equations, the mathematical model of the motor can be created. The model is presented in Fig.4. Where (Ta) is the time constant of motor armature circuit Ta=La/Ra in (sec). and (Tm) is the mechanical time constant of the motor Tm=J/B (s).

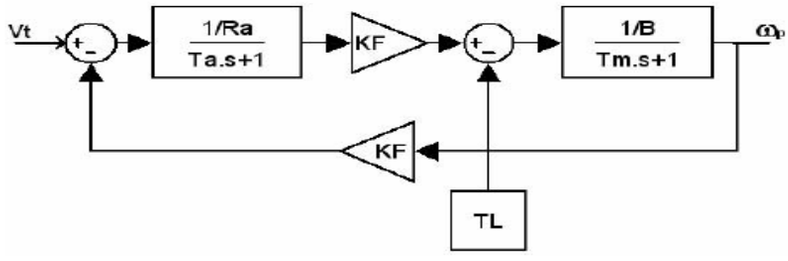

Fig. (4): The mathematical model of a separately excited DC motor

The transfer function of all subsystems of given plant model are taken as per [1][9]. Now the transfer functions of different sub-systems of speed controlled DC drives plant model are:

$$Motor = Km\frac{\mathbf{1+\tau s}}{(\mathbf{1+T_a s})(\mathbf{1+T_m s})} = 1.4\frac{1+0.7s}{0.001488s^2+0.1s+1.9613} \quad (12)$$

$$Load = \frac{Kb/Bt}{(1+T_m s)} = \frac{\frac{1.4}{0.0005}}{1+0.7s} \quad (13)$$

$$converter = \frac{Kr=5.348e005}{s^2+1818s+5.348e005} \quad (14)$$

$$current\ transducer = H_c = 0.1\ volt/amper \quad (15)$$

$$Gc(s) = Kc\frac{(1+T_c s)}{T_c s} = 0.017\frac{(1+0.0148s)}{0.0148s} \quad (16)$$

$$Gs(s) = Ks\frac{(1+T_s s)}{T_s s} = 28.73\frac{(1+0.0188s)}{0.0188s} \quad (17)$$

Where Ks, Kc, Km, Kr, are the gain of speed controller, current controller, motor and converter. Tm, Tc ,Ts and Tr are the time constant for motor, current controller, speed controller and converter plant and Gs, Gw, Gc and Hc are the speed controller, speed controller feedback gain, current controller gain, current feedback gain respectively [1]. The basic principle behind the motor speed control is that the output speed of the motor can be varied by controlling armature voltage for speed below and up to rated speed keeping field voltage constant.

The output speed is compared with the reference speed and error signal is fed to speed controller. Controller output will vary whenever there is a difference in the reference speed and the speed feedback. The output of the speed controller is the control voltage Ec that controls the operation duty cycle of (here the converter used is a Chopper) converter [2][10].

The converter output give the required Va required to bring motor back to the desired speed [10].

4- Simulink Plant Models

a. Conventional PI Control Using Current And Speed Control

In the both control strategy, the current control and speed control are applied for improving the performance of DC motor drive. The response shows that the speed of motor can achieve the steady state value with an a small time. The settling time of motor drive is reduced by applying the both control strategy. Fig.5(a) represent the all block diagram of both controller strategies, the armature current control and speed control for DC motor by using conventional PI controller. The Fig.5 (b) show the response of speed control per unit for DC motor by using both controller strategies as mentioned above.

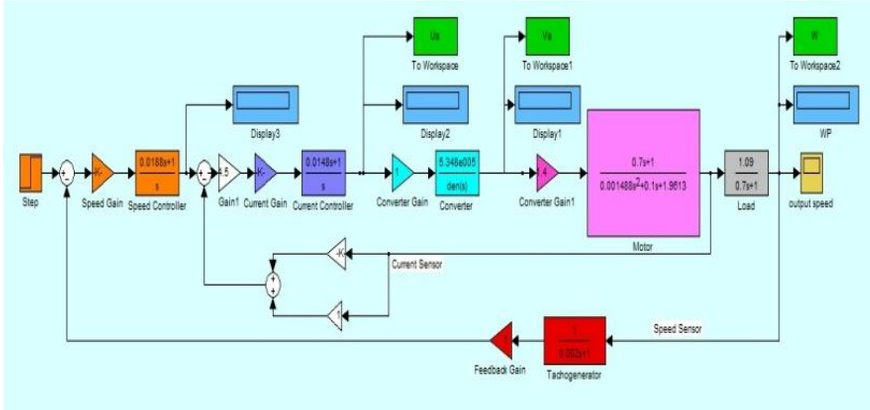

Fig. 5 (a): Simulink plant model with speed and current control strategy

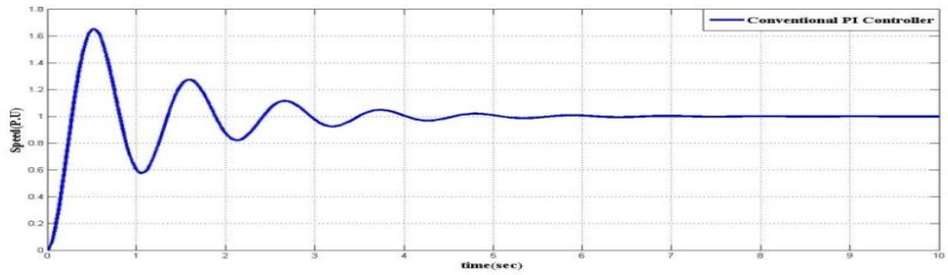

Fig. 5 (b): Output speed with current and speed control strategy

b. Ad*a*ptive ANN Based intelligent PI controller

- **Model reference adaptive control (MRAC)**

The Model Reference Adaptive Control (MRAC) configuration uses two neural networks, a controller network and a model network as shown in Fig.6.

The model network can be trained off-line using historical plant measurements. The controller is adaptively trained to force the plant output to track a reference model output. The model network is used to predict the effect of controller changes on plant output, which allows the updating of controller parameters [11][12].

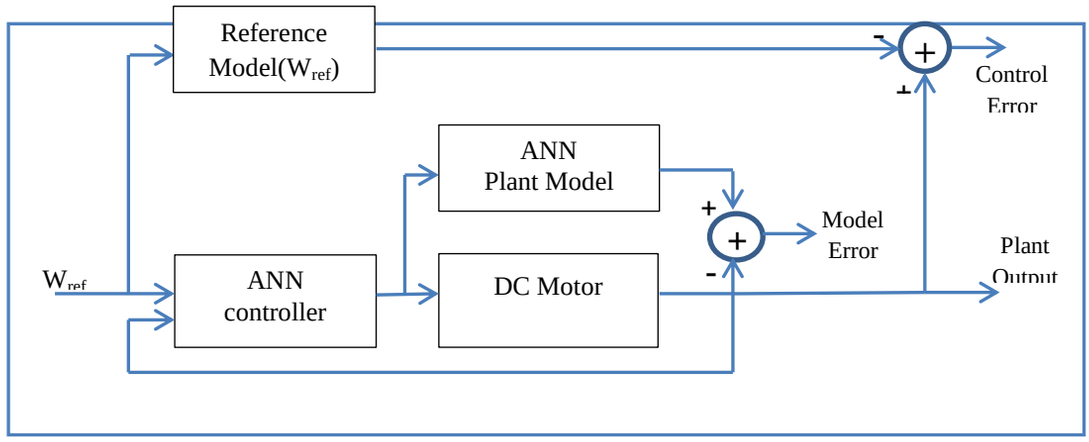

Fig. (6): Internal Configuration of Model Reference Adaptive Control

In this work, MRAC controller like PI controller was used to enhance the performance of DC motor. The ANN controller has been used to generate the control signal for converters to control the speed of motor according to the plant output. The control signal according to plant output was generated by trained ANN on the basis of plant identification[1]. The block diagram as shown in Fig.7 represents comparison between Conventional PI Controller and MRAC ANN controller. Fig. 8 shows the result of the comparison as mentioned above.

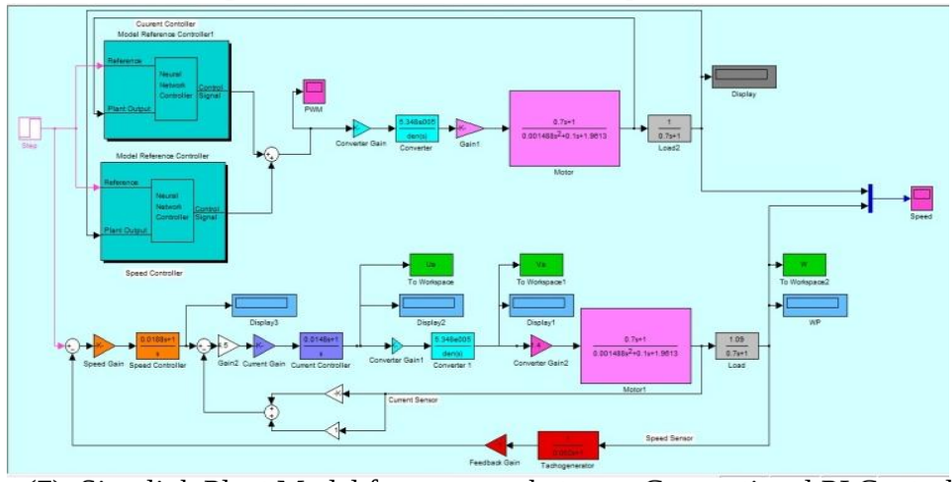

Fig. (7): Simulink Plant Model for compare between Conventional PI Controller and current, speed control strategy using ANN (MRAC) like PI controller

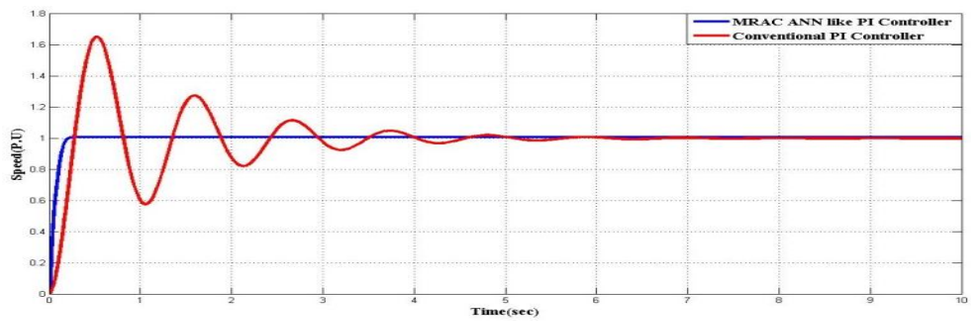

Fig. (8): Compare results between conventional PI Controller and MRAC like PI Controller

The Neural network specifications are given in Table 1. The results show that the response of the system is better than the conventional PI current controller. The settling time and steady state error is further reduced effectively. the reference model input and output of ANN (MRAC)as shown in Fig. 9.

Table 1: ANN(MRAC) Plant Specification

ANN plant specification	
Number of inputs	3: are [$W_{ref}(t)$, $W_{ref}(t-1)$ and $W_{ref}(t-2)$]
Number of outputs	2: are [controlled output and Plant output]
Number of hidden layer	2
Number of training samples	500

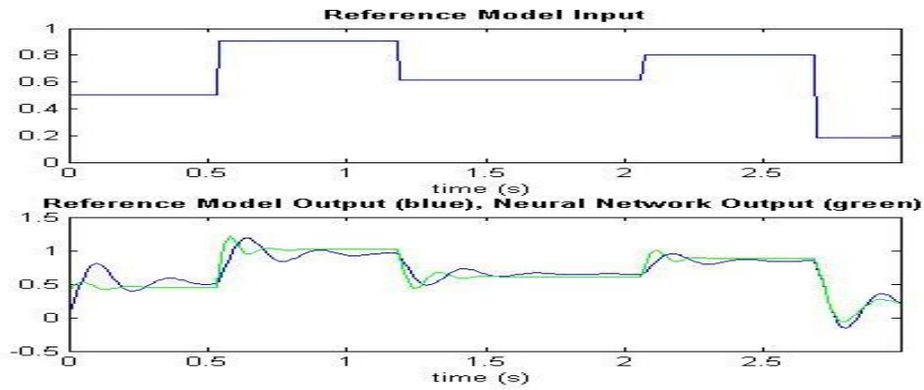

Fig. (9): Reference model input and output of ANN(MRAC)

- **Nonlinear auto regression moving (NARMA_L2)**

The neural adaptive feedback linearization technique is based on the standard feedback linearization controller. An implementation is shown in Figure 10. The feedback linearization technique produces a control signal with two components. The first component cancels out the nonlinearities in the plant, and the second part is a linear state feedback controller, as shown in Fig. 10. [11][12][13]. The central idea of this type of control is to transform nonlinear system dynamics into linear dynamics by canceling the nonlinearities [14].

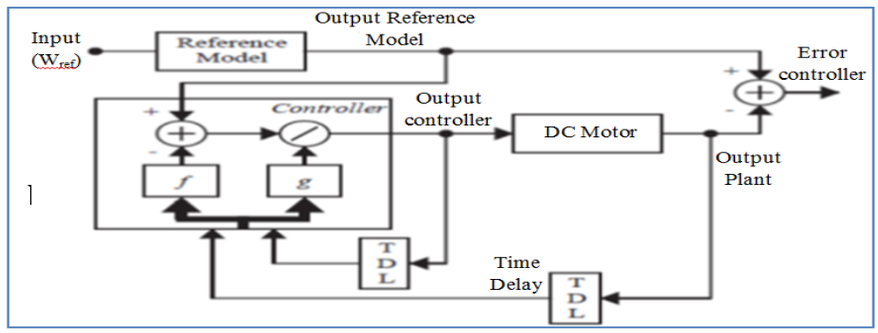

Fig. (10): Neural Adaptive Feedback Linearization

The block diagram as shown in Fig.11. represented compares between Conventional PI Controller and NARMA_L2 neural network like PI Controller. The Fig.12. refer to the result of this comparison as mentioned above.

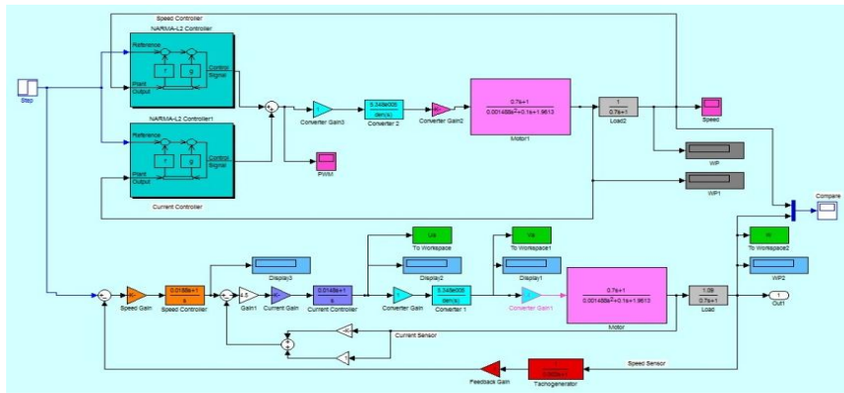

Fig. (11)**:** Simulink Plant Model for compare between Conventional PI Controller and current, speed control strategy using ANN (NARMA_L2) like PI controller.

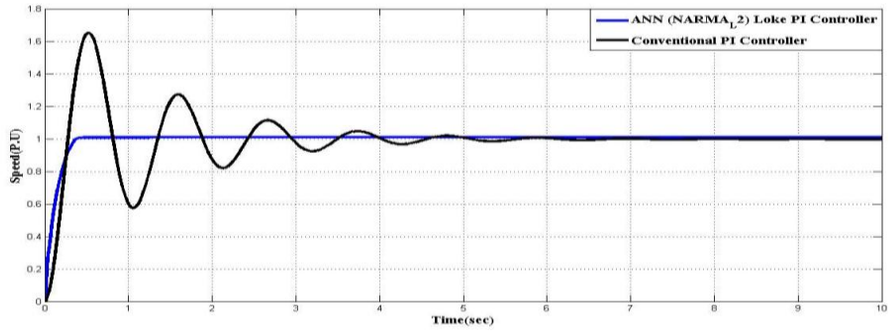

Fig. (12): compare results between conventional PI Controller and ANN (MRAC) like PI Controller.

The Neural network specifications are given in Table 2. The results shows that the response of the system is better than the conventional PI current controller. The settling time and steady state error is further reduced effectively.

Table (2): ANN (NARMA_L2) Plant Specification

ANN plant specification	
Number of inputs	3: are [$W_{ref}(t)$, $W_{ref}(t-1)$ and $W_{ref}(t-2)$]
Number of outputs	2: are [controlled output and Plant output]
Number of hidden layer	2
Number of training samples	500
Number of training epoches	150

The Plant input and output of ANN (NARMA_L2) as shown below in Fig. 13. The testing data for ANN (NARMA_L2) as shown below in Fig. 14.

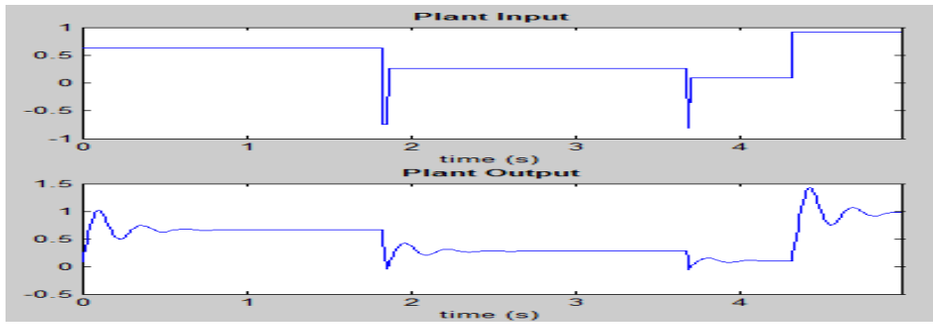

Fig (13): Plant input and output of ANN (NARMA_L2)

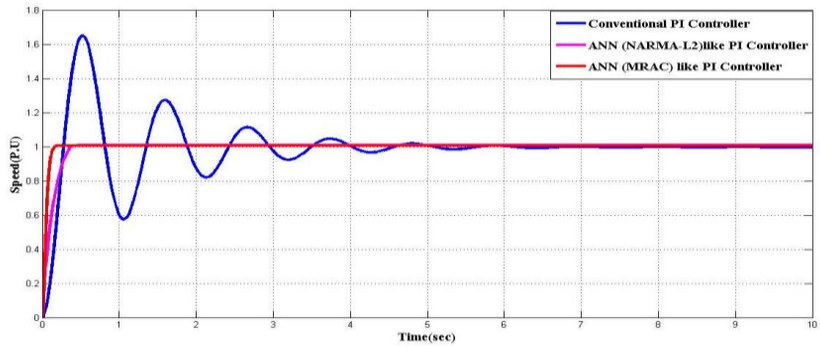

Fig (14): Testing data of ANN (NARMA_L2)

The Fig. 15. as shown below represent compare between Conventional PI Controller and Adaptive ANN like PI controller.

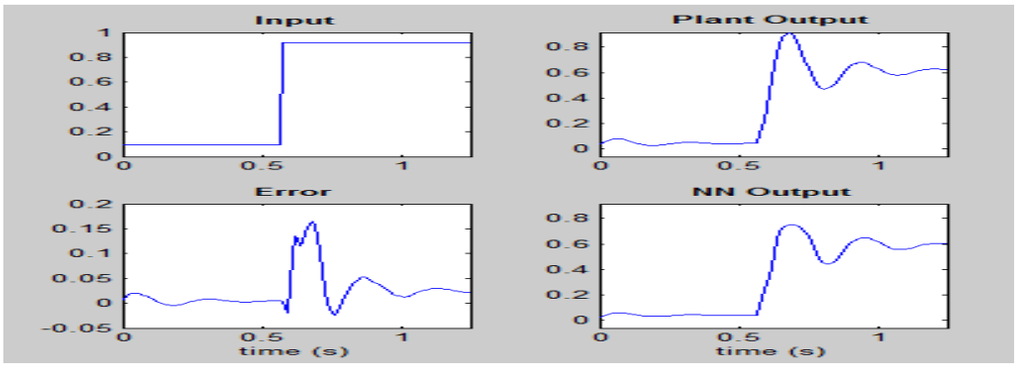

Fig. (15): Plant output speed for using ANN(MRAC and NARMA_L2) like PI controller and Conventional PI Controller for current and speed both.

5- Results And Discussion

In this work, the performance of a DC motor with a constant load using different control strategy, conventional (PI) and intelligent (ANN) controller is evaluated on the basis of settling time, maximum overshoot and steady state error. this results has been explained on table 3 as shown below.

Table (3): Results for the speed control of DC Motor

Speed response			
Cases	Settling time (ts) (second)	Maximum overshoot (p.u)	Steady state error (p.u)
Conventional PI controller using both current and speed control strategy	5.2	0.6	0.04
ANN approach for both current and speed control strategy by using ANN (NARMA_L2)	0.4	No overshoot	0.03
ANN approach for both current and speed control strategy by using ANN (MRAC)	0.2	No overshoot	0.02

6- Conclusion

Using ANN mode controller for the separately excited DC motor speed control, the following advantages have been realized. The speed response for constant load torque shows the ability of the drive to instantaneously reject the perturbation. The design of controller is highly simplified by using a cascade structure for independent control of flux and torque.

Excellent results added to the simplicity of the drive system, makes the ANN based control strategy suitable for a vast number of industrial, paper mills etc. The sharpness of the speed output with minimum overshoot defines the precision of the proposed drive. Settling time has been reduced to a label of 0.2 sec.

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Appendix (A)

Motor Ration	
Power	1.3kW
V_a	220V
I_a	7.3A
V_f	220V
I_f	0.4A
N	1500rpm

Motor Constant	
Element	Value
R_a	2.5 Ω
L_a	37.2 mH
R_f	485Ω
L_f	8.2H

اقتراح مسوق متسامح العطب للمحرك الحثي ثلاثي الطور

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المستخلص

ان التطبيقات الحديثة للمحركات الكهربائية تحتاج الى مسوقات كهربائية ذات وثوقيه عالية يعول عليها في امكانية استمرار عمل المحرك بكفاءة عالية حتى في حالات حدوث بعض انواع الاعطاب سواء في دائرة المسوق او المحرك . وتزداد الحاجة الى مثل هذه المسوقات خاصة في التطبيقات الحرجة التي لا تتحمل توقف المحرك حتى في حالة العطب مثل السيارات الكهربائية والطائرات ومضخات الوقود وغيرها من التطبيقات الحرجة في المعامل والمصانع.

يقدم هذا البحث تحليلاً وتمثيلاً لاستخدام ثلاثة مغيرات احادية الطور كمسوق متسامح مع اعطاب المحرك او المسوق. تم تحليل وتمثيل المغير عند ثلاثة اعطاب مختلفة وهي اعطاب قطع طور من اطوار المحرك (Single Phasing) وعطب حدوث دائرة قصر في احد مفاتيح المغير (Switch Short circuit) وعطب فتح في احد مفاتيح المسوق (Switch open circuit) ومن ثم تم عرض النتائج العملية لتشغيل المحرك الحثي ثلاثي الطور اثناء وقوع العطب. حيث تمت دراسة وتحليل اداء وتصرف المحرك الحثي عند وقوع الاعطاب اعلاه من خلال مراقبة تأثير كل عطب على تيارات وفولتيات المحرك وعزمه المتولد وكذلك على سرعة دورانه. ويقدم البحث الطوبوغرافيات الجديدة لربط المسوق مع المحرك الحثي بعد وقوع العطب والمقارنة في ثلاثة استراتيجيات مختلفة لقدح وسوق الطورين السليمين بعد خروج الطور الثالث بسبب وقوع العطب. حيث تمت محاكاة المنظومة عند استراتيجيات قدح وزوايا ازاحة طورية مقدارها (° 60، ° 90، ° 120) بين الطورين السليمين.

Proposed Fault Tolerant Drive for Three Phase Induction Motor

Dr. Yasir M. Younis **Omar M. Atiea**

Abstract

Induction motor are the most widely used electrical machines and the most popular in the industrial application, aerospace, and electrical vehicles. This celebrity of these machines because of some of their benefits such as: relatively low manufacturing cost, robust construction, moderate power factor, ability to operate in hostile environments, good reliability, and ease of control especially in recent years. In fact induction motors are the critical component of many of these applications and they are used in the most in the most of these applications with their power electronics drives in order to control their speeds, torques, or control their starting conditions, However, these motors and their drives may encounter several faults due to operating conditions. In fact, these faults are either due to the motor itself or its due to its power electronic driver circuit.

This paper presents the proposed fault tolerant drive for three phase induction motor; to drive induction motor in normal operating condition and during some faults conditions. The drive circuit with the machine is simulated in computer and practically implemented. The system is studied under three different fault types. These faults are switch open circuit fault, single phasing fault, and leg open circuit fault. The motor currents, voltages, induced torque and rotation speed characteristics are analyzed during the above fault conditions. Through change angle between two healthy phases to (120°, 90°, 60°) respectively after fault, and comparison of induction motor performance from side induced torque, motor speed and induction motor current post fault, then chose the best strategy to implement it.

1- المقدمة

تستخدم المحركات الحثية ثلاثية الطور في التطبيقات الصناعية المختلفة بكثرة، وذلك لما لها من مواصفات وخصائص جيدة تمتاز بها عن غيرها من المحركات الكهربائية الاخرى [1]. إذ تمتاز هذه المحركات بكفاءتها الجيدة وقلة حاجتها الى إجراءات الصيانة الدورية، وتمتاز ايضا بنسبة قدرة الى الوزن عالية وعامل قدرة مقبول، وبوثوقيه عالية يمكن القول انها محركات يعول عليها في ظروف العمل المختلفة [2]. لذا فان اكثر من 90% من المحركات الكهربائية المستخدمة في التطبيقات الصناعية هي محركات حثية ثلاثية الطور [3]. وفي اغلب هذه التطبيقات تُستخدم دوائر الكترونيات القدرة كمسوقات لهذه المحركات في منظومات تحكم مغلقة، اما للتحكم في سرع دورانها او للتحكم في عمليات بدئها او غيرها من الاستخدامات [4]. وبالرغم من الوثوقية العالية لهذه المحركات الا انها تتعرض مع مسوقاتها الى اعطاب جمة في اثناء عملها ربما تتسبب في ايقافها واخراجها عن العمل، مما يؤدي الى خسائر مادية ومعنوية كبيرة ناجمة عن توقف الانتاج وضياع الوقت. بل ان بعض التطبيقات الحرجة مثل السيارات الكهربائية وغيرها لا تتحمل التوقف عن العمل عند حدوث العطب وذلك لتعلق الامر بحياة الانسان ورفاهيته [5]. ومن هنا فان العديد من التطبيقات الصناعية المهمة تتطلب بناء مسوقات يعول عليها تسمح باستمرار عمل المحرك حتى عند حدوث العطب سواء أكان العطب في المحرك نفسه او في دائرة مسوقه. ان مثل هذه المسوقات تسمى بالمسوقات متسامحة العطب (Fault Tolerant Drives).

2- المسوقات متسامحة العطب

سماحية العطب من المصطلحات الحديثة التي تطلق على منظومات التحكم والسيطرة التي لها القابلية على العمل في الظروف السليمة (قبل وقوع العطب) وبعد وقوع العطب من اجل استمرارية العمل لبعض المنظومات الحرجة التي لا تحتمل التوقف. يمكن تعريف المسوقات متسامحة العطب على انها تلك المسوقات التي لها القابلية على سوق المحرك في الظروف الطبيعية (قبل وقوع العطب) والظروف غير الطبيعية (بعد وقوع العطب)، وذلك من خلال إمكانياتها في كشف العطب وعزله وتغيير طوبوغرافية دائرة المسوق او (و) المحرك واختيار استراتيجيات السوق المناسبة لكل نوع من انواع العطب ومن ثم العودة بالمحرك الى ظروف التشغيل الطبيعية بعد اصلاح العطب.

ان المسوق التقليدي للمحرك الحثي ثلاثي الطور والاكثر استخداماً وشيوعاً هو باستخدام تقنية تضمين عرض النبضة (PWM)، وهذا المسوق يعمل على تشغيل المحرك في الظروف الطبيعية فقط وليس له القابلية على العمل في حالات العطب التي يتعرض لها المحرك الحثي ثلاثي الطور او المسوق نفسه.، حيث يتكون من ستة مفاتيح قدرة مربوطة مع مصدر تجهيز فولتية مستمرة، تُسلط عليها نبضات السوق المناسبة باستخدام إحدى استراتيجيات تقنية تضمين عرض النبضة ، وذلك من اجل الحصول على فولتية متناوبة ثلاثية الطور متغيرة القيمة و(او) التردد بُغية السيطرة اتجاهياً او مقدارياً على عمل المحرك الحثي ثلاثي الطور، وهو احد اشكال ما يسمى بمجهز مغير الفولتية (Voltage Source Inverter).

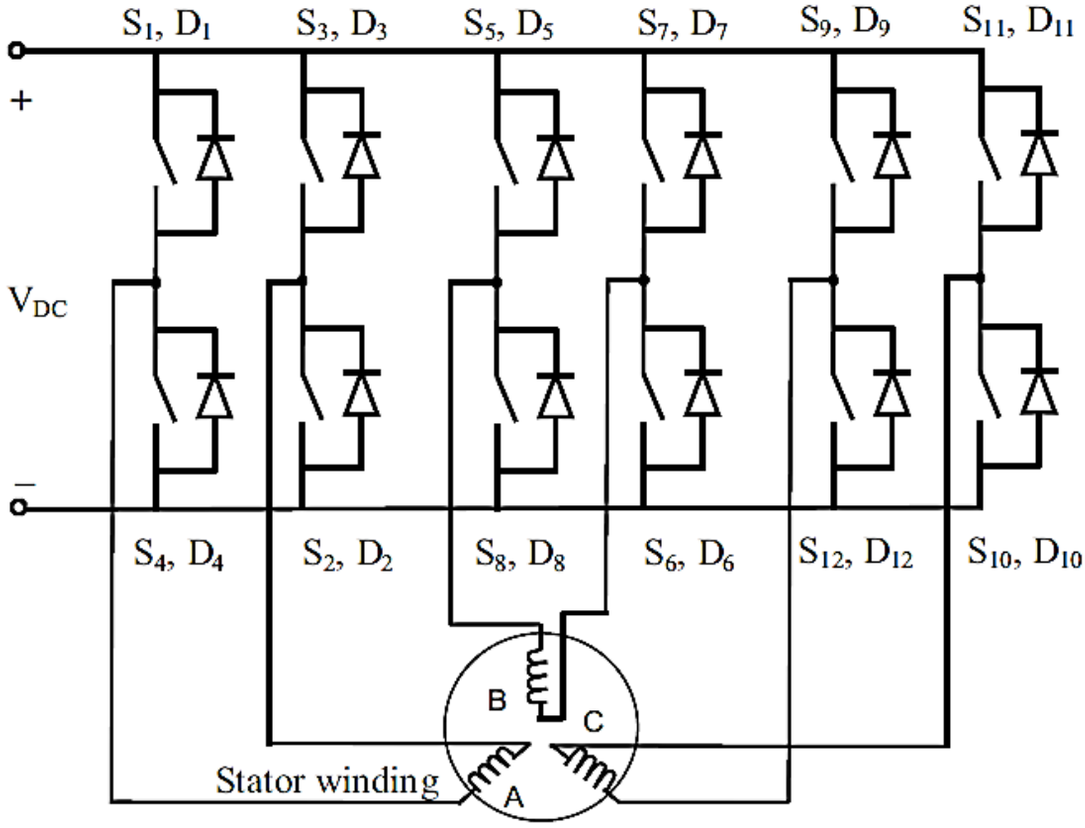
3- تمثيل مسوق محرك حثي ثلاثي الطور متسامح العطب

هناك عدة دوائر للمسوق متسامح العطب، ولكل منها طبيعة تختلف عن الاخرى. وتستخدم هذه الدوائر حسب المتطلبات التي يقتضيها التطبيق، ففي بعض التطبيقات تكون الأولوية للحصول على عزم ثابت، وفي البعض الاخر تكون الاولوية الحصول على مدى واسع من السرع، واما البعض الاخر فتكون الاولوية للحصول على كفاءة عمل عالية للمحرك. ومن جهة اخرى فان المحرك يجب ان يكون له القابلية على العمل في الظروف الغير اعتيادية بعد وقوع العطب. وفي بعض الاحيان يزداد التيار المسحوب من قبل المحرك او تزداد قيم التوافقيات المجهزة من قبل المسوق للمحرك نتيجة حدوث العطب والتي تعمل بدورها على زيادة الخسائر في المحرك، فترتفع الحرارة في اجزاء المحرك واذا ما كانت عوازل المحرك ليست لها القابلية على تحمل هذه الحرارة الزائدة فأن ذلك ربما سيؤدي الى انهيارها. العازل. وربما يؤدي التشغيل المستمر بهذه الظروف الى عطب ملفات المحرك بالكامل، لذا فيجب الاخذ بنظر الاعتبار مواصفات المحرك وقراءة لوحته التعريفية جيداً قبل اختيار الطوبوغرافية التي سيعمل عندها المسوق بعد حدوث العطب. فعلى سبيل المثال يعتمد تحمل الماكنة لأعظم حرارة على نوع وصنف عازل اسلاكها حيث من المعلوم ان هنالك اربعة اصناف قياسية لعوازل الاسلاك وهي اما ان يكون من الصنف A او B او F او H والتي تكون حدودها العليا للحرارة هي 60°C او 80° C او 105° C و 125° C على التوالي.

وعلى اية حال، يتطرق هذا البحث الى تمثيل وتحقيق مسوق متسامح العطب للمحرك الحثي ثلاثي الطور عند حالات تشغيل مختلفة للمحرك وخصائص كل من هذه الحالات في سماحية الاعطاب التالية:

1. عطب فتح في احد اطوار المحرك. Winding open circuit.
2. عطب فتح احد مفاتيح المسوق. Inverter Switch Open circuit.
3. عطب فتح احد سيقان المسوق. Leg Open circuit.

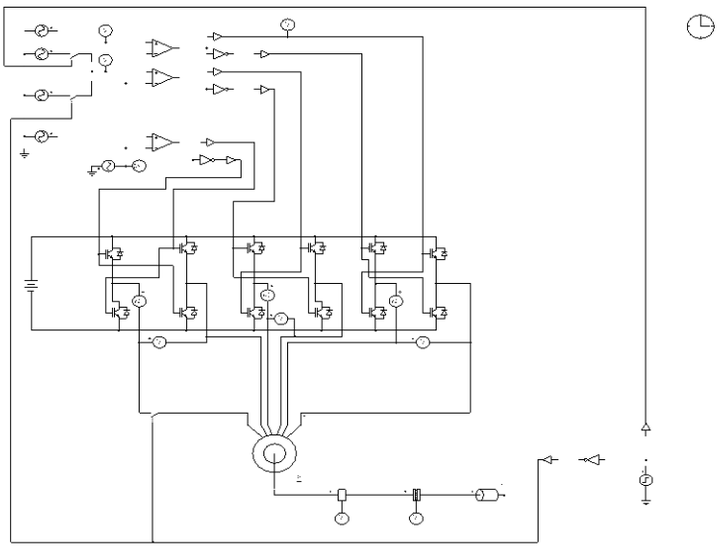
ان المسوق المقترح يعمل عمل ثلاثة مغيرات احادية الطور والموضحة في الشكل رقم (2) له القابلية على العمل قبل وبعد وقوع العطب بطوبوغرافيات مختلفة تتكيف مع الاعطاب التي تقع في المسوق نفسه او الاعطاب التي تقع في الجزء الساكن للمحرك. حيث يمكن له العمل عند طوبوغرافيات واستراتيجيات مختلفة ويكون عمله على النحو الاتي:



الشكل رقم (2) : مسوق محرك حثي ثلاثي الطور ذو المغيرات الثلاثة

تجهز كل ملف من ملفات المحرك في هذه الطوبوغرافية من طريق مغير قنطري احادي الطور باستخدام اربعة مفاتيح. حيث يقوم المغير الاول بتجهيز فولتية احادية الطور الى الملف الاول (a) بزاوية ازاحة طوريه تساوي صفر (θ_a=0°) في حين يقوم المغيرين الثاني والثالث بتجهيز الفولتية نفسها ولكن بزاوية ازاحة طوريه مقدارها (θ_b =120°,θ_c =240°) على التوالي. عندئذ يعمل المحرك وكانه مجهز من ثلاث مصادر احادية الطور منفصلة، ان هذا التشغيل له مساوئ حيث تظهر التوافقية الثالثة ومضاعفاتها مما يزيد من خسائر المحرك ويقلل من العزم المتولد. عند حدوث عطب في احد ملفات المحرك او في احد مفاتيح المغير يقوم المسوق بعزل الطور الذي وقع فيه العطب وتغيير طوبوغرافية الدائرة واستراتيجية القدح للطورين السليمين وذلك للمحافظة على السرعة والعزم دون الزيادة المفرطة في تيار الخط. وعلى فرض ان عطبٌ ما وقع في الطور (C) فيتم عزل الطور المعطوب بإحدى طرق العزل كما مبينة في الشكل رقم (3) ومن ثم يتم تغيير زاوية الفولتية بين الطورين السليمين وتشغيل المحرك كمحرك حثي ثنائي الطور. ان هذه الطوبوغرافية تسهل من عملية عزل العطب كون كل من ملفات المحرك يجهز بصورة منفصلة عن الملفات الاخرى

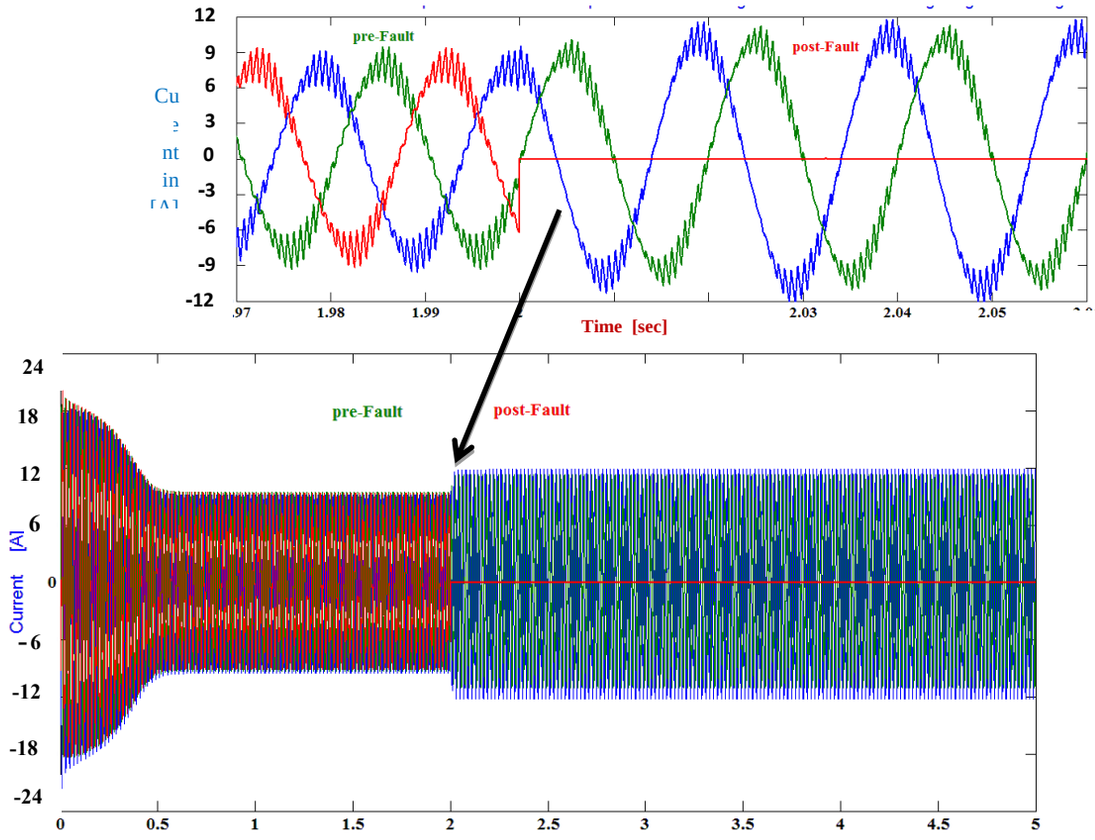
بالإضافة الى انه تم التخلص من استخدام المقسم السعوي وعدم ظهور مركبة التتابع الصفري بعد وقوع العطب. من مساوئ هذا المسوق ان اداء المحرك الحثي بعد العطب يقل، بسبب حدوث تذبذب في السرعة والعزم وحصول زيادة في خسائر المحرك نتيجة عدم التوازن في مصدر التجهيز. وفي الفقرة القادمة سيتم فحص اداء المحرك ودراسة سلوكه من خلال محاكاة المنظومة عند زاويا مختلفة للإزاحة الطورية بين الطورين السليمين وهما (°120 و °90 و°60) وذلك باستخدام برنامج محاكاة الدوائر والمنظومات الكهربائية (Psim). إذ تم استخدام هذا البرنامج لما له من امكانية عالية ومرونة في محاكاة وتمثيل منظومة مسوقات المحركات الكهربائية بأنواعها المختلفة. ويوضح الشكل رقم (3) التمثيل الكهربائي للمسوق المقترح مع المحرك الحثي ثلاثي الطور. وفيما يلي تفصيلاً لأداء المحرك عند هذه الزاويا.



شكل رقم (3) : تمثيل المسوق المقترح مع المحرك الحثي ثلاثي الطور

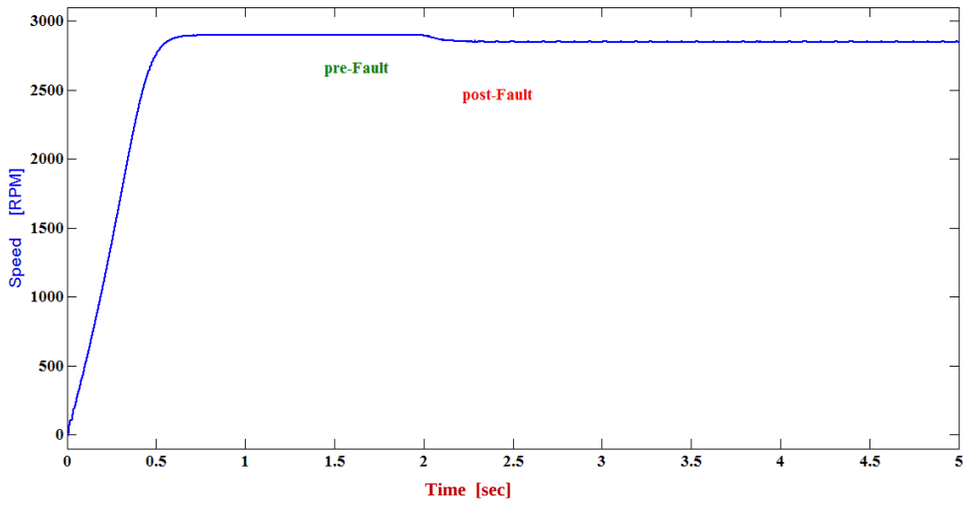
a. <u>الاستراتيجية الاولى: زاوية ازاحة طوريه °120</u>

عند جعل الزاوية بين فولتية الطورين السليمين بمقدار ° 120 تمت ملاحظة تيارات المحرك وسرعته وعزمه قبل وبعد وقوع العطب. حيث يوضح الشكل رقم (4) ان الزاوية بين التيارين في الطورين السليمين هي الزاوية نفسها بين الفولتيتين بعد وقوع العطب أي بمقدار ° 120 وليس بمقدار ° 180، وذلك لان كل ملف منفصل عن الاخر ويزداد التيار بعد وقوع العطب بقيمة اكبر من قيمته قبل وقوع العطب. حيث زادت هذه القيمة بنسبة 1.2 من قيمته قبل العطب.

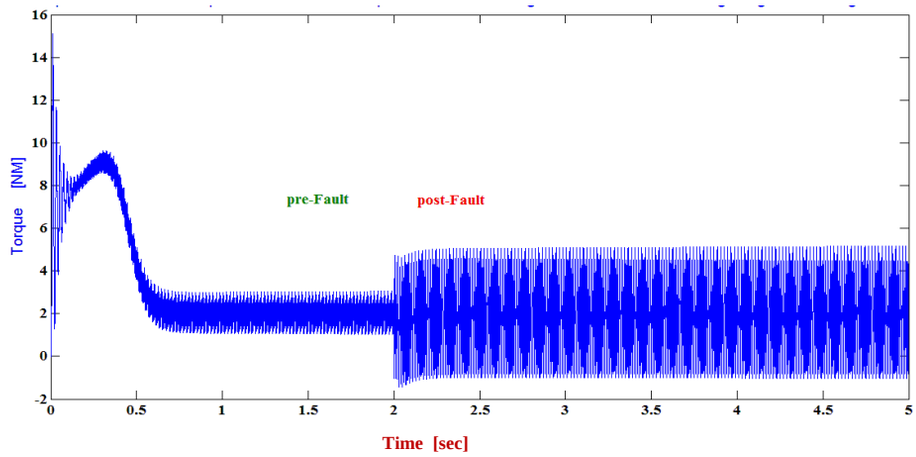


شكل رقم (4) : تيارات الاطوار قبل وبعد وقوع العطب عند الحفاظ على زاوية الازاحة الطورية بين فولتيتي الطورين السليمين 120° بعد العطب

اما الشكل رقم (5) فيبين سرعة قبل وبعد وقوع العطب حيث يُلاحظ ثبوت قيمة السرعة وخلوها من التموج قبل وقوع العطب، اما بعد العطب فتمر بحالة عابرة ثم تعود لتستقر عند قيمة اقل من السابقة مع حصول تموج وتذبذب قليل فيها يتسببان في زيادة اهتزاز الماكنة. وهكذا تحدث مع منحني العزم مع الزمن عند الظروف نفسها، وكما هو موضح في الشكل رقم (6).



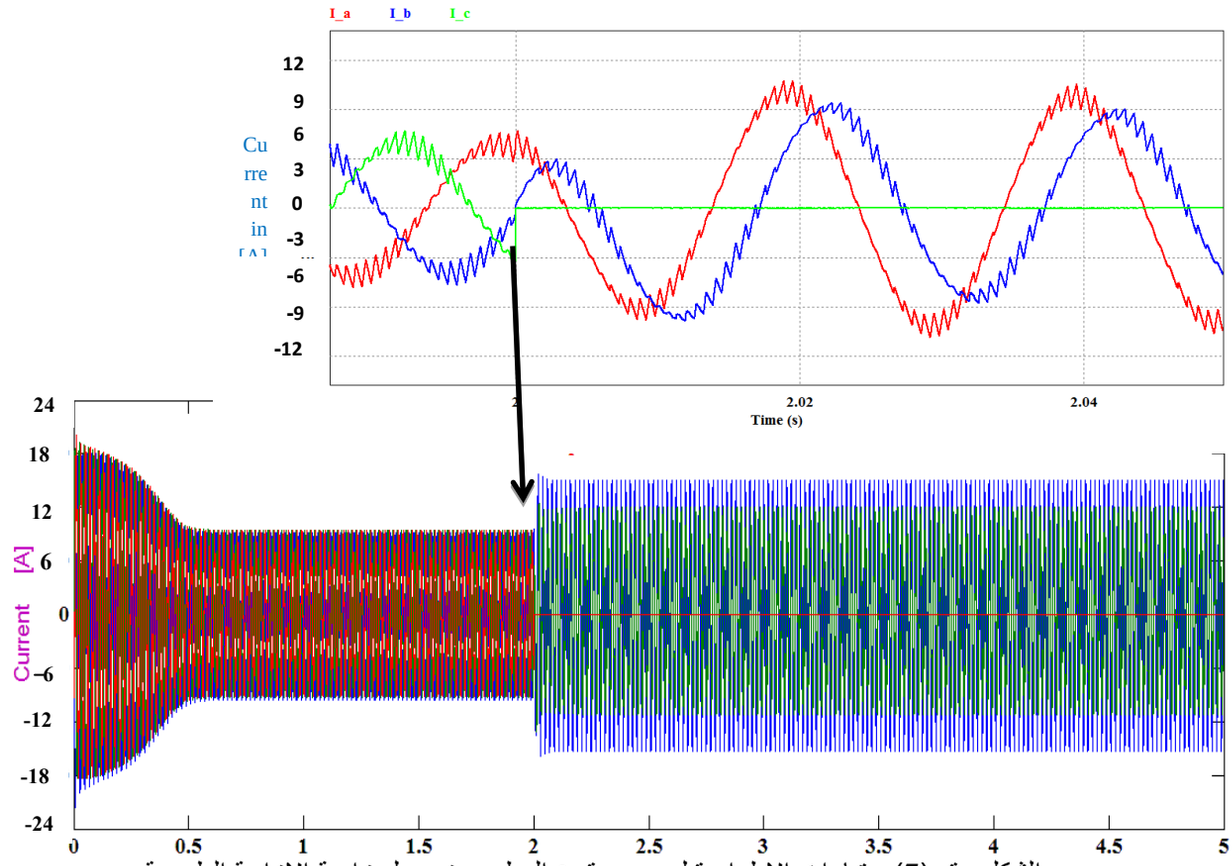
الشكل رقم (5) منحني السرعة قبل وبعد وقوع العطب عند الحفاظ على زاوية الازاحة الطورية بين فولتيتي الطورين السليمين 120° بعد العطب



الشكل رقم (6) : العزم قبل وبعد وقوع العطب عند الحفاظ على زاوية الازاحة الطورية بين فولتيتي الطورين السليمين 120^{o} بعد العطب

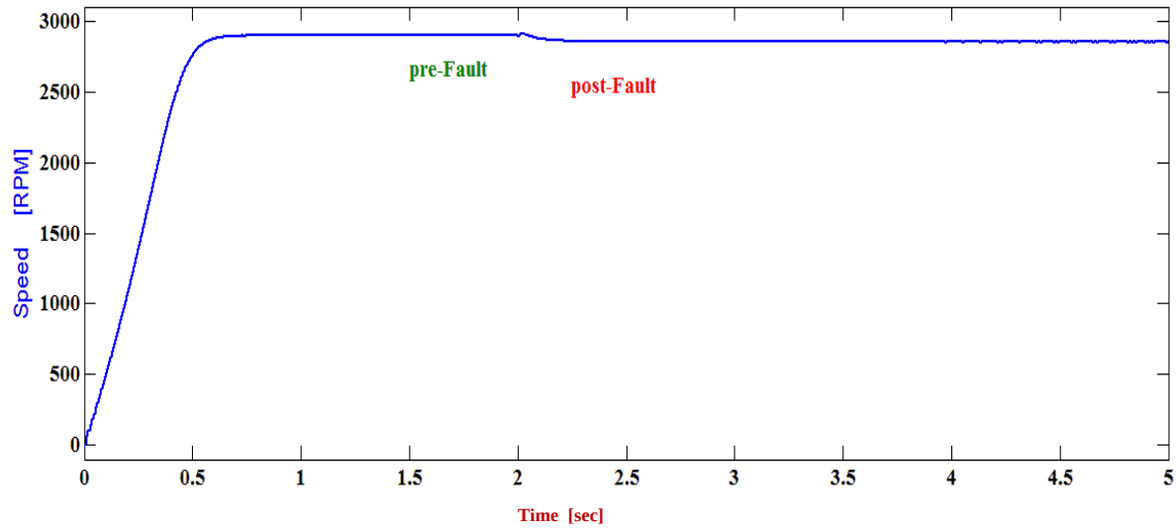
b. الاستراتيجية الثانية: زاوية ازاحة طوريه 90°

تم جعل زاوية الازاحة الطورية بين فولتيي الطورين السليمين بمقدار 90° بعد وقوع العطب وتمت ملاحظة تيارات المحرك وسرعته وعزمه قبل وبعد وقوع العطب. ويوضح الشكل رقم (7) ان الزاوية بين التيارين في الطورين السليمين تكون 90° بعد وقوع العطب. في حين ان قيمة التيار تزداد بنسبة 1.5 من قيمته قبل وقوع العطب. ويُلاحظ ان السرعة قيمتها ثابتة وخالية من التموج قبل وقوع العطب اما بعد العطب فتمر بحالة عابرة ثم تعود لتستقر عند نفس القيمة تقريبا ولكن مع تموج قليل كما مبينة في الشكل رقم (8) حيث يوضح منحني السرعة مع الزمن قبل وبعد وقوع العطب. اما شكل منحني العزم والمبين في الشكل رقم (9) فانه يحتوي على تموج قليل بالمقارنة مع الحالة السابقة.

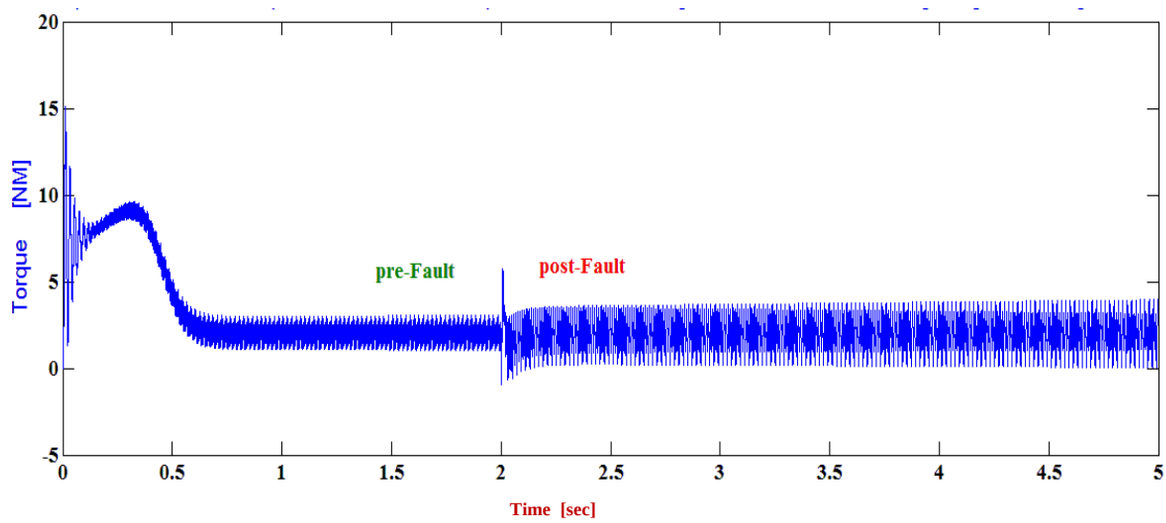


الشكل رقم (7) : تيارات الاطوار قبل وبعد وقوع العطب عند جعل زاوية الازاحة الطورية بين فولتيتي الطورين السليمين 90^{o} بعد العطب

يُلاحظ ان الزيادة الحاصلة في قيم التيارات في هذه الاستراتيجية هي اكبر من استراتيجية التشغيل الاولى (°120) اذن الاستراتيجية الثانية هي افضل من الاستراتيجية الاولى من ناحية التيارات. بينما منحني العزم يكون التذبذب به قليل والسرعة تحافظ على قيمتها تقريباً بعد وقوع العطب في وهي افضل من الاستراتيجية الاولى من ناحية اداء المحرك.



الشكل رقم (8) : السرعة قبل وبعد وقوع العطب عند جعل زاوية الازاحة الطورية بين فولتيتي الطورين السليمين 90^{o} بعد العطب



الشكل رقم (9) : العزم قبل وبعد وقوع العطب عند جعل زاوية الازاحة الطورية بين فولتيتي الطورين السليمين 90^{o} بعد العطب

c. <u>الاستراتيجية الثالثة: زاوية ازاحة طوريه 60^{o}</u>

في هذه الاستراتيجية تم جعل الزاوية بين الطورين السليمين (°60) بعد وقوع العطب وكانت النتائج كما موضحة ادناه. حيث يوضح الشكل رقم (10) شكل موجة التيار للمحرك قبل وبعد وقوع العطب، حيث يلاحظ ان قيمة التيارات بعد وقوع العطب تزداد بنسبة 1.833 من قيمته قبل وقوع العطب. بينما يوضح الشكل رقم (11) منحني السرعة، حيث يلاحظ ان السرعة قيمتها ثابتة قبل العطب، اما بعده تمر بحالة عابرة ثم تعود لتستقر عند قيمة اقل من قيمتها قبل وقوع العطب. اما الشكل رقم (12) فيبين منحني العزم المتولد في المحرك مع الزمن قبل وبعد

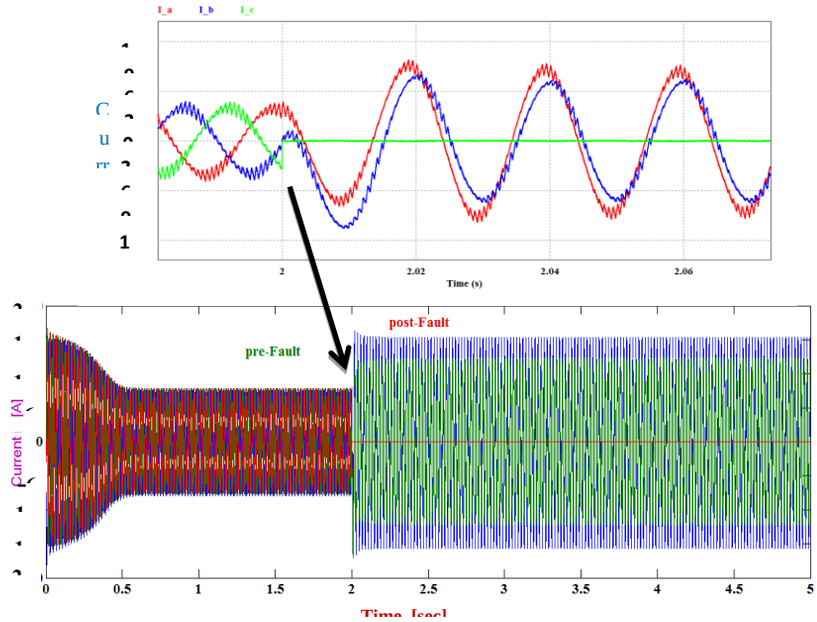
وقوع لعطب، حيث يلاحظ ان قيمة العزم المتولد قبل وقوع العطب ثابتة مع تموج قليل اما بعد وقوع فيحصل تذبذب عالي في العزم وهذا التموج يسبب اهتزاز جسم الماكنة بعد وقوع العطب.

ان الزيادة في قيمة التيارات بعد وقوع العطب في هذه الاستراتيجية اكثر من الاستراتيجيتين الاولى والثانية بينما العزم يتذبذب بنفس الاستراتيجية الاولى تقريباً.

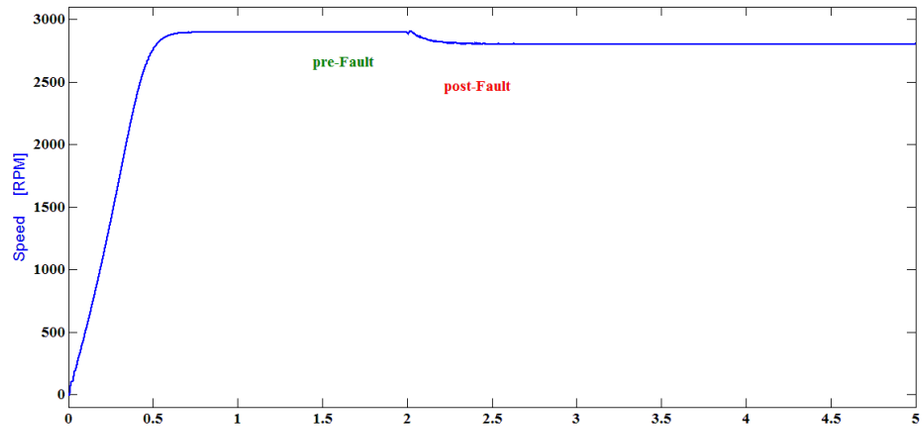
يمكن مقارنة اداء المحرك الحثي ثلاثي الطور بعد وقوع العطب عند اشتغاله بالاستراتيجيات المذكورة اعلاه مقارنة مع التشغيل الطبيعي للمحرك قبل وقوع العطب كما هي موضحة في الجدول رقم (1)

الجدول رقم (1) : مقارنة اداء المحرك من حيث السرعة والعزم وتيارات الاطوار عند تشغيله بزوايا مختلفة بعد وقوع العطب

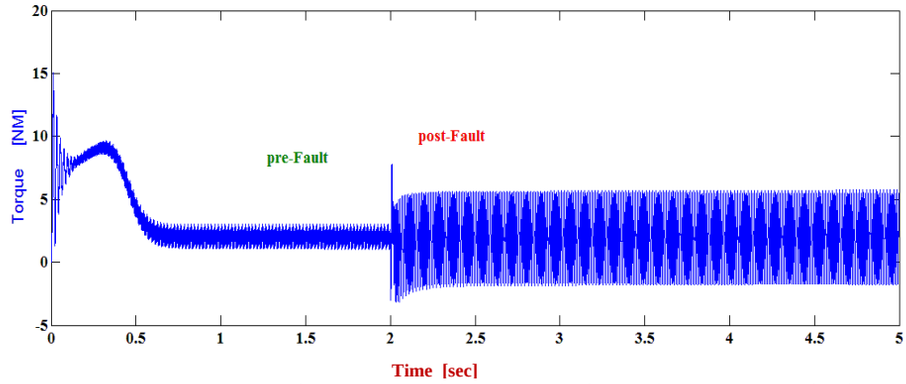
استراتيجية التشغيل المستخدمة	الزيادة في تيارات الاطوار %	نسبة تذبذب العزم p-p	السرعة pu
التشغيل الطبيعي	0	2	1
زاوية مقدارها 60°	83.3	3.1	0.9
زاوية مقدارها 90°	50	2.5	0.97
زاوية مقدارها 120°	26	3	0.92



الشكل رقم (10) : تيارات الاطوار قبل وبعد وقوع العطب عند جعل زاوية الازاحة الطورية بين فولتيتي الطورين السليمين 60^{o} بعد العطب



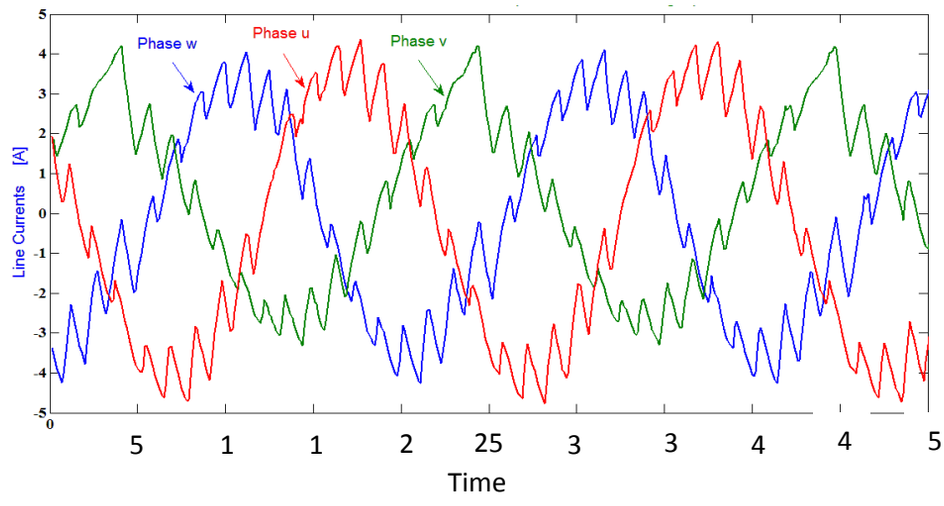
الشكل رقم (11) السرعة قبل وبعد وقوع العطب عند جعل زاوية الازاحة الطورية بين فولتيتي الطورين السليمين ° 60 بعد العطب



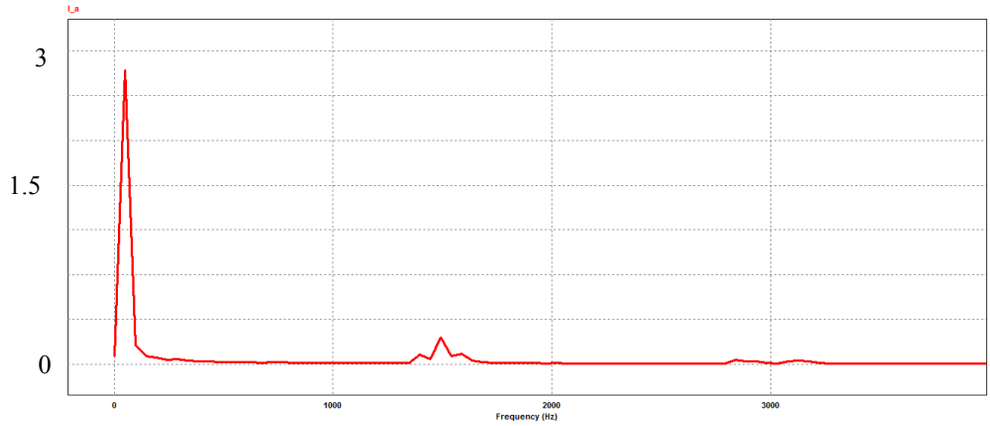
الشكل رقم (12) : العزم قبل وبعد وقوع العطب عند جعل زاوية الازاحة الطورية بين فولتيتي الطورين السليمين 60^{o} بعد العطب

4- النتائج العملية

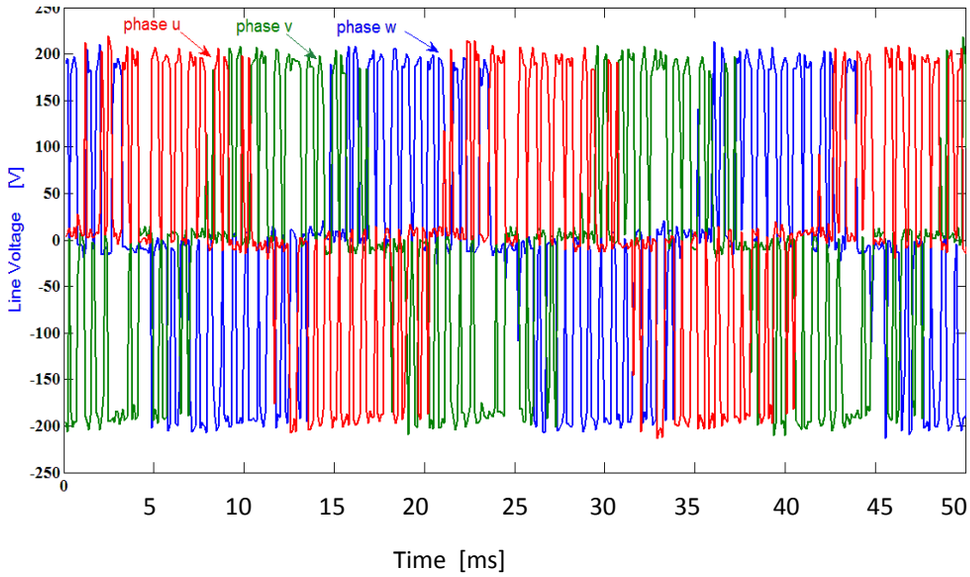
تم تحقيق مسوق المحرك الحثي ثلاثي الطور متسامح العطب عمليا في المختبر باستخدام ثلاث مغيرات احادية الطور، عند استراتيجية المحافظة على زاوية فرق الطور بين فولتيتي الطورين السليمين 120° ؛ لان هذه الاستراتيجية هي الانسب من ناحية التيارات المسحوبة من المصدر فضلاً عن الحصول على استجابة عزم وسرعة مقبولين. وتمت ملاحظة الفولتيات المسلطة على المحرك الحثي ثلاثي الطور والتيارات المسحوبة من المصدر وتم عرض منحني الفولتية والتيار على نفس الرسم وتليلهما لملاحظة التوافقيات الموجودة فيهما قبل وقوع العطب وبعده، فضلاً عن قياس العزم المتولد قبل وقوع العطب وبعده. إذ يوضح الشكل رقم (13) تيارات الاطوار قبل وقوع العطب اما الشكل رقم (14) يبين تحليل موجة التيار إذ يلاحظ التوافقيات الموجودة في موجة التيار قليلة جدا نتيجة لاستخدام تقنية عرض النبضة الجيبي بالإضافة الى مرور هذا التيار في ملفات المحرك حيث ان هذه الملفات عملت كمرشح للموجة، بينما وضح الشكل رقم (15) شكل الفولتية ثلاثية الطور الخارجة من المسوق في حال التشغيل الطبيعي للمحرك والشكل رقم (16) اظهر تحليل التوافقيات الموجودة في موجة الفولتية. بينما وضح الشكل رقم (17) موجة الفولتية والتيار على نفس الرسم لملاحظة زاوية فرق الطور بينهما.



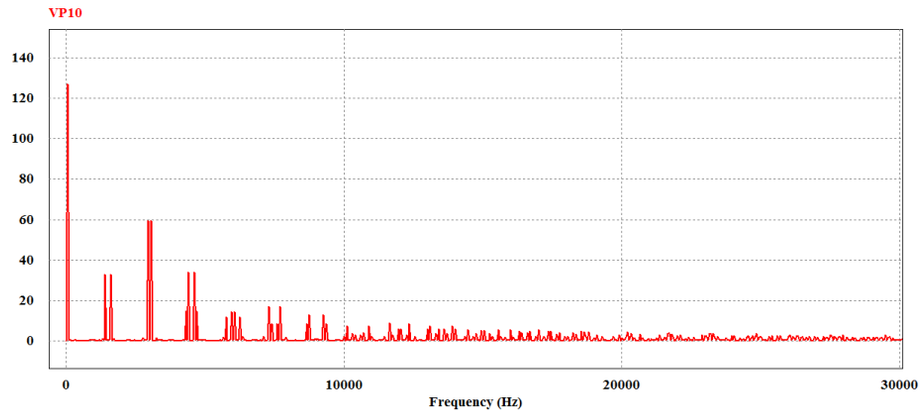
الشكل رقم (13) : شكل موجة التيار ثلاثية الطور العملية عند تشغيل المحرك من ثلاث مغيرات احادية الطور



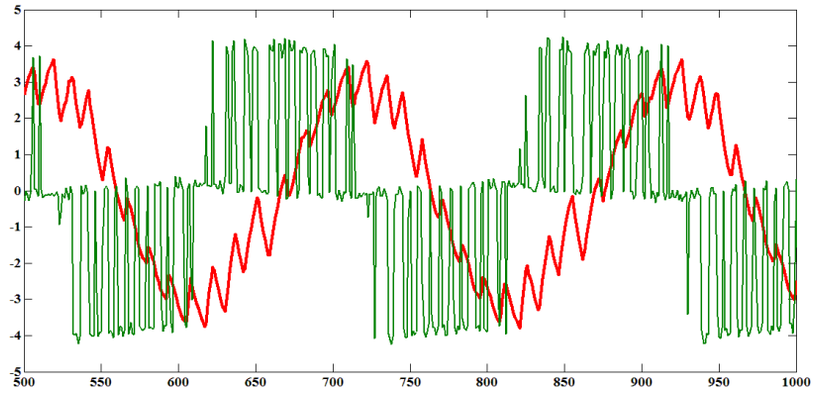
الشكل رقم (14) : تحليل التوافقيات في موجة تيار الخط



الشكل رقم (15) : شكل موجة الفولتية ثلاثية الطور عند تشغيل المحرك من المسوق المقترح

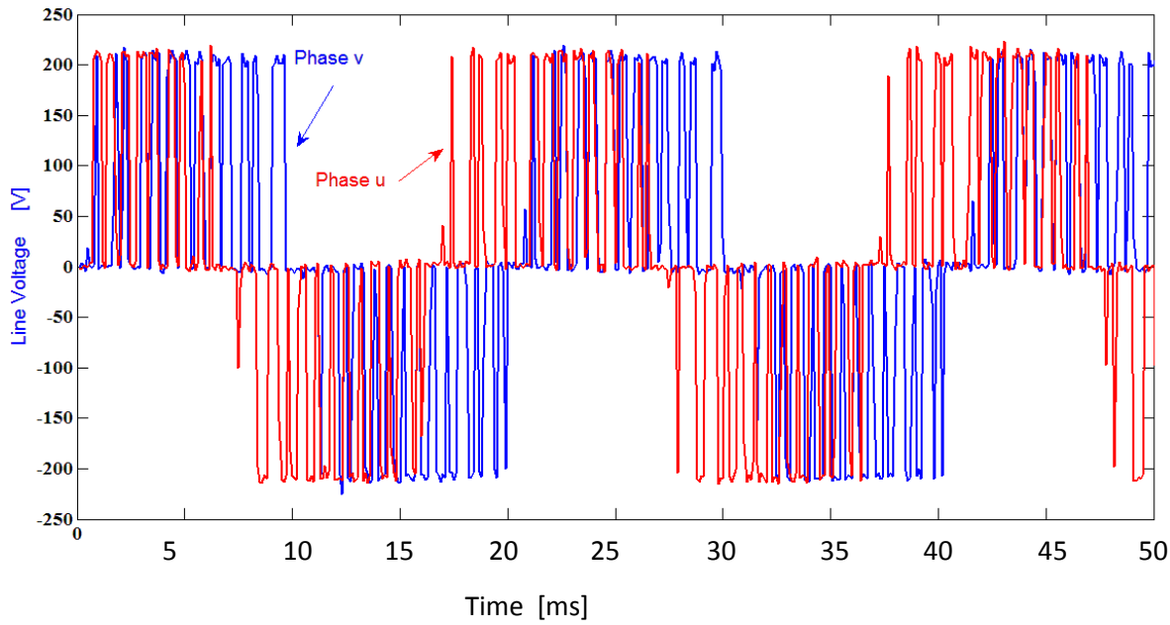


الشكل رقم (16) : تحليل التوافقيات في موجة الفولتية



الشكل رقم (17) : شكل موجة الفولتية والتيار

اما بعد وقوع عطب ما في المحرك الحثي ثلاثي الطور يتم اطفاء المغير الذي يجهز الملف الذي وقع في العطب وتشغيل المحرك الحثي ثلاثي الطور كمحرك حثي ثنائي الطور حيث يوضح الشكل رقم (15) شكل موجة الفولتية المُجهزة الى المحرك عند تشغيل المحرك كمحرك حثي ثنائي الطور. بينما يوضح الشكل رقم (16) شكل موجة التيار بعد وقوع العطب فتكون الزيادة في قيمة التيار بنسبة 26% من قيمته قبل العطب. اما الشكل رقم (17) فيوضح منحني العزم قبل وقوع العطب وبعده حيث يُلاحظ ان العزم يحتوي على تذبذب قبل وقوع العطب اما بعد وقوع العطب يحافظ على قيمته ولكن يزداد التذبذب قليلاً.



الشكل رقم (18) : شكل موجة الفولتية ثنائية الطور عند تشغيل المحرك الحثي
من ثلاث مغيرات احادية الطور اثناء وقوع العطب

5- الاستنتاج

نستنتج من هذا البحث ان قيمة التيارات تزداد بعد وقوع العطب في الاستراتيجيات اعلاه كلها ولكن هذه الزيادة غير متساوية، حيثُ كانت نسبة الزيادة 26% في الاستراتيجية الاولى بينما اصبح العزم اقل وحصلَ تذبذب عالي فيه مما يسبب زيادة اهتزاز الماكنة. اما في الاستراتيجية الثانية فان التيار ازداد بنسبة 50% من قيمته قبل العطب بينما العزم حافظ على قيمته تقريباً مع زيادة قليلة في التذبذب ونقصان قليل في السرعة. وفي الاستراتيجية الثالثة كانت الزيادة في نسبة التيار 83.3% من قيمته قبل وقوع العطب بينما العزم المتولد حافظ على قيمته تقريباً ولكن ازداد التذبذب بصورة عالية وحَصل نقصان قليل في قيمة السرعة.

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المحتويات

Implementation of FFT/IFFT Processor On A Reconfigurable Platform

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Abstract

The FFT/IFFT is one of the most widely used digital signal processing algorithm. Contemporary attention has come back to real-time FFT/IFFT processors in many applications. In this paper, a fixed point hardware model of an FFT/IFFT processor is designed and then implemented on a reconfigurable platform. Two approaches are used to model the architecture of the proposed processor. First approach uses the FFT Xilinx logic core generator with its four architectures including: Pipelined-Streaming I/O, Radix-4-Burst I/O, Radix-2-Burst I/O, and Radix-2 Lite-Burst I/O. The second approach is based on manually writing VHDL codes. The twiddle factors for Radix-4 FFT engine in this approach is generated according to the CORDIC algorithm. All the above architectures are implemented and synthesized on Spartan-3E FPGA of 500,000 gates. Finally, a comparison study in respect to hardware recourses(chip utilization), and speed(throughput) is achieved between the CORDIC based processor and the four FFT Xilinx Logic core based processors.

Keywords: Fast Fourier Transform, FPGA, Radix-2, Radix-4, reconfigurable FFT/IFFT processor, system generator, Xilinx Logiccore FFT.

تنفيذ تحويل فورييه السريع ومعكوسه على شريحة قابلة لإعادة التشكيل

د.شفاء عبد الرحمن داوود **سهى مظفر نوري**

الخلاصة

يعتبر معالج تحويل فورييه السريع ومعكوسه احد خوارزميات معالجة الإشارات الرقمية الأكثر استخداما. حيث انه مؤخرا زاد الاهتمام بمعالجات فورييه السريع ومعكوسه في الكثير من تطبيقات الزمن الحقيقي. في هذا البحث تم تصميم نموذج نقطة ثابتة مادي لمعالج تحويل فورييه ومعكوسة ومن ثم تنفيذه على منصة قابلة لإعادة التهيئة. تم استخدام طريقتين في بناء نموذج معمارية المعالج المقترح. تستخدم الطريقة الأولى مولد القطب المنطقي لتحويل فورييه السريع الخاص بشركة Xilinx يدويا في الطريقة الثانية. يتم توليد معاملات التحويل في VHDLبمعمارياته الأربع. بينما يتم استخدام كتابة شفرة هذه الطريقة اعتمادا على خوارزمية كورديك. تم تنفيذ وتركيب المعماريات أعلاه على مصفوفة البوابات القابلة للبرمجة حقليا من نوع Spartan-3E المكونة من 500,000 بوابة. أخيرا تم مقارنة مواصفات معالج فورييه السريع ومعكوسه والمصمم اعتمادا على خوارزمية كورديك مع المعالجات الأربعة المصممة اعتمادا على مولد القطب المنطقي.

1. Introduction

The Discrete Fourier Transform (DFT) plays a significantly important role in many applications of digital signal processing. Basically, it has been applied in a wide range of fields such as linear filtering[1], spectrum analysis[2], digital video broadcasting[3] and Orthogonal Frequency Demodulation Multiplexing (OFDM)[4]. The DFT is also used to competently solve partial differential equations, and to proceed other operations such as convolutions[5].There are several ways to deem the Discrete Fourier Transform (DFT),such as resolving simultaneous linear equations or the correlation method. The Fast Fourier Transform (FFT) is another method for calculating the DFT .It may be noted that the numeral of complex multiply and add operations needed by the modest forms both the DFT and IDFT is of order N^2 . This is because there are N data points to calculate, each of which demands N complex arithmetic operations, while an FFT can compute the same DFT in only O(N log N) operations. The difference in speed can be enormous, especially for long data sets where N may be in the thousands or millions. If we (naively) assume that algorithmic complexity fits a direct measure of execution time (and that the relevant logarithm base is 2) then the ratio of execution times for the (DFT) vs. (FFT) can be expressed:

$$\frac{N^{\cdot}}{Nlog_2N} = \frac{N}{log_2N} = \frac{2^{\mathfrak{p}}}{p} \qquad (1)$$

For a 1024 point transform (p=10, N=1024), this gives approximately 100 fold speed improvement[6]

Because of these high-speed of Fast Fourier Transform, The FFT/IFFT is one of the most widely used in digital signal processing algorithms. Recently attention has been returned to real-time FFT/IFFT processors in many applications.

One of real time application is (FFT convolution) where FFT convolution uses the principle that *multiplication* in the frequency domain corresponds to convolution in the time domain. The input signal is transformed into the frequency domain using the DFT, multiplied by the frequency response of the filter, and then transformed back into the time domain. Using the inverse DFT convolution via the frequency domain can be *faster* than directly convolving the time domain signals. The final result is the same; only the number of calculations has been changed by a more efficient algorithm. For this reason, FFT convolution is also called high-speed convolution

In OFDM based systems, the FFT/IFFT processor is a key component. The FFT/IFFT is widely used in many digital signal and image processing applications such as sound or medical image, and the efficient implementation of the FFT/IFFT is a topic of continuous research[7].

There is a growing number of recently reported works on FFT/IFFT algorithms and their implementation. In 2006C. Lin, et al have implemented64-Point FFT/IFFT using radix-8 [8], in 2009 A. Said, et al have implementedradix-2^2 single-path delay feedback pipelined FFT/IFFT processor for transformation length 256-point[9]. and in 2012 Joseph, E., et alhaveutilized radix-4 CORDIC to generate the twiddle factor for radix-2 FFT processor[10].In this paper a Fixed-Point FFT/IFFT processor is implemented in FPGA which are based on both a manually written VHDL codes and automatic tools of Xilinx System Generator.

The rest of the paper is organized in the following order: in section 2, the theory of FFT algorithms are briefly introduced. In section 3, different modeling and architectures of FFT

are presented. The result and discussion are presented in section 4. Finally conclusion are given in section 5.

2. Theory Of The Fast Fourier Transform(Fft)

The basic relationship of the discrete Fourier Transform (DFT)[11]:

$$X(k) = \sum_{n=0}^{N-1} x[n] W_N^{nk} \qquad 0 \le k \le N-1 \tag{2}$$

Where X(k) is the k^{th} harmonic, x[n] is the n^{th} input sample (n=0..N-1), and W_N is shorthand for $\exp(-i2\pi/N)$.To make the DFT operation more practical, there are different types of FFT algorithms for different DFT lengths and the most common fast Fourier transform (FFT) algorithm is Cooley–Tukey FFT algorithm. There are basically two types of algorithm to achieve Cooley–Tukey FFT algorithm:

1. DIT(Decimation In Time)FFT algorithm: it is based on decomposition of the N point DFT computation by dividing input sequence and this process continued until two point DFT is obtained.**2. DIF(Decimation In Frequency)FFT algorithm:** it is based on decomposition of the N point DFT computation by dividing output sequence and this process continued until two point DFT is obtained. The most significant difference between DIF and DIT algorithms is that in DIT the input is bit reversed and output is in natural order. In DIF the input is in natural order and output is bit-reversed order. So if both forward and inverse transforms are required and bit reversed addressing isn't available, then DIF is used for the forward transform(FFT) and DIT for the inverse transform(IFFT is fast computation algorithm of IDFT(inverse DFT)).

IFFT can be obtained from FFT for the proposed processor by conjugate the twiddle factors because the only important difference between FFT and IFFT is the sign of the twiddle factor

In this paper DIT algorithm is introduced for radix-2 and radix-4 FFT algorithms:

a) The radix-2 DIT FFT algorithm:

A radix-2 decimation-in-time (DIT) FFT is the simplest and most common form of the Cooley–Tukey algorithm, although highly optimized Cooley–Tukey implementations typically use other forms of the algorithm as described below. Radix-2 DIT divides a DFT of size *N* into two interleaved DFTs (hence the name "radix-2") of size *N*/2 with each recursive stage[12].The equation (2) of DFT can be rewritten as:

$$X(k) = \sum_{n=0}^{\frac{N}{2}-1} x[2n] W_N^{2nk} + \sum_{n=0}^{\frac{N}{2}-1} x[2n+1] W_N^{(2n+1)k} \tag{3}$$

The decimation of data sequence can be repeated again and again until the resulting sequences are reduced to one-point sequences. For $N=2^v$, this decimation can be performed $v=\log_2 N$ times. Thus the total number of complex multiplication is reduced to ($N/2 \log_2 N$). the number of complex addition is ($N \log_2 N$)[13].In Fig.1 an example of computing 16 point DFT is shown. It can be noticed that the computation is performed in four stages, beginning with the computation of eight 2-points DFTs, then four 4-point DFTs, and then eight 2-point DFTs, and finally one 16- point DFT.

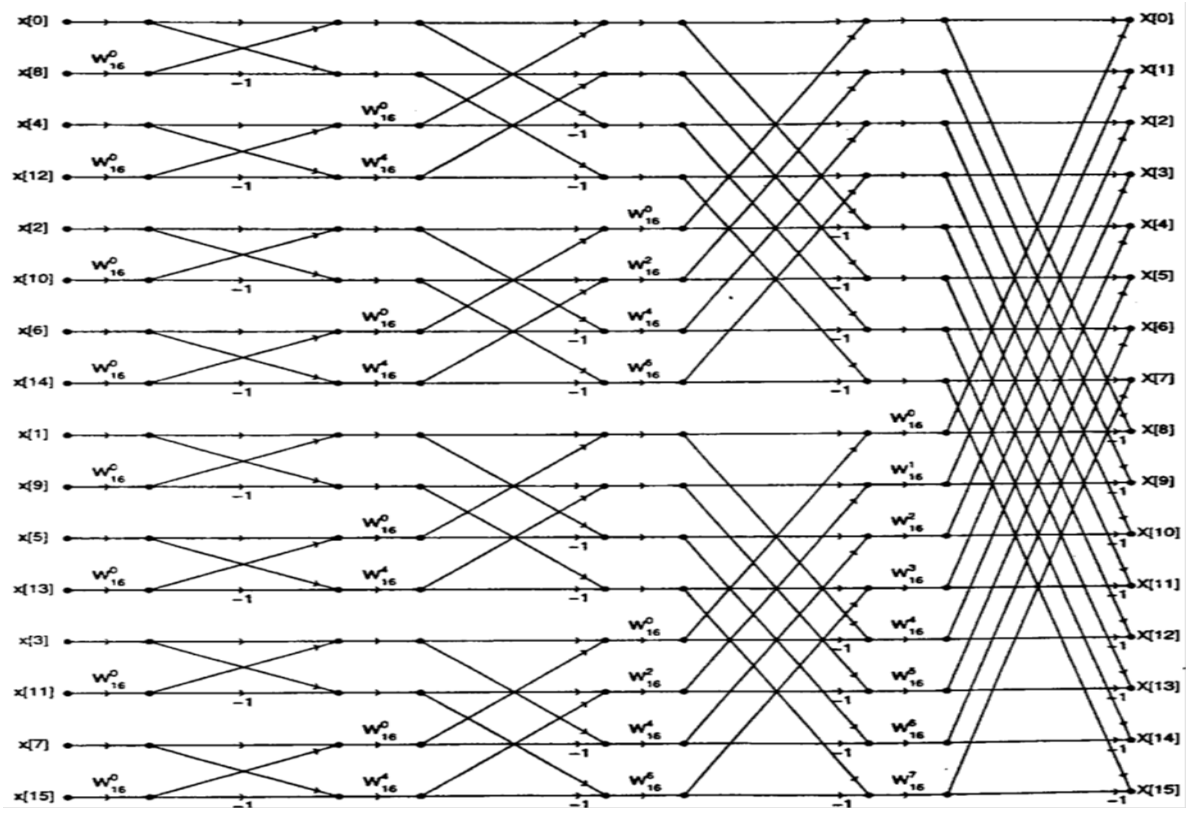


Figure 1:16-point radix-2 decimation-in-time algorithm

The butterfly is the basic computational unit of this algorithm,The name "butterfly" comes from the shape of the data-flow diagram in the radix-2 case and the butterfly operation is performed on a pair of complex numbers (a,b) to produce (A,B) asshown in Fig.2

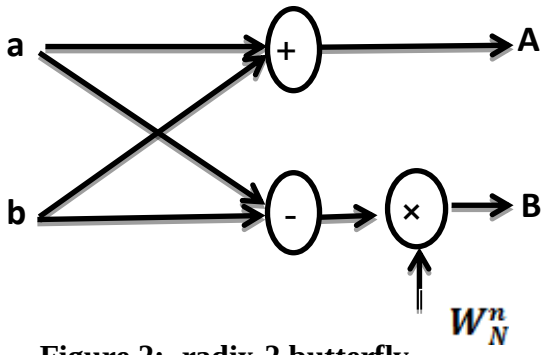


Figure 2: radix-2 butterfly

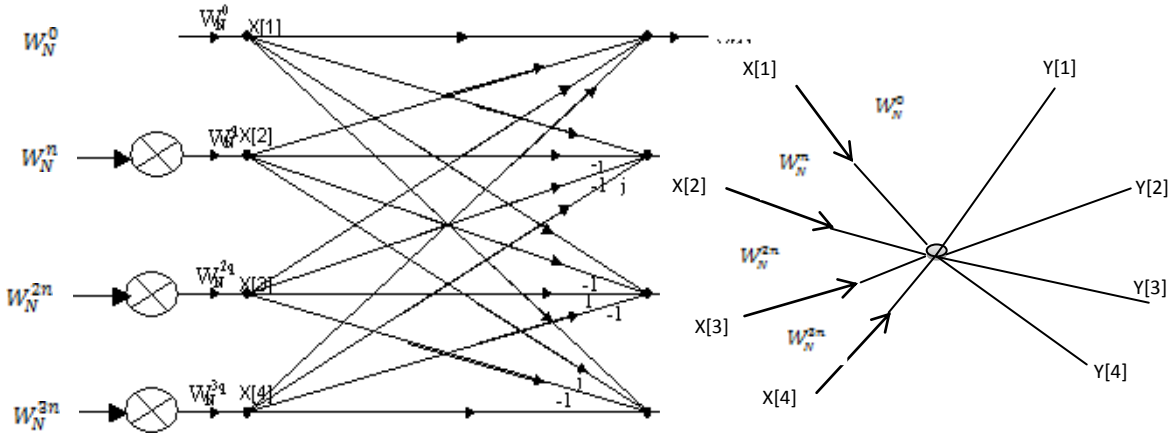
b) The radix-4 FFT Algorithms:

The radix-4 decimation-in-time algorithm rearranges the discrete Fourier transform (DFT) equation into four parts: sums over all groups of every fourth discrete-time index n=[0,4,8,…,N−4] , n=[1,5,9,…,N−3] , n=[2,6,10,…,N−2] and n=[3,7,11,…,N−1]

$$\left.\begin{aligned} X(4k) &= \sum_{n=0}^{N/4-1}[x(n)+x(n+N/4)+x(n+N/2)+x(n+3N/4)]\,W_{N/4}^{nk} \\ X(4k+1) &= \sum_{n=0}^{N/4-1}[x(n)-jx(n+N/4)-x(n+N/2)+jx(n+3N/4)]\,W_N^n W_{N/4}^{nk} \\ X(4k+2) &= \sum_{n=0}^{N/4-1}[x(n)-x(n+N/4)-x(n+N/2)-x(n+3N/4)]\,W_N^{2n} W_{N/4}^{nk} \\ X(4k+3) &= \sum_{n=0}^{N/4-1}[x(n)+jx(n+N/4)-x(n+N/2)-jx(n+3N/4)]\,W_N^{3n} W_{N/4}^{nk} \end{aligned}\right\} \quad \text{.....(4)}$$

for k=0 to N/4-1

The radix-4 butterfly is depicted in Fig.3. Note that since $W_N^0=1$, each butterfly involves three complex multiplications and twelve complex additions.



a-radix-4 butterfly **b-symbolic representation**

Figure 3: radix-4 butterfly and it's symbolic representation

Number of points N for radix-4 is a power of 4.(i.e., $N=4^v$) then the decimation-in-timeprocess can be repeated recursively v times. Hence the resulting FFT algorithm consists of v stages. Each stage contain N/4 butterflies. Concequently, the computation burden for the algorithm is $3vN/4=(3N/8)\log_2 N$ complex multiplications and $(3N/2)\log_2 N$ complex additions. It can be noticed that number of multiplications is reduced by 25%, but number of addition has increased by 50% from $N\log_2 N$ to $(3N/2)\log_2 N$[13].

An allustration of radix-4 decimation-in-time FFT algorithm is shown in Fig.4 for N=16. Note that in this algorithm, the input sequence in normal order while the output of DFT is in reversed order.

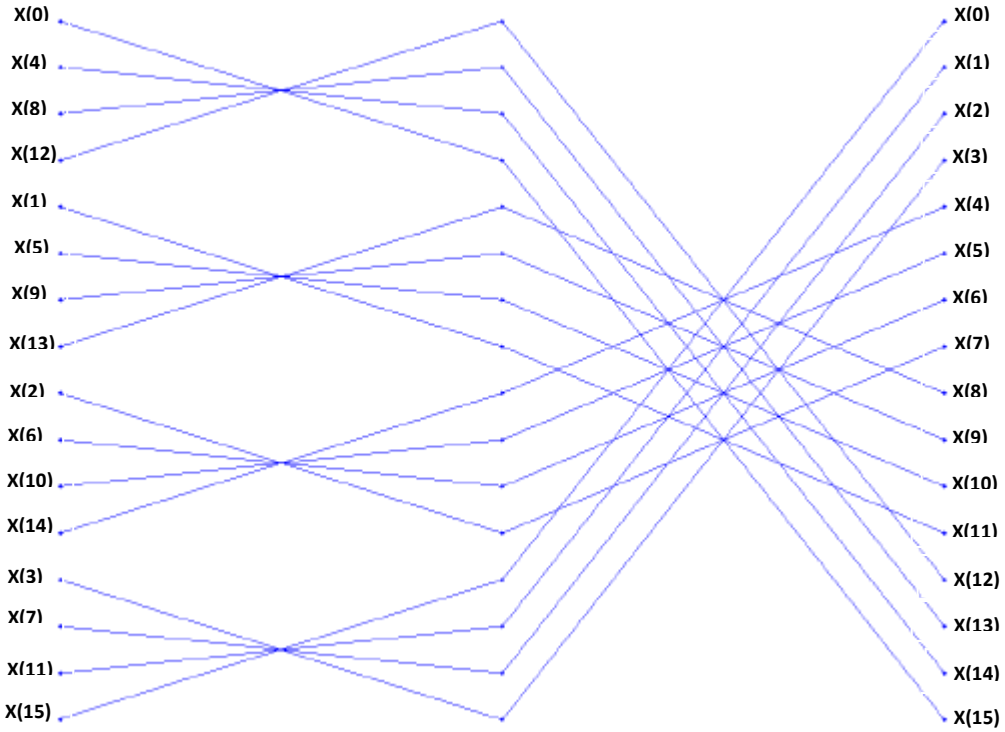


Figure 4:16-point radix-4 decimation-in-time algorithm

3. Modeling and architecture of FFT

In this paper a performance comparisonin respect to hardware recourses (chip utilization), and speed (throughput) oftwo different techniques namely System generator for DSP (Sysgen) and manually HDL method for FFT/IFFT (Fast Fouriere Transform/Inverse Fast Fouriere Transform) is presented.

In what follows, the basics and architectures of these two techniques are discussed.

3.1 Xilinx System Generator

System Generator is a system-level modeling tool that facilitates FPGA(Field Programmable Gate Array) hardware design. It extends Simulink of Matlab in many ways to provide a modeling environment that is well suited to hardware design. The tool provides high-level abstractions that are automaticall compiled into an FPGA at the push of a button. The tool also provides access to underlying FPGA resources through low-level abstractions, allowing the construction of highly efficient FPGA designs[14].

The Xilinx System Generator for DSP is a plug-in to Simulink that enables designers to develop high-performance DSP systems for Xilinx FPGAs. Designers can design and simulate a system using MATLAB, Simulink, and Xilinx library of bit/cycle-true models. The tool will then automatically generate synthesizable Hardware Description Language (HDL) code mapped to Xilinx pre-optimized algorithms. This HDL design can then be synthesized for implementation in Virtex-II Pro Platform FPGAs and Spartan-IIE FPGAs. As a result, designers can define an abstract representation of a system-level design and easily transform this single source code into a gate-level representation. Additionally, it provides automatic generation of a HDL testbench, which enables design verification upon implementation[15].

To program the Xilinx Logiccore FFT on the FPGA, two distinct software packages in Matlab and Xilinx ISE will be used. Matlab is the software where the brunt of the programming will take place, and ISE is where the program will be configured to run on the FPGA. The main bridge between the two packages is System Generator which is added as a part of Matlab to convert the Simulink math code to VHDL code that the ISE recognizes. Fig.5illustratesSystem Generator model for implemmenting the XilinxLogiccore FFT version 7.1 in simulink-Matlab.

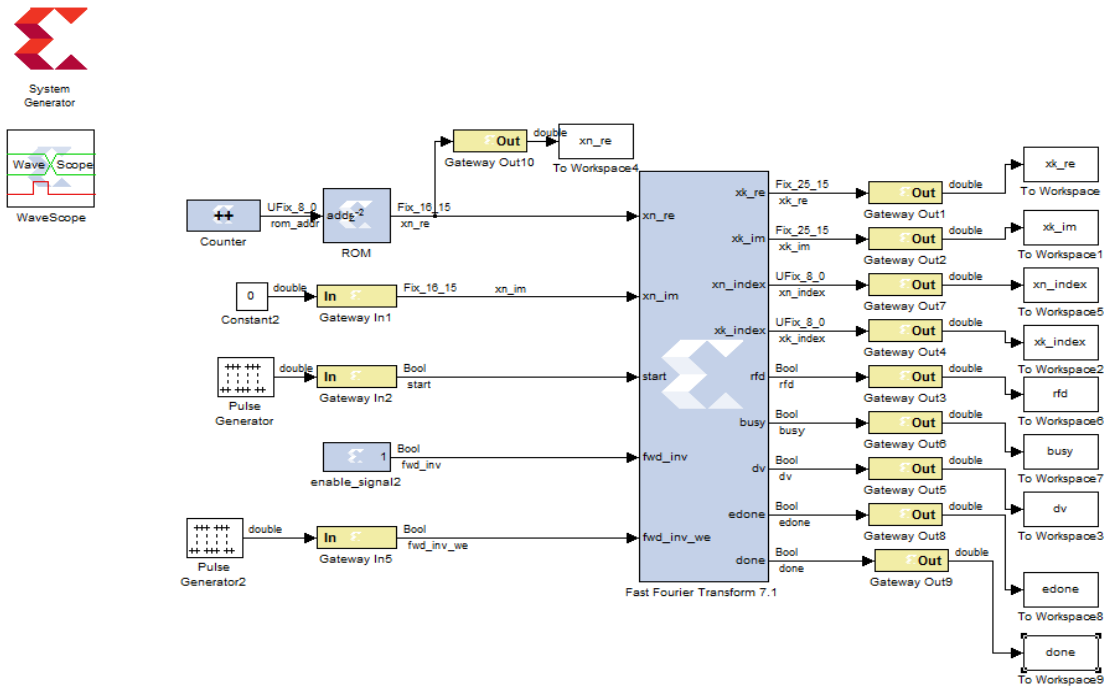


Figure 5: Simulink-System Generator Model for Xilinx Logiccore

By using the system generator we generate the HDL code for the four architecture of Xilinx Logiccore FFT that above-mentioned and create HDL behavioral model for them using Xilinx ISE.The Xilinx LogiCORE™ IP Fast Fourier Transform (FFT) implements the Cooley-Tukey FFT algorithm, computationally efficient method for calculating the Discrete Fourier Transform (DFT).The FFT core provides four different architectures to offer a trade-off between core size and transform time [16].

3.1.1 Architectures of Xilinx Logic core FFT:

a)Pipelined, Streaming I/O : The Pipelined, Streaming I/O solution pipelines several Radix-2 butterfly processing engines which connected using pipeline fashion to offer continuous data processing.Fig.6 illustrates the architecture.

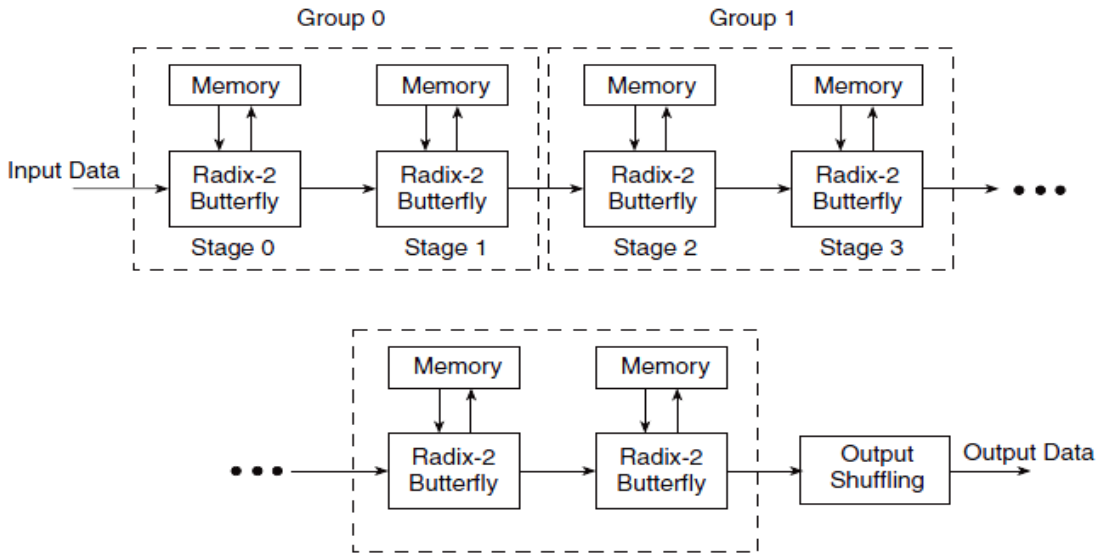


Figure 6: Pipelined, Streaming I/O[16]

b)Radix-4, Burst I/O: With the Radix-4, Burst I/O solution, the FFT core uses one Radix-4 butterfly processing engine.Fig.7 It loads and processes data separately and it is smaller in size than the pipelined solution, but has a longer transform time.

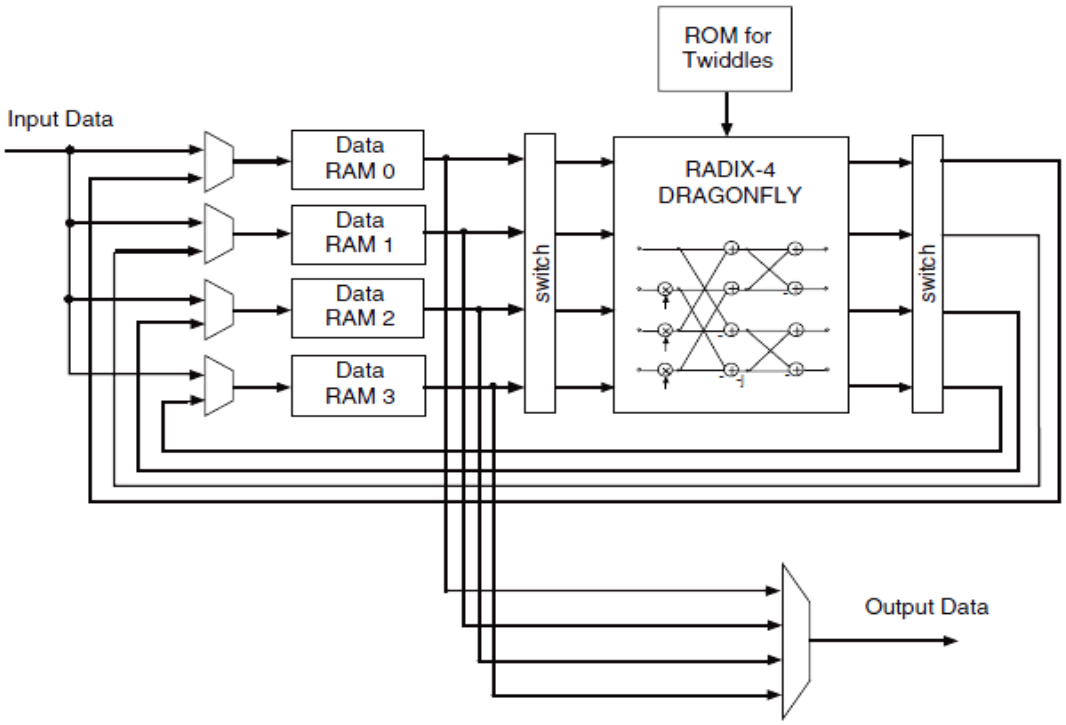


Figure 7: Radix-4, Burst I/O[16]

c)Radix-2, Burst I/O : The Radix-2, Burst I/O architecture uses one Radix-2 butterfly processing engine.Fig.8ItUses the same iterative approach as Radix-4, but the butterfly is smaller. This means it is smaller in size than the Radix-4 solution, but the transform time is longer.

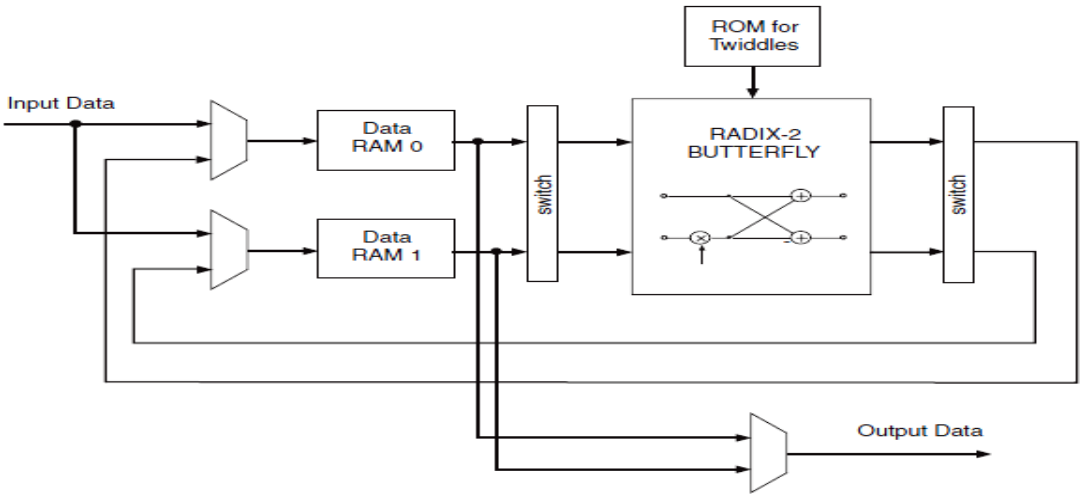


Figure 8: Radix-2, Burst I/O[16]

d)Radix-2 Lite, Burst I/O : This architecture differs from the Radix-2, Burst I/O in that the butterfly processing engine uses one shared adder/subtractor, hence reducing resources at the expense of an additional delay per butterfly calculationthis variant uses a time-multiplexed approach to the butterfly for an even smaller core.Fig.9[16].

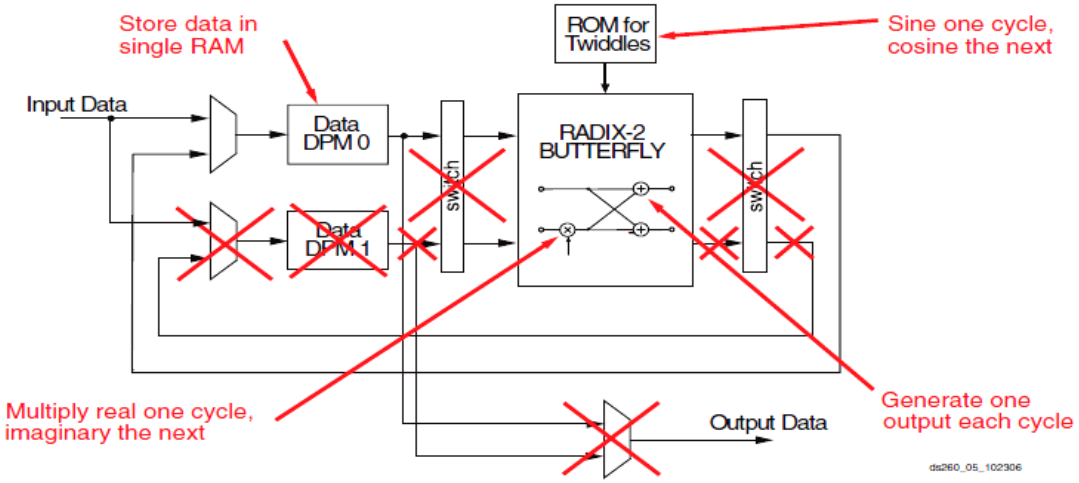


Figure 9: Radix-2 Lite, Burst I/O[16]

3.2 VHDL modeling of FFT/IFFT Processor using CORDIC algorithm

It can be observed that the four architectures of Xilinx Logiccore FFT utilized the ROM for storing the twiddle factors. For large input points, and if FFT and IFFT is to be implemented on the same platform, the required storage elements to store the twiddle factors and their conjugates becomes large and infeasible. To resolve this issue, CORDIC algorithm is used in this paper to generate the twiddle factor

3.2.1 Cordic (coordinate rotation digital computer) algorithm:

Coordinate Rotation Digital Computer is a set of shift-add algorithms for rotating vectors in a plane. It is a simple algorithm designed to calculate mathematical, trigonometric and hyperbolic functions. The CORDIC method can be employed in two different modes: rotation mode and vectoring mode.

The rotation mode is used to perform the general rotation by a given angle θ. The vectoring mode computes unknown angle θ of a vector by performing a finite number of micro-rotation. A vector $Vi(x_i,y_i)$ can be rotated through an arbitrary angle θ to obtain a new vector $V_{i+1}(x_{i+1},y_{i+1})$ [17]. Fig.10 shows an example for rotation of a vector Vi.

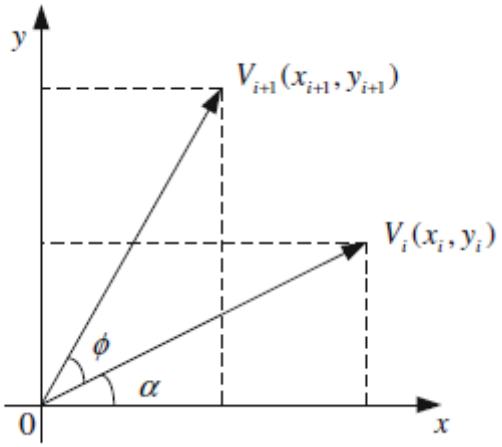


Figure 10: rotate vector $V_i(x_i,y_i)$ to $V_{i+1}(x_{i+1},y_{i+1})$

$$\begin{bmatrix} xi+1 \\ yi+1 \end{bmatrix} = \begin{bmatrix} xi \\ yi \end{bmatrix} \begin{bmatrix} cos\theta & -sin\theta \\ sin\theta & cos\theta \end{bmatrix}$$ generalized equation governing CORDIC operation is given by Eq.5:

(5)

$yi+1 = yi - xi.di \quad 2^{-i}$ It can be shown that rotation can be simplified to:

$$xi+1 = xi - yi.di \quad 2^{-i}$$

(6)

$$zi+1 = zi - di \quad tan^{-1}(2^{-i})$$

(7)

The angle accumulator adds a third difference equation to the cordic algorithm:

(8)

where diindicates the direction of the so called micro-rotation. In a conventional CORDIC, di∈ {−1, 1}.

The CORDIC rotator implements a rotation using a series of specified incremental rotation angles chosen so that each is achieved by a shift and add operation, typically for a *i*-bit Precision for input vector Vi, approximately *i*iterations are needed

It is particularly suited to hardware implementations because it does not require any multiplies [18].

There are three types of CORDIC structures: Sequential / iterative, Parallel / cascaded and Pipelined For the proposed FFT/IFFT processor, the pipelined CORDIC algorithm is used because it is the most efficient one [19].Fig.11 shows the pipelined CORDIC structure.

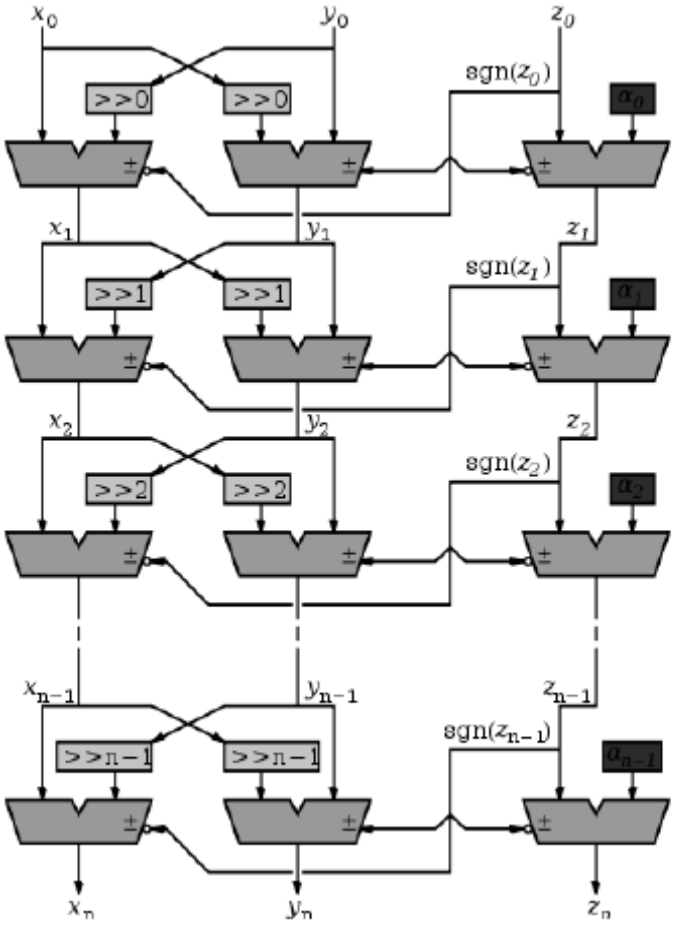


Figure 11: pipelined CORDIC structure

3.2.2 FFT/IFFT architecture with CORDIC

The FFT processor are designed using Radix-4 algorithm with configurable data width and a configurable number of sample points using VHDL language. Twiddle factors are generated using the CORDIC algorithm. The design flow of FFT/IFFT Processor is shown in Fig.12. The selector block is a memory buffer which determines the memory allocated for input samples which are written in the dual port RAM in addresses that are generated from the address generation unit. Then the control unit sends start signals to radix-4 butterfly and rotate factor generator units to start computing 4-point FFT in radix-4 butterfly and generating the required phase in rotate factor generator unit for the twiddle factor that will be generated in the CORDIC unit . The truncateand route unit is used to resize the width of data.

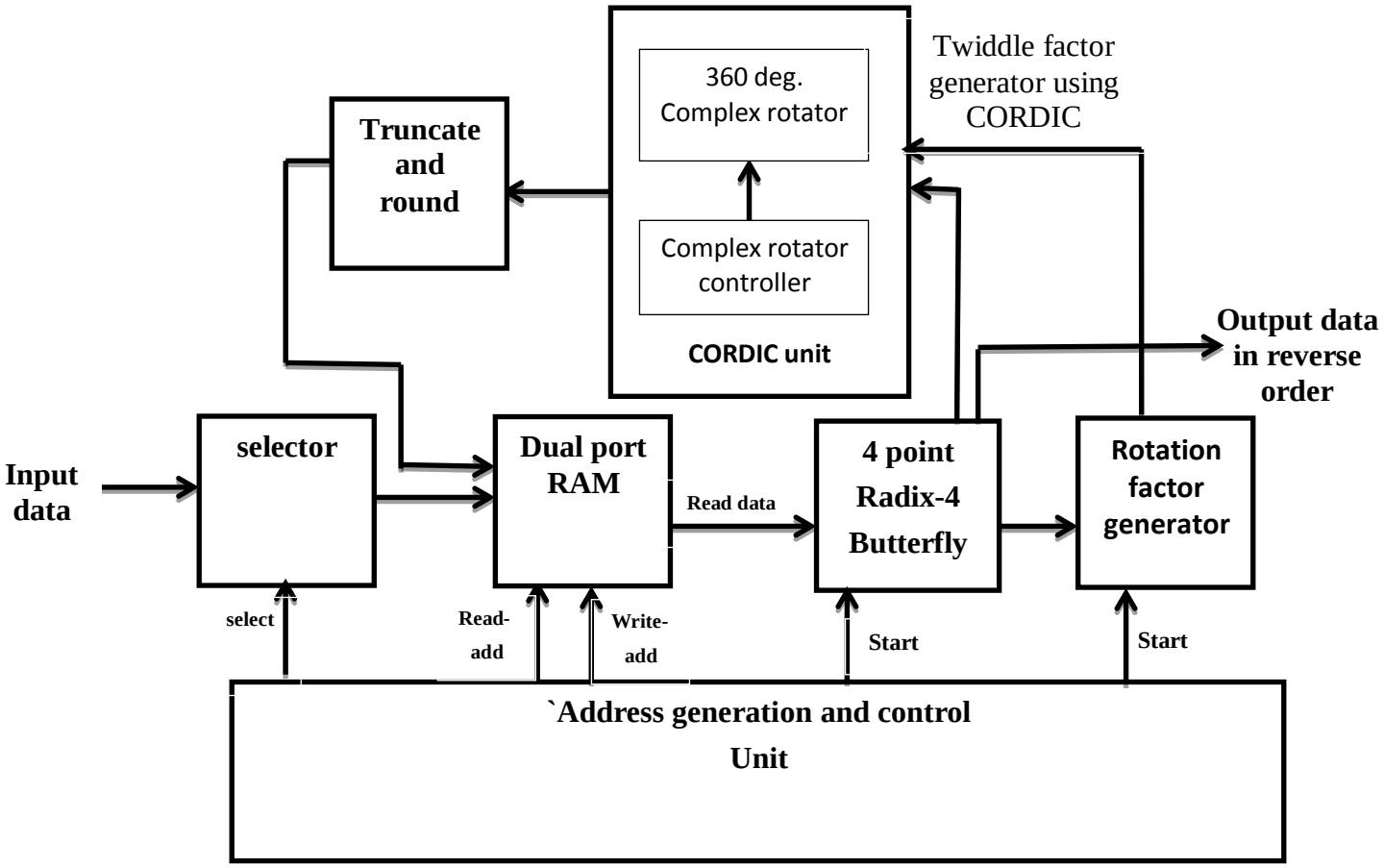


Figure 12: Architecture of FFT/IFFT processor using Cordic

4. Results and discussion:

The four architectures of Xilinx Logic core FFT (Pipelined-Streaming I/O, Radix-4-Burst I/O, Radix-2- Burst I/O, Radix-2 Lite-Burst I/O) and the CORDIC-based FFT/IFFT Processorare implemented by using (Spartan 3E-FPGA of 500.000 gates).

Both of the used techniques are scalable. For comparsion issue, a sequence of 1024 points each of 12-bit word length are analyzed using the mentioned two techniques and the twiddle factor word length is selected to be of 16-bit.A comparative study in terms of number of slices (area) and computation time (Latency), among all the mentioned architectures have been done. Fig.13 and Fig.14 illustrate the comparison.

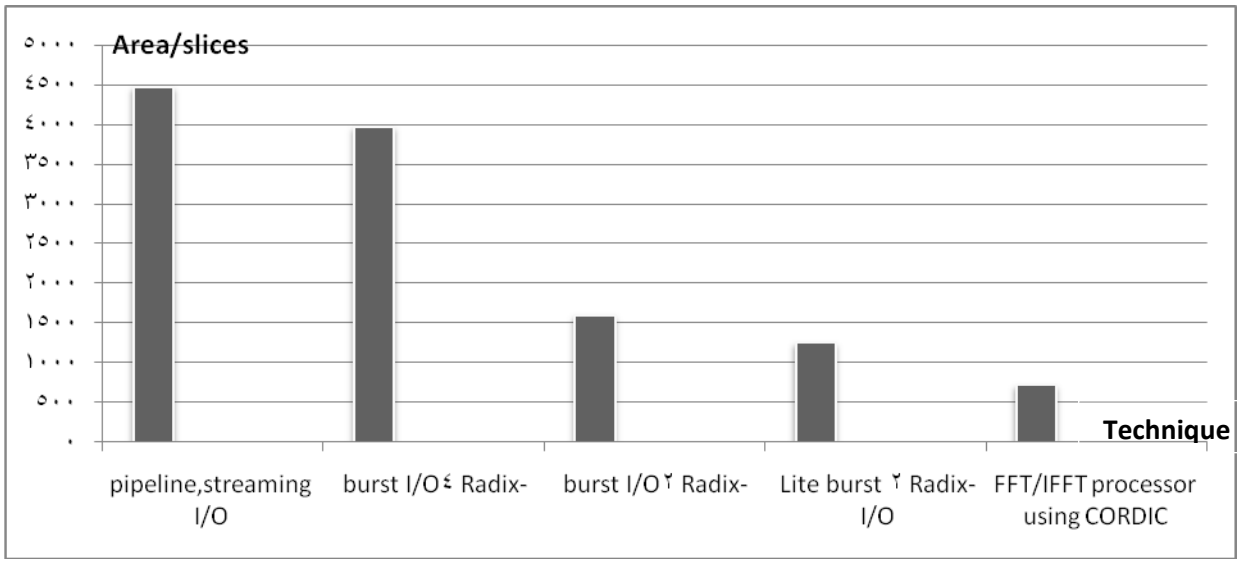


Figure 13: Comparative studies in terms of number of slices(area) among different architectures

In Fig.13, one can see that the CORDIC-based FFT/IFFT processor has a minimum number of slices because it uses the CORDIC algorithm to generate the twiddle factor insteade of saving it in ROM.

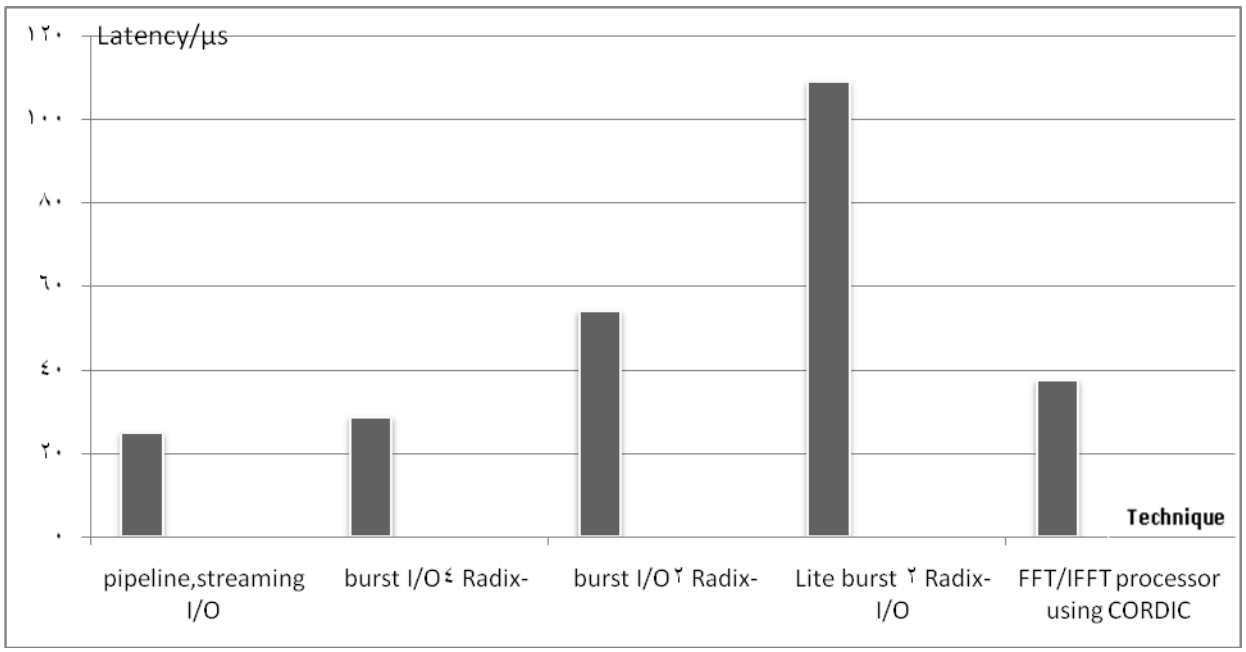


Figure 14 Comparative studies in terms of computation time (Latency) among different architectures

In Fig.14, one can see that the Pipelined-Streaming I/O architecture has a minimum latency as compared to other architectures because it uses pipelining technique**.**

5. Conclusion:

Using system generator as a helpful tool for implementing the architectures of Xilinx Logic-core FFTusing VHDL on FPGA gave us simplicity and flexibility in dealing with this architectures. .

The results of implementation the four architectures of Xilinx Logiccore FFT, which include (Pipelined-Streaming I/O, Radix-4-Burst I/O, Radix-2- Burst I/O, Radix-2 Lite-Burst I/O)in addition to the architecture of the CORDIC-based FFT/IFFT Processoris comparedin terms of number of slices (area) and computation time(Latency). .

In terms of number of slices (area), the CORDIC-based FFT/IFFT Processor is the best option because it requires few resources. It generates the twiddle factor when forward transform (FFT) is used and generates the conjugate twiddle factor for inverse transform (IFFT). It doesn't require any ROM for saving the twiddle factors therefore it's the best as compared to other architectures, which store the twiddle factors in ROM.

The Pipelined-Streaming I/O architecture is the best choice in terms of computation time(latency), it has a least latency because it uses pipelining technique which accelerate the circuit at the expense of cost therefore it requires most resources as compared to others.

It can be observed thatCORDIC-based FFT/IFFT Processor in terms of latency is less efficient thanPipelined-Streaming I/O and Radix-4-Burst I/O architectures, but more efficientthan Radix-2- Burst I/O and Radix-2 Lite-Burst I/O architectures..

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An FPGA HW/SW Co-Design for Real Time Video Edge Detection

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Abstract

This paper presents the concept of real time implementation computing tasks in Video Processing Platform (VPP) based on FPGA (Field Programmable Gate Arrays) architecture using EDK embedded system and Xilinx System Generator. This hardware/software co-design platform has been implemented on a Xilinx Spartan 3A DSP FPGA. The video interface blocks are implemented and the MicroBlaze soft processor is used as an embedded video processing. This paper discusses the architectural building blocks for edge detection showing the flexibility of the proposed platform. This flexibility is achieved by using a new design flow based on Xilinx System Generator. This video processing platform allows custom-processing blocks to be plugged-in to the platform architecture without modifying the front-end (capturing video data) and back-end (displaying processed output). The Xilinx Embedded Development Kit (EDK) design tool is used for the required hardware and software to work in an integrated fashion (SoPC). This paper presents several examples of video processing applications, such as a Prewitt and Sobel edge detector that have been realized using the Video Processing Platform (VPP) for real-time video processing.

Keywords: Real time, Embedded system design, Embedded Development Kit (EDK), FPGA-based design, hardware-software co-design, , video processing, Edge detection.

تصميم يجمع بين المكونات المادية والمعالج البرمجي المطمور في مصفوفة البوابات القابلة للبرمجة حقليا لاستخراج حواف الفيديوهات في أنظمة الزمن الحقيقي

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الملخص

يعرض هذا البحث تنفيذ معمارية المعالجة الفيديوية في الزمن الحقيقي باستخدام مصفوفة البوابات القابلة للبرمجة حقليا المعمارية صُممت بعدة التطوير المُضمن ومولد النظام لشركة Xilinx . هذا الدمج بين المكونات المادية والمعالج الدقيق المطمور في مصفوفة البوابات القابلة للبرمجة حقليا نفذ على رقاقة Spartan 3A DSP. تم تنفيذ كتل واجهة الفيديو و أستخدم المعالج المرن MicroBlaze كوحدة مضمنة لمعالجة الفيديو. يناقش هذا البحث معمارية للكشف عن الحواف للفيديوات في الزمن الحقيقي بمرونة. ويتم تحقيق هذه المرونة باستخدام كتل مولد النظام الخاص بشركة Xilinx. هذه المعالجة الفيديوية المقترحة تسمح باستبدال كتل مخصصة للمعالجة، الواجهة الأمامية (التقاط بيانات الفيديو) والنهائية (عرض الفيدوهات). استخدمت عدة التنمية المطمورة كأداة للدمج ما بين الجزء البرمجي و المادي مما أتاح العمل في بيئة متكاملة واحدة مما جعل النظام مجتمع على رقاقة واحدة قابلة للبرمجة. اقترح هذا البحث عدة أمثلة للمعالجة الفيديوية منها نوعين لكشف الحافات في الزمن الحقيقي.

1. Introduction

Applications such as cell phones, hearing aids, and digital audio devices are applications with stringent constraints such as area, speed and power consumption. These complex applications can be well addressed by Systems On Programmable Chip (SoPC). Such applications require an implementation that meet these constraints with the minimum time to market.

Modern Field Programmable Gate Arrays (FPGAs) contain many resources that support DSP applications such as embedded multipliers, Multiply Accumulate (MAC) units and processor cores. The motivation for the introduction of such processor core comes from the idea that most FPGAs contained within an embedded system require interaction level with an external processor. Moving this processor onto the chip allows the FPGA and the processor to communicate without the bottlenecks associated to communicating with off-chip devices. Altera, Atmel and Xilinx are programmable logic manufactures offer FPGAs platform [1]. The propose devices that integrate hardware cores of processors such as ARM, MIPS and PowerPC. And soft processor such as MicroBlaze from xilinx and Nios from Altera, DSP and microcontroller cores like PicoBlaze.

Embedded Systems are hardware and software components working together to perform a specific application. Embedded Systems exist in a modern society and play a vital role in everyday lives. The hardware platform of the embedded system often consists of one or more processors, along with a verity memory blocks peripherals. In order to create embedded system which able to detect the edge of the input frames with a high performance, low power consumption and low cost, can be used System on Programmable Chip (SoPC). SoPC is a complete embedded system on a single chip. The SoPC consist of pre-designed complex blocks (or so-called cores or IP blocks). SoPC design techniques are focused on the problems of integrating, verifying multiple pre-existing blocks and software components[2]. In SoPC the main task has divided into two major sub tasks. One of this is implemented in hardware and other in software. The hardware subtask is mainly performed by using an Intellectual-Property (IP) core and software subtask is performed on embedded processor inside the FPGA. So hardware-software co-design offers dynamic reconfiguration to the system.

Edge detection is a fundamental tool used in most image processing applications to obtain information from the frames as a precursor step to feature extraction and object segmentation. This process detects outlines of an object and boundaries between objects and the background in the image. An edge-detection filter can also be used to improve the appearance of blurred or anti-aliased video streams [3]. Implementing image processing algorithms on reconfigurable hardware minimizes the time-to-market cost, enables rapid prototyping of complex algorithms and simplifies debugging and verification. Therefore, FPGAs are an ideal choice for implementation of real time image processing algorithms [4].

With the evolution of FPGA architecture, it has in build processor for designing reconfigurable embedded system. The design involves use of processor, hardware logic IP and its integration. This is termed as System on Chip (SoC) design [5].

The Xilinx Embedded Development Kit (EDK) is offered for SoPC design platform. It provides a rich set of tools like Software development kit (SDK) to develop embedded software application and Xilinx platform studio (XPS) for hardware development and with a wide range of embedded processing Intellectual Property (IP) cores including processors and peripherals.

Integrating all the cores with processors inside the FPGA leads to reconfigurable embedded processor system [2].

The introduction of high level hardware system modeling tools has further accelerated the design of image processing in FPGA. The Xilinx System generator (XSG) offers a new design methodology that uses a model based approach for design and implementation of Digital Signal Processing (DSP) applications in FPGA [6].

The objective of this work is to develop a real-time video processing platform (VPP) with an input from a CMOS camera and output to a DVI display and verified the results video in real time. It is an edge detector processing as a hardware component with possibility to change the threshold until reach the suite one by using Microblaze soft processor. At first design a hardware platform utilizing the flexibility in the system generator are implemented, which consists of all the hardware components of the system and their connections through buses their interfaces. These steps are designed in XPS (Xilinx Platform Studio) which is part of EDK. There are already lots of standard supported modules available in the tool that can be added to the hardware platform [7]. Software subtask is performed on a processor inside the FPGA(code running on an embedded CPU core) in XPS program.

The rest of this paper is organized as follows. In section 2, the previous work is presented. The concept of SoPC Design using Xilinx Tools is discussed in section 3. Experimental result are given in section 4. Finally, conclusions are presented in section 5.

2. Previous Work

The following are the few papers that were referred to, in the process of designed this project. Following are some of the literature that has somehow contributed for understanding of the Sobel edge detection, Prewitt edge detection, real time video systems and HW/SW Co-Design system on chip(SoPC).

- Y. SAID et al. [2] design of Sobel edge detector system on FPGA. The design is developed in System Generator and integrated as a dedicated hardware peripheral to the Microblaze 32 bit soft RISC processor with the EDK embedded system and using constant threshold.
- Y. SAID et al. [8] presented several examples of video processing applications, such as a Prewitt edge detector and video wavelet coding that have been realized using the Video Processing Platform (VPP) for real-time video processing.
- A. Hassan[9] presented method to processing video by utilizing the concept of co-design to implement it in Spartan 3E. The Artificial Neural Network (ANN) is used to improve the system by its parallelised computing and to detect the edges of an image within an embedded system. The ANN contained ten entries, one hidden layer of two neurons and one output layer with one neuron, which represents an edge of the image.
- J. Majumdar et al.[10] briefly explains the implementation of several edge detection algorithms like Sobel, Prewitt, Robert and Compass edge detectors on FPGA and makes a comparative study of their performance.
- F. Kristensen et al.[11] , the design of an embedded automated digital video surveillance system with real-time performance is presented. Hardware accelerators for video segmentation, morphological operations, labeling and feature extraction are required to

achieve the real-time performance while tracking will be handled in software in an embedded processor.

- N. P. Sedcole [12], implemented a modular dynamic FPGA reconfiguration for real time video architectures in his thesis.
- R.Peesapati et al. [5], is performed System on Chip (SoC) platform. In this work, two methods are proposed for creating IP core, one for design Distributed Arithmetic FIR (DAFIR) filter by using Create and Import peripheral CIP and the second using system generator for design Fast Fourier Transform (FFT) IP core on Xilinx Virtex-II Pro XC2VP30 FPGA.

In this paper, the complete system on chip has been implemented on the hardware beside the threshold has been computed by the soft processor only, that gives an extra computation affects the overall system performance.

3. SoPC Design using Xilinx Tools:

The board used for VPP is the VSK Spartan 3A-DSP Platform developed by Xilinx [13]. This board has Xilinx Spartan-3A DSP XC3SD3400A-4FGG676C FPGA with 53,712 logic cells, 126 DSP48A Slices, and 2,268Kb of block ram (BRAMs).

The data stream from the camera is in the form of a high-speed LVDS data stream. This stream is received and deserialized using a National DS92LV1212A deserializer. This is capable of carrying LVDS data from a camera which has a pixel rate of 26.6 MHz [13]. This board is ideal for a video processing platform since it has all the hardware necessary to capture and display the data on a monitor. Video data are captured from the camera at a resolution of 720x480P at 60Hz.

Then these data are sent through a Gamma block for data correction, and then on to the video to VFBC, so that we only send the active data into the MPMC. The default is a 3-frame buffer, and a simple sync signal that is connected between the video to VFBC and the display controller to make sure that we read out one frame behind what is being written into the external memory. The display controller then reads data out of memory and passes it to the DVI out. A flexible architecture that enables real-time image and video processing are built. The overview of the design is given in Figure 1.

The system is controlled by a MicroBlaze processor [14] that initializes the VPP peripherals and controls the video processing and frame buffer pipelines by reading and writing control registers in the system.

The MicroBlaze soft processor core is a 32-bit Harvard Reduced Instruction Set Computer (RISC) architecture optimized for implementation in Xilinx FPGAs with separate 32-bit instruction and data buses running at full speed to execute programs and access data from both on-chip and external memory at the same time [14]. It is used as an embedded video threshold controller in this design.

The peripherals are connected to the Embedded MicroBlaze processor through Processor Local Bus (PLB). The Processor is connected to dual-port SRAM, called Block RAM (BRAM), through Local Memory Bus (LMB). This bus features separate 32-bit wide channels for program instructions and program data, using the dual-port feature of the BRAM. The LMB provides single-cycle access to on-chip dual-port Block RAM.

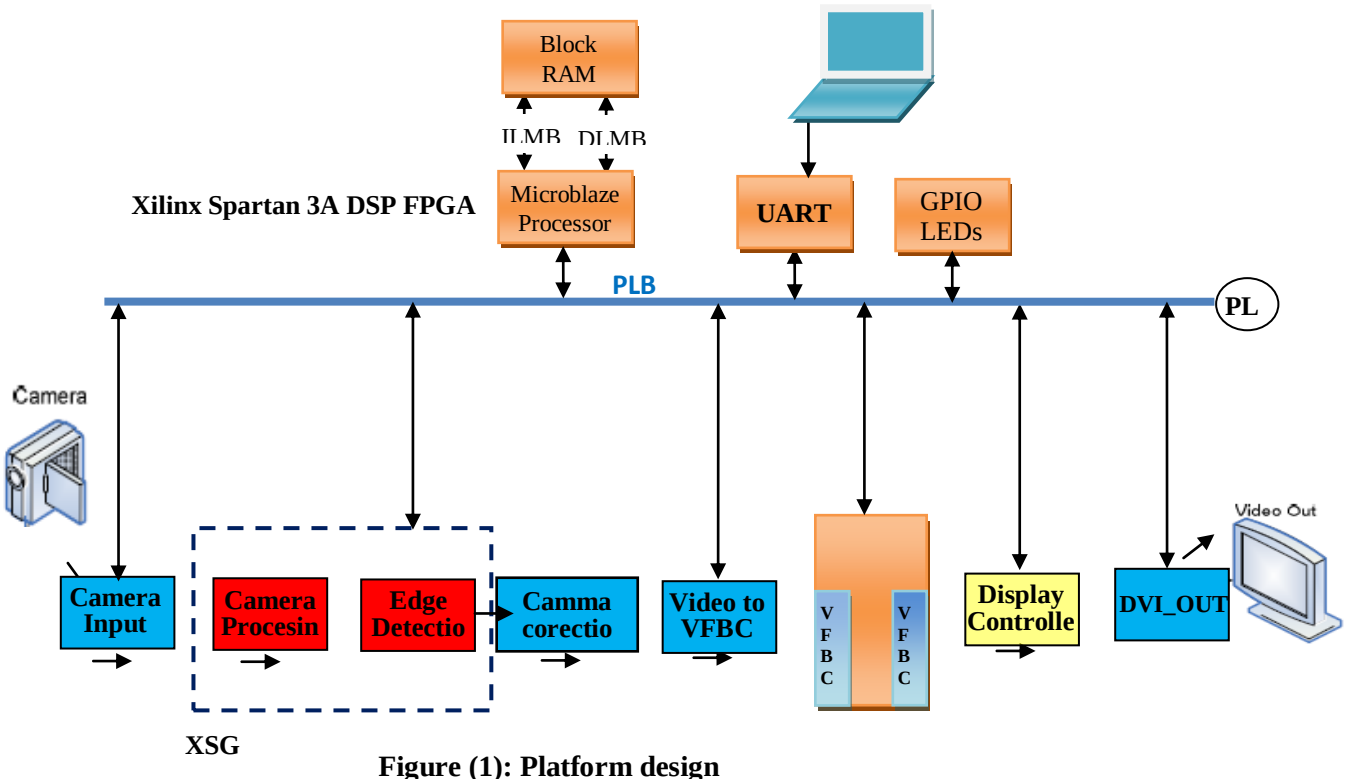


Figure (1): Platform design

The Embedded Development Kit (EDK) is offered by Xilinx for SoPC design platform. It provides a rich set of tools like Software development kit (SDK) for software development and Xilinx platform studio (XPS) for hardware development and with a wide range of standard IPs and Processors like MicroBlaze, PowerPC etc. Integrating all the cores with processor inside the FPGA leads to reconfigurable embedded processor system [2].

3.1. System Generator for DSP(sysgen)

Sysgen offers a new design methodology that uses a model based approach for design and implementation of DSP applications in XILINX FPGA. Simulation in Sysgen uses cycle accurate and bit-true accurate simulation for simulating the design. Various components in Sysgen environment that describes the entire design is:

- ***EDK Processor:*** The EDK Processor IP block provides an interface to MicroBlaze and Custom logic being developed in Sysgen. In this paper export IP core technique is used for designing SoPC system. The EDK Processor block allows System Generator Shared Memory blocks (i.e., "From/To Register"s, "From/To FIFOs", and "Shared Memory"blocks) to be associated with a processor through an automatically generated memory map interface. Once associated, that memory can be read or written in software running on the MicroBlaze processor[15].

- ***Custom Logic:*** These are the block sets used for designing an IP for DSP, communication, logical, relational, mathematical, shared memory, importing HDL models and for custom logic.

3.2 Design of Modules

The FPGA is connected to a CMOS camera, a VGA monitor and an external DDR2 DDRAM memory through the camera interface module, memory interface module and display interface module respectively. In addition there are four modules that perform the video processing task. The filter module performs the pre-processing to the pixels acquired in the camera interface module.

3.2.1 Camera Interface Module

The Video Starter Kit (VSK) consisting of Spartan 3A DSP XCSD3400A FPGA connected to a Micron CMOS camera of resolution 720 x 480 pixels delivering frames at 60 fps through a FPGA Mezzanine Card (FMC) Daughter card used for decoding the data arriving through the serial LVDS camera interface. The de-serialized input consists of V-Sync, H-Sync and 8 line data bus which serves as the input for the Edge detection model. The edge filter is applied in the Camera Processing block on the input signal arriving from the Camera In block. The output signal is Gamma corrected for the output DVI monitor and is driven by Display controller to the DVI output monitor. Video to VFBC and MPMC core helps us to store the image data and buffer them to the output screen[10].

3.2.2 Edge Detector

An edge, in an image, is a collection of connected high frequency points. Visually, an edge is a region in an image where there is a sharp change in intensity of the image. Edge detection refers to the operation performed on an image to detect the edges in an image. The output of edge detection is usually thresholded to retain only the edge. Edge detection plays a vital role in object detection and feature extraction and plays pivotal role in machine vision. There are different types of edges detection: Roberts, Sobel, Prewitt, Canny and etc. In this paper, Sobel edge detection is presented[16].

3.2.2.1 Sobel Edge Detector

Edge detection is the process of localizing pixel intensity transitions. The Sobel operator is an algorithm for edge detection in images discovers the boundaries between regions also it determine and separate objects from background in an image. It's an important part of detecting features and objects in an image. The Sobel edge detection algorithm uses a 3x3 table of pixels to store a pixel and its neighbors while calculating the derivatives. The 3x3 table of pixels is called a convolution table, because it moves across the image in a convolution-style algorithm. Figure 2 shows the convolution table at three different locations of an image: the first position , the last position and the position to calculate whether the pixel at [i;j] is on an edge. And figure 3 shows the convolution table containing the pixel located at coordinate [i,j] and its eight neighbors. The Sobel method finds edges using the Sobel approximation to the derivative. It returns edges at those points where the gradient of I is maximum, where the gradient of the considered image is maximum. The horizontal and vertical gradient matrices whose dimensions are 3×3 for the Sobel method has been generally used in the edge detection operations, where A as the source

image, Gx and Gy are two images the horizontal and vertical derivative approximations are as follows. These filters estimate the gradients in the horizontal (x) and vertical (y) directions and the magnitude of the gradient is simply the sum of these 2 gradients[16].

-1	-2	-1
0	0	0
1	2	1

(a)

-1	0	1
-2	0	2
-1	0	1

(b)

Figure (2) Sobel Edge detector – (a) Horizontal and (b) Vertical Kernel

Gradient magnitude is given by:

$$G = \sqrt{G_x^2 + G_y^2} \approx |G_x| + |G_y|$$

Gradient direction is given as,

$$\theta = tan^{-1}(\frac{G_y}{G_x})$$

The implementation of the Edge detector consists of RGB to grayscale color space conversion and line buffers to synchronize H-sync, V-sync and Data-enable signals by applying the following equation, the block diagram is shown in figure 3.

Gray-Scale= 0.3 * R +0.59 *G + 0.11 *B

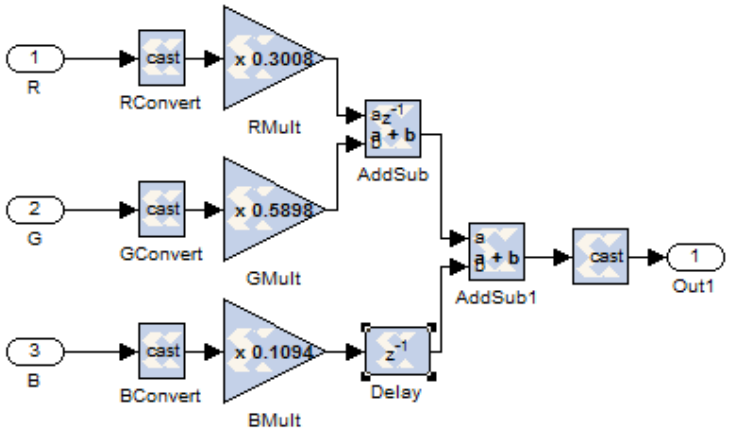


Figure (3): Color conversion Block

The filter and buffer block consists of line buffer to hold the corresponding rows and edge detector block. The edge detector block consists of two convolution block which performs the operation specified by the kernel. Individual rows of each kernel are multiplied by the delayed elements which are stored in the line buffers to yield vertical and horizontal edges. These are added and gradient magnitude is found out. The gradient magnitude is thresholded using a manual threshold to obtain proper edges. The Complete system shown in figure (4).

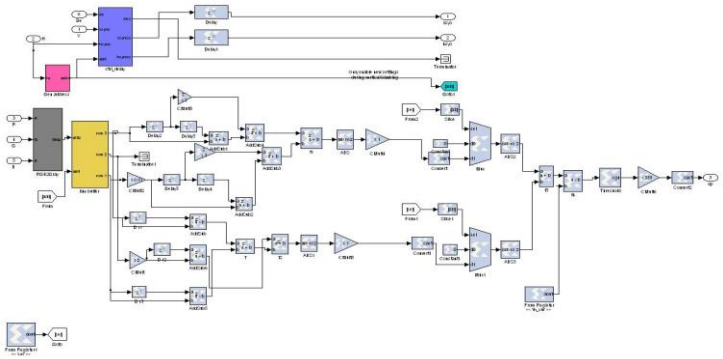


Figure (4): Complete Real time system for edge detection

3.2.2.2 Prewitt Edge Detector

Prewitt edge detector is a 2D edge detector with a 3x3 kernel. The kernel is almost similar to the Sobel operator except for the weights assigned to the center pixels. The kernel is shown below in figure 5.

-1	-1	-1
0	0	0
1	1	1

(a)

-1	0	1
-1	0	1
-1	0	1

(b)

Figure (5): Prewitt Edge detector – (a) Horizontal and (b) Vertical Kernel

3.2.3 Hardware/Software Implementation

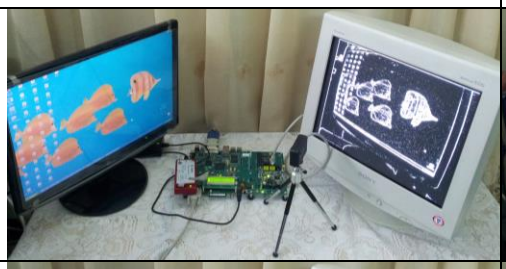
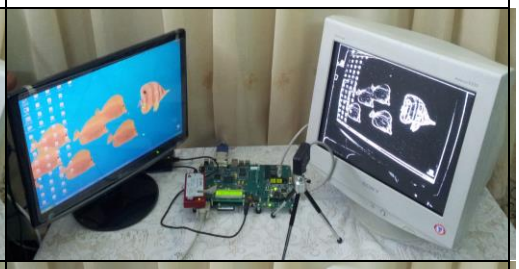
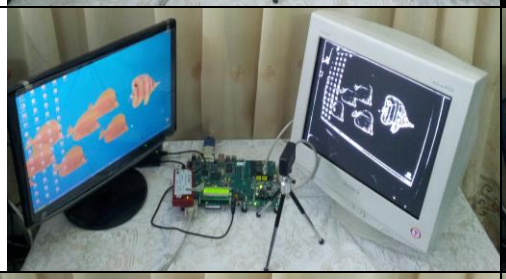
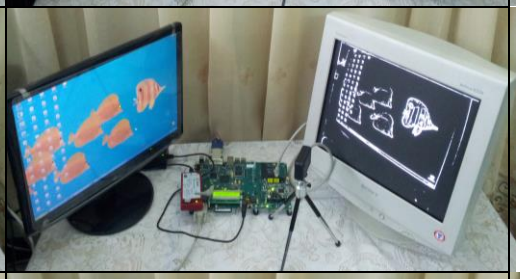
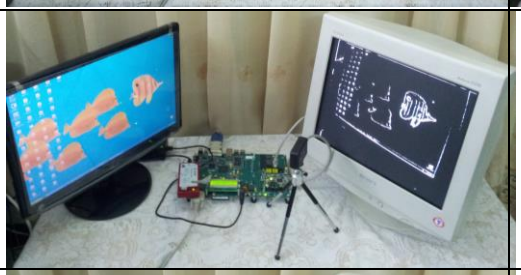
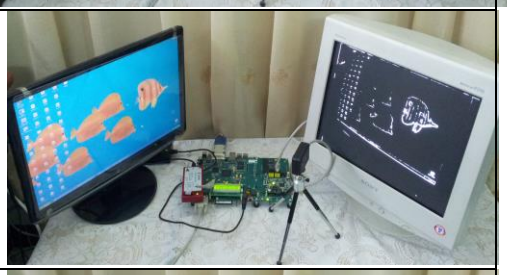
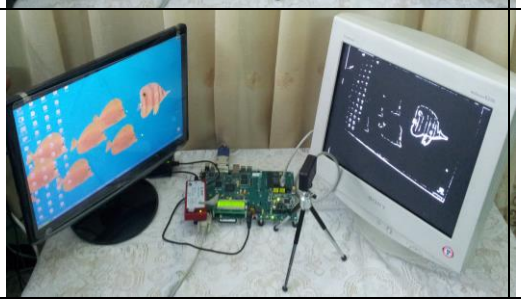
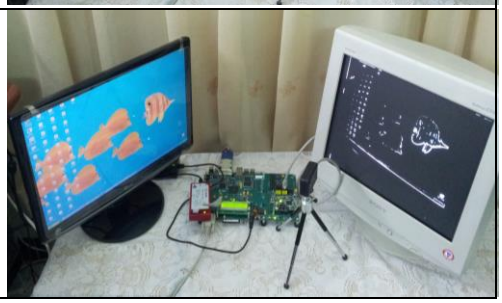
One of the biggest challenges of this architecture was to get a System On a Programmable Chip (SOPC). This means implementing both software and hardware components. As the target device, a Spartan-3A Video starter kit was chosen due to its flexibility, great promise of integrating both the hardware and software co-designs into one.

The soft core Processor MicroBlaze is used in a standalone mode to run a software program (written in C) which is loaded into BRAM. The MicroBlaze processor achieves the thresholds computation then sends the results to the edge detection hard Block to compute the filter outputs.

4. Result:

The different edge detection operators implemented in this paper are given below along with their corresponding hardware outputs obtained. The input image utilized for edge detection and outputs of various operators is shown in Table (1).

Table (1): Real time Edge Detection for Sobel and Prewitt operator in different thresholds

Thresholds	Sobel filter	Prewitt filter
20		
30		
40		
50		
60		

The total resource usage for the system, including the MicroBlaze, bus structure, the Soble, Prewitt edge core and peripherals, is 9,791 slices, equaling 20 % of the FPGA's total resources. Table 2 shows the amount of logic used for the edge module. The post-synthesis resource usage

of this module is 5%. It has a post-synthesis maximum estimate frequency of 62.783 Mhz. is shown in table 2.

Table (2): Resources utilized

Logical utilization	Used	Utilization
No. of Slice	9,791	20%
LUT	10,825	22%
No. of Bounded IOs	187	39%
No. of DSP48A	7	5%
DCM	2	25%

5. Conclusion

Continual growth in the size and functionality of FPGAs over recent years has resulted in an increasing interest in their use as implementation platforms for image processing applications, particularly real-time video processing.

In this work, a Video Processing Platform (VPP) for real-time video processing is presents. This video platform were implemented on Spartan-3A FPGA at a rate of 60 fps for an input image of resolution 720x480. Two applications have been presented showing the performance and flexibility of the proposed platform. For the system architecture, including the MicroBlaze, bus structure, the Soble/Prewitt edge core and peripherals, the total resource usage is 9,791 slices, equaling 20% of the FPGA's total resources. It has a post-synthesis maximum estimate frequency of 62.783 MHz.

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Design and Implementation of Decimation Filter for 15-bit Sigma-Delta ADC Based on FPGA

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Abstract

A 15 bit Sigma-Delta ADC for a signal band of 40K Hz is designed in MATLAB Simulink and then implemented using Xilinx system generator tool. The first order Sigma-Delta modulator is designed to work at a signal band of 40 KHz at an Oversampling ratio (OSR) of 512 with a sampling frequency of 40.96 MHz. The proposed decimation filter design consists of a second order Cascaded Integrator Comb filter (CIC) followed by two finite impulse response filters. This architecture reduces the need for multiplication which needs very large area. This architecture implements a decimation ratio of 512 and allows a maximum resolution of 15 bits in the output of the filter. The decimation filter is designed and tested in Xilinx system generator tool which reduces the design cycle by directly generating efficient VHDL code. The results obtained show that the overall Sigma-Delta ADC is able to achieve an ENOB (Effective Number Of Bit) of 14.71 bits and SNR of 90.3 dB.

Keywords: Sigma-Delta modulation, decimation filter, A/D conversion, oversampling, FPGA, VHDL.

تصميم وتنفيذ مرشح الـقاتل للمحول التناظري الى رقمي نوع سيكما دلتا بدقة 15 bit باستخدام البوابات القابلة للبرمجة حقلياً

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الخلاصة

تم تصميم وتنفيذ المحول التناظري الى الرقمي نوع سيكما دلتا بدقة 15 bits وبحزمة ترددية مقدارها 40 KHz باستخدام برنامج الماتلاب ومولد النظام. تم تصميم المضمن سيكما دلتا ذو الرتبة الاولى عند حزمة ترددية مقدارها 40 KHz، و (Oversampling ratio) مقدارها 512 ،وتردد نمذجة مقداره 40.96 MHz. يتكون مرشح (Decimation) المقترح من المرشح (CIC) ذو الرتبة الثانية ومرشحي الاستجابة محدد النبضة. المعمارية المقترحة لتنفيذ مرشح الـ(Decimation) تقلل من الحاجة إلى دائرة الضرب التي تحتاج مساحة كبيرة جداً عند التنفيذ. تعمل المعمارية المقترحة للمرشح الـ(Decimation) على تقليل تردد النمذجة بمقدار (512) وجعل الدقة في اخراج المرشح تساوي 15 bits.المعمارية المقترحة لتنفيذ مرشح الـ(Decimation) تقلل من الحاجة إلى دائرة الضرب التي تحتاج مساحة كبيرة جدا عند التنفيذ. تم تصميم وفحص المرشح (Decimation) باستخدام مولد النظام مما ساعد على تقليل دورة التصميم عن طريق توليد مباشر للكيان المادي الخاص بتنفيذ المرشح (Decimation). أظهرت النتائج النهائية ان مقدار نسبة إشارة المعلومات إلى الإشارة الضوضائية للمحول المقترح كانت تساوي90.3 dB ، وأن مقدار الـ(ENOB) كان يساوي 14.71 bits.

1. Introduction

In many modern electronic systems the key components are the analog to digital converters. They provide the translation of a measured analog signal to a digital representation. In the digital form the data can be easily and accurately processed to extract the information desired. The process of converting the analog signal to a digital signal some time limits the speed and resolution of the overall system. Therefore, it is necessary to develop analog to digital converters that achieve both high speed and resolution. In particular, many instrumentation, communication, and imaging systems can benefit from such converters[1, 2].

There are different types of analog to digital conversion techniques available today, each having its own advantages and disadvantages. Analog-to-digital converters are categorized into two types namely Nyquist rate converters and oversampling converters depending on the sampling rate. Sigma-delta ADCs come in oversampling converters group[3,4].

Oversampling converters reduce the requirements of analog circuitry at expense of faster and more complex digital circuitry [5,6]. Sigma Delta analog-to-digital converters need relatively imprecise analog circuits and digital decimation filtering[5]. The sigma-delta ADC works on the principle of sigma-delta modulation. The sigma-delta modulation is a process for encoding high-resolution signals into lower resolution signals using pulse-density modulation. it samples the input signal at a rate much higher than the Nyquist rate. A sigma-delta ADC consists of an analog block of modulator and a digital block of decimator. The modulator samples the input signal at an oversampling rate, generating a one bit output stream and decimator is a digital filter or down sampler where the actual digital signal processing is done[6].

2. Sigma-Delta A/D Converter

Fig.1 shows the block diagram of a Sigma-Delta A/D converter. It consists of a sigma-delta modulator and a decimation filter. The modulator can be realized using analog technique to produce a single bit stream and a digital Decimation filter to achieve a multi bit digital output thus completing the process of analog to digital conversion[4,6].

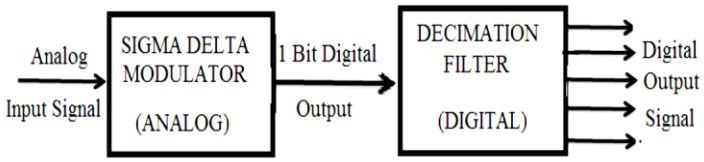


Figure (1): Block Diagram of Sigma delta A/D converter [4].

2.1 Sigma-Delta Modulator

The first order Sigma-Delta modulator consists of an analog difference node, an integrator, a 1- bit quantizer (A/D converter) and a 1-bit D/A converter in a feed-back structure. The modulator output has only 1-bit (two levels) of information, i.e., 1 or -1. Fig. 2 shows first order Sigma-Delta modulator [7].

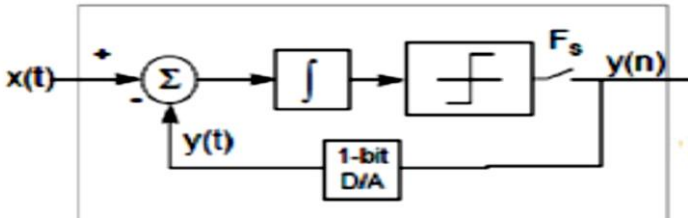


Figure (2): First Order Sigma-Delta Modulator[7].

The relation between the input and output in the discrete time is shown as :

$$Y(z) = X(z) + (1- z^{-1})\, Q(z) \quad (1)$$

The error introduced from the quantizer is pushed to the high frequency terms due to the term $(1-z^{-1})$ [8]. The key equations can be given by [9] :

$$\frac{Y(z)}{Q(z)} = 1- z^{-1} \quad (2)$$

Where $z = e^{j2\pi f T_{ck}}$, then

$$\frac{Y(z)}{Q(z)} = (1 - e^{-j2\pi f T_{ck}}) \quad (3)$$

Hence the noise shaping function is written as:

$$S_y(f) = 2\, S_q(f)\, |1 - \cos(2\pi f T_{ck})| \quad (4)$$

Where:
T_{ck}: is the clock frequency of Sigma-Delta modulator
fs = $\frac{1}{T_{ck}}$ (sampling frequency of Sigma-Delta modulator)
Where $S_q(f)$ is relatively flat for the low frequencies.
Fig. 3 shows the spectrum of a first order Sigma-Delta noise shaping.

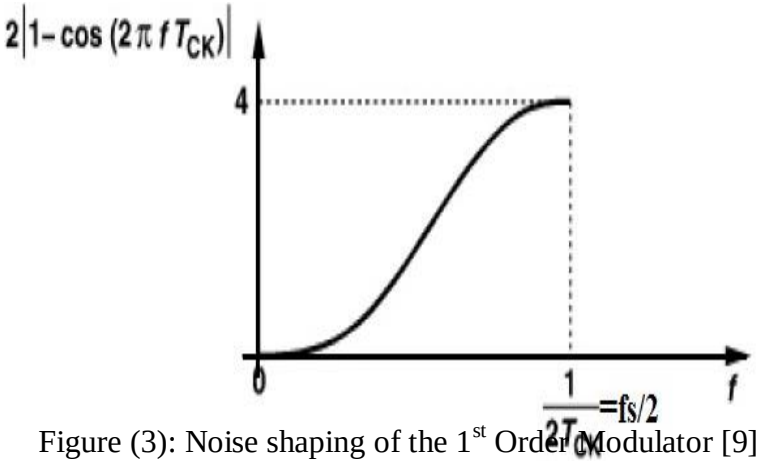


Figure (3): Noise shaping of the 1st Order Modulator [9].

The sigma-delta modulator suffers from high quantization noise at high frequencies. To achieve high resolution, this quantization noise must be removed, and decimate or reduce the sample rate of the Sigma-Delta modulator output to the Nyquist rate which minimizes the amount of information for subsequent transmission, storage or digital signal processing [10].

2.2 Digital Filtering

The basic aim of the digital filter is to remove the quantization Noise at high frequencies due to using of sigma-delta modulator , reduce the sample rate of the Sigma-Delta modulator output to the Nyquist rate and increase the 1-bit or several-bit data word to high-resolution sample word. Practically it is impossible to implement a single filter that would meet the characteristic of decimation filter, because the order of such filters would be very high [11]. So it is necessary to divide the architecture of decimation filter into two parts: Cascaded integrator-comb (CIC) and FIR filters**.** The CIC filter is a combination of digital integrator and digital differentiator stages which execute the operation of digital low pass filtering and decimation. The CIC filter is a multiplier free filter that can accepts large rate changes. The CIC filter first performs the averaging process then follows it with the decimation. A simple block diagram of a first order CIC filter is shown in Fig. 4[12].

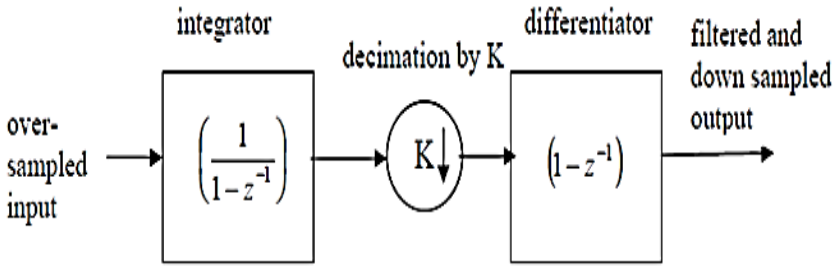


Figure (4): Block Diagram of CIC filter[12].

The integrator works at the sampling clock frequency, (f_s)while the differentiator works at down sampled clock frequency of (f_s/K). By operating the differentiator at lower frequencies, a saving in the power consumption is achieved. Eq.(5) gives the magnitude response of a CIC filter at frequency,(f) where (N) is the order of the filter[13].

$$|H(f)| = \left| \frac{Sin(\pi M f)}{Sin(\frac{\pi f}{K})} \right|^{N} \qquad (5)$$

Fig.5 shows the frequency response of the CIC filter found using Eq. (5). The aliasing bands $2f_c$ centered around multiples of the low sampling rate. As the number of stages in a CIC filter is increased, the frequency response has a smaller flat pass band . To overcome the magnitude droop, an FIR filter can be applied to achieve frequency response correction. Such filters are called “compensation filters" [13].

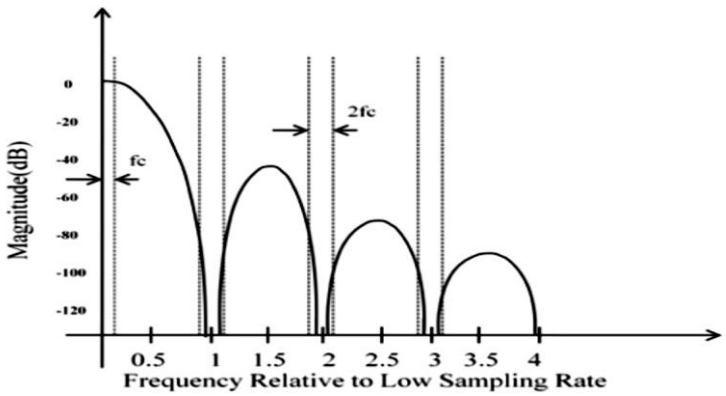


Figure (5): Frequency response of a CIC filter[13].

3. Design And Simulation Methods

The proposed Sigma-Delta ADC used in this paper is shown in Fig.6 which consists of a sigma delta modulator followed by a Decimation Filter which is designed in MATLAB Simulink.

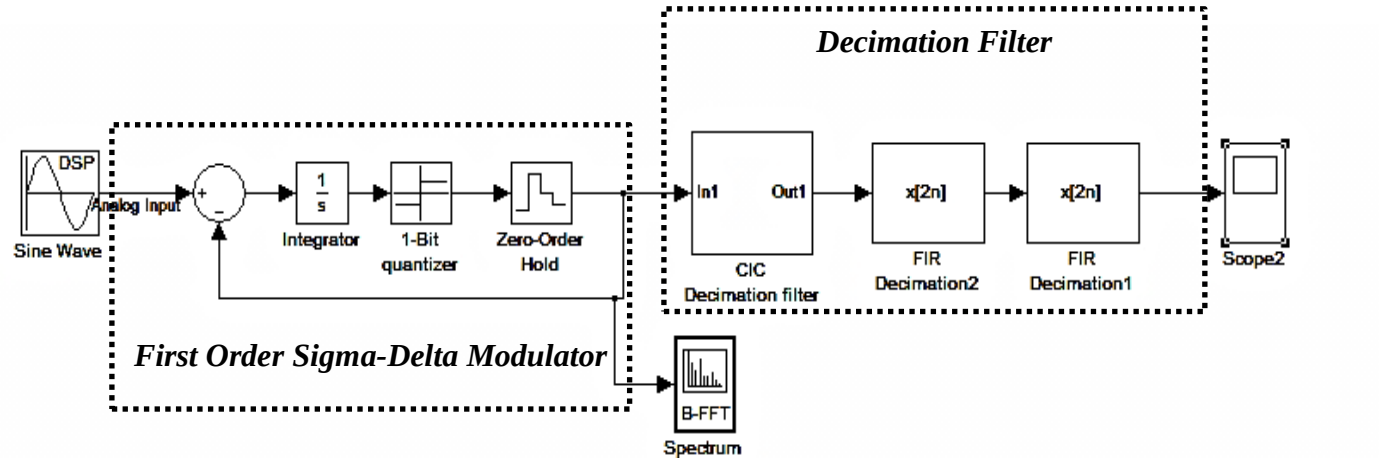


Figure (6): MATLAB model of the Sigma-Delta ADC.

The characteristics of the proposed Sigma-Delta ADC is shown in Table 1. A 15 bit Sigma-Delta ADC for a signal band of 40K Hz is designed in MATLAB Simulink and then the decimation filter has been designed using Xilinx system generator tool , which reduces the design cycle by directly generating efficient VHDL code .The VHDL code has been implemented on a Spartan 3E FPGA using ISE 14.1 tool.

Table (1): The characteristics of Sigma-Delta ADC

Parameters	Symbol	Value
Signal bandwidth	BW	40 KHz
Sampling Frequency	F_S	40,96 MHz
Over Sampling Ratio	K	512
Modulator order	M	1
Number of bits in modulator bit stream	B_{Mod}	1
Number of bits in output of filter	B	15

The Simulink Model of first order Sigma Delta Modulator is shown in Fig.7. It consists of a difference operator, integrator, 1-bit quantizer, and a negative feedback.

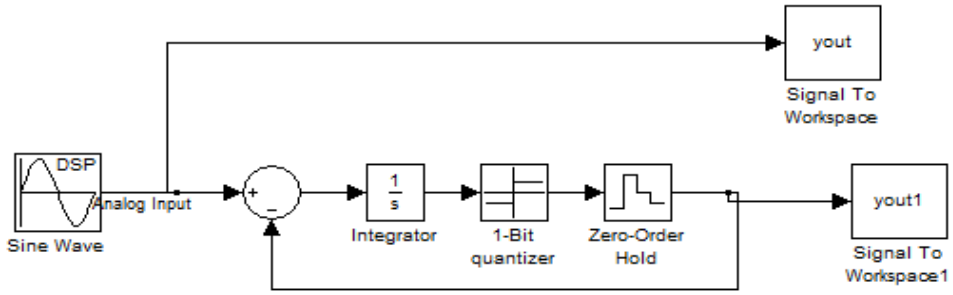


Figure (7): MATLAB model of First Order Sigma-Delta Modulator.

The modulator achieves a SNR of 67.1 dB for a signal bandwidth of 40 KHz. The modulator operates with an oversampling ratio (OSR) of 512 and a sampling frequency of 40.96 MHz .

In order to remove the high quantization noise at high frequencies, the sample rate of the output of the Sigma-Delta modulator must be reduced to the Nyquist rate and to achieve high resolution the decimation filter should have the characteristics shown in table 2.

Table (2): decimation filter characteristics

Filter parameters	Value
Sampling frequency	Fs = 40.96 MHz
Down Sampling Ratio	DSR = 512
Pass band frequency	Fpass = 40 KHz
Stop band frequency	Fstop = 41.6 KHz

The decimation filter accepts the single bit stream from the modulator and converts it into a 15 bit digital output . Practically it is not possible to implement a single filter that would meet the characteristics of Table 2. The order of such filter would be close to 5000. It is difficult to implement such a hardware filter . Therefore, it is needed to use a multi-stage approach, whereby the decimation is performed in several stages. The proposed decimation filter architecture is consist of three stages Second-order Cascaded Integrator Comb filter followed by two (FIR) filters, as shown in Fig.8.

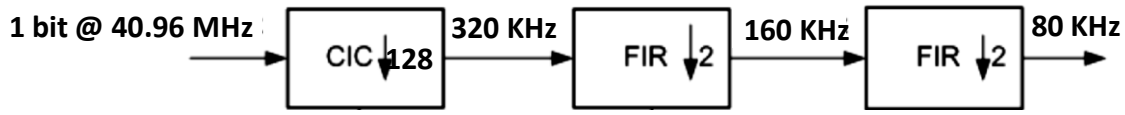


Figure (8): Decimation filter architecture.

The multistage architecture allows most of the filter hardware to operate at a lower clock frequency, and have lower hardware complexity when compared to a single state decimator. The frequency response of a Second order Cascaded Integrator Comb filter is shown in Fig.9.

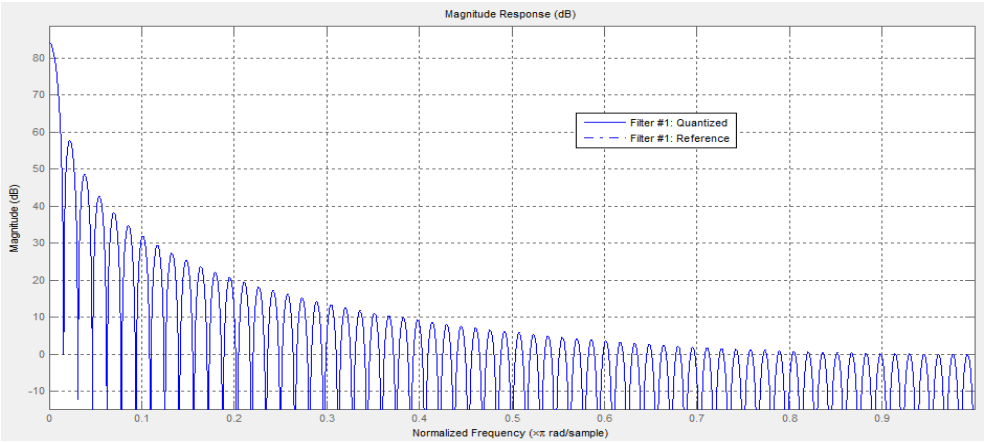


Figure (9): Frequency response of a Second order CIC filter.

The input to the Cascaded Integrator Comb (CIC) filter is a 1-bit pulse density modulated signal from a first order sigma-delta modulator. Internal word width (W) for this design of CIC filter need to ensure that there is no run time overflow given by Eq.6 [4].

W=(1Sign bit)+(Number of input bits)+(Number of stages, N) log2(Decimator factor) (6)

In this paper, W = 1 + 1 + 2 log2(128) i.e. W=16

The output from the Cascaded Integrator Comb (CIC) filter is a (1 sign bit +15 resolution bits) digital output. To overcome the magnitude droop in Cascaded Integrator Comb (CIC) filter, two FIR filters has been used to achieve frequency response correction. The order of the designed FIR filters is 18 and 150 respectively. Fig.10 shows the frequency response of the designed FIR filters.

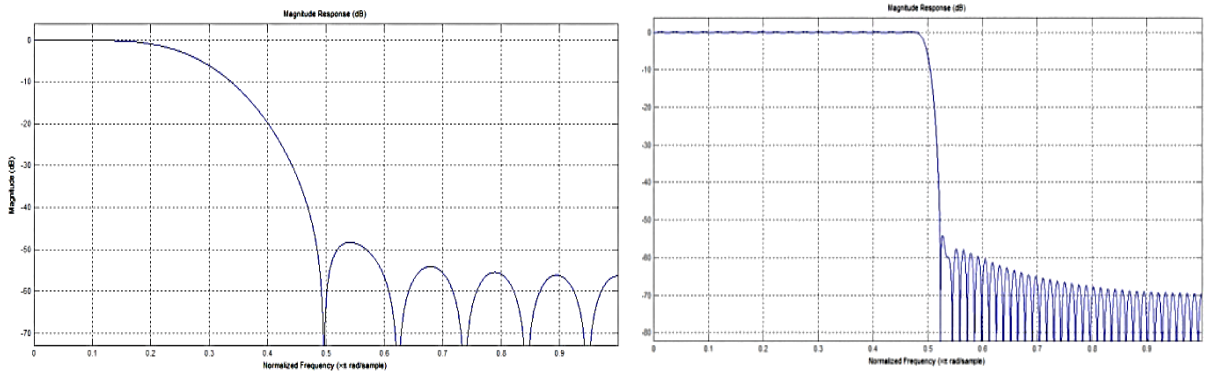


Figure (10): Frequency response of first and second FIR filter.

For the first-order over sampled sigma-delta modulator and the second-order CIC filter used in the design, the desired output resolution is given by Eq. (7)[7].

$$N_{final} = N_{i/p} + \frac{30\log K - 5.17}{6.02} \qquad (7)$$

Where :

N_{final} is the final output resolution,

$N_{i/p}$ is the input resolution of the decimator.

So, for *K=512*, the output resolution achieved is 15 bits.

The proposed decimation filter has been designed using MATLAB Xilinx system generator tool , which reduces the design cycle by directly generating efficient VHDL code. Figure 11 shows the decimation filter designed in system generator. The VHDL code has been implemented on a Spartan FPGA using ISE 14.1 tool.

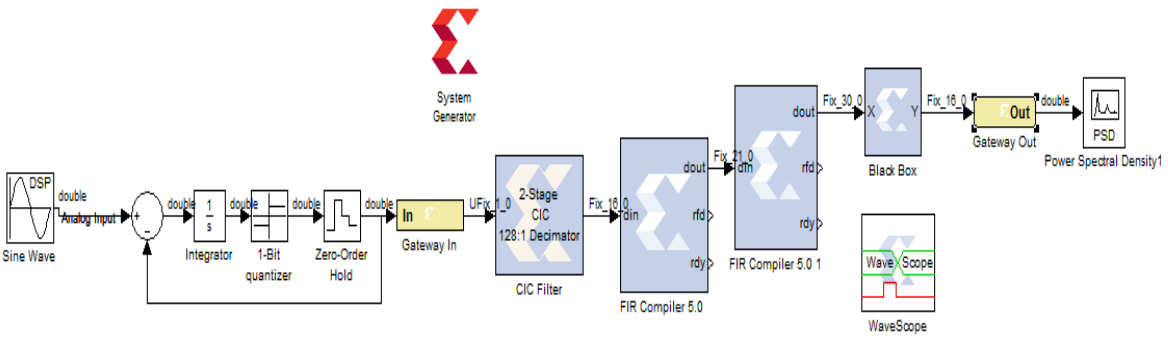


Figure (11): Decimation filter designed in system generator

4. Results And Discussion

The output of first order Sigma-Delta modulator with a sampling frequency of 40.96 MHz for a sine wave input of 1 Vpp and 20 KHz is shown in Fig.12.

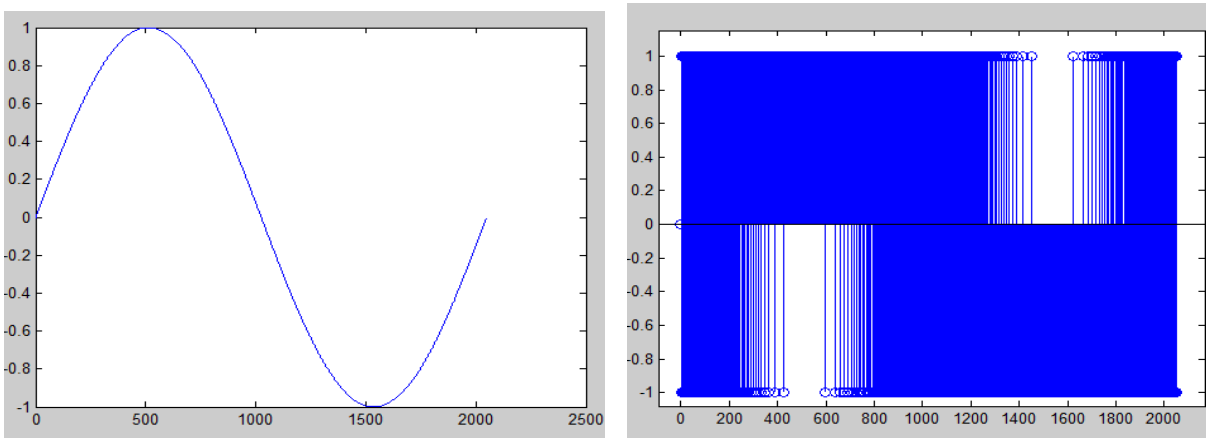


Figure (12): Transient response of first order Sigma-Delta modulator for a sine wave input of 20 KHz.

It is a clear evident that the output (single bit) is a pulse width modulated in accordance with input sine wave. The number of 1's increases at the positive peak of the input sine wave and the number of -1's are more at the negative peak. There are equal number of 1's and -1's when the input signal is at zero amplitude, which is the expected response of a Sigma Delta Modulator.

Fig.13 shows the simulated power spectral density (PSD) of the proposed Delta Sigma modulator for a 20 KHz input sine wave.

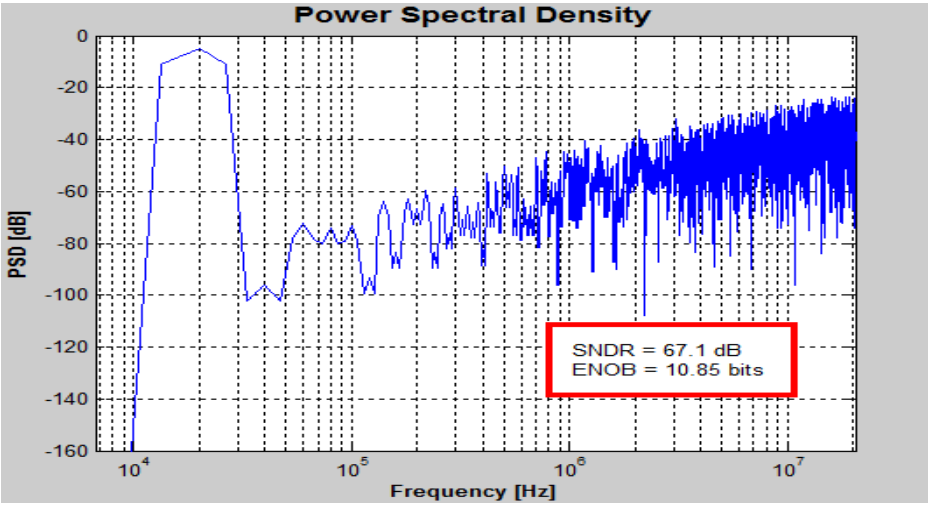


Figure (13): Power Spectral Density (PSD) of output of Sigma-Delta modulator.

As shown in Fig.13 the quantization noise shifted towards high frequency band. The modulator signal to noise ratio (SNR) was designed to be 67.1 dB for first-order output with an OSR of 512.

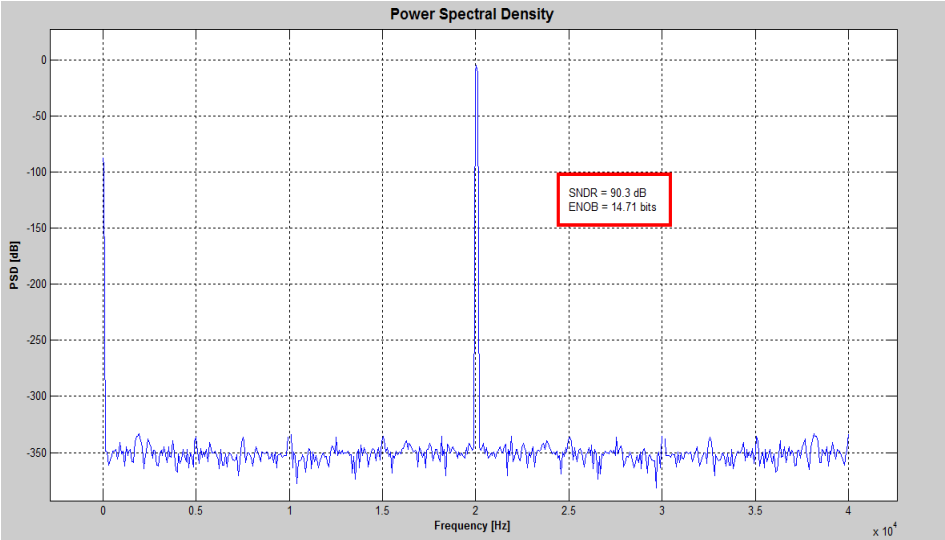


Figure (14): Power Spectral Density (PSD) of Output of decimation filter.

Fig.14 shows the output spectrum of the decimation filter, it is clear that the decimation filter is able to remove the out-of-band noise effectively and increases the SNR. The complete ADC is able to achieve a resolution of 14.71 bits and SNR of 90.3 dB .

The output Power Spectral Density (PSD) of the decimation filter using Xilinx system generator tool was exactly the same as the result in MATLAB Simulink as shown in Fig.14. Fig.15 shows the digital output from decimation filter for 20 KHz analog signal.

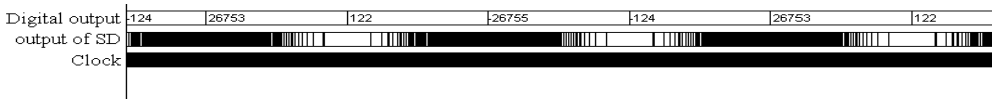
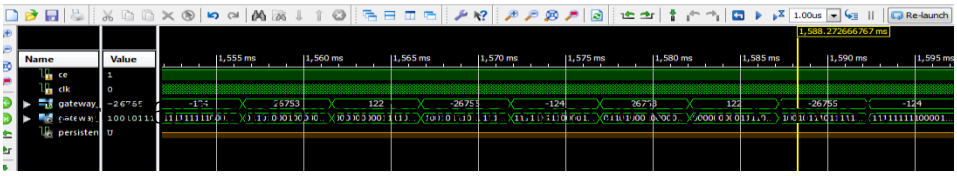


Figure (15): digital output for analog signal 20 KHz.

To implement the decimation filter in Spartan 3E the efficient VHDL code was directly generated from the design of the decimation filter in Xilinx system generator. Using Xilinx ISE to simulate the VHDL code generated from system generator ,the result of digital output from decimation filter for 20 KHz analog signal in Xilinx ISE simulation is shown in Fig.16.



The result of Xilinx ISE simulation was exactly the same as the result from MATLAB Simulink. Table 2 shows a summary of the resources utilized in the implementation of the decimation filter in Spartan 3E.

Table (2): Resource Utilization for Spartan 3E

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	759	9,312	8%	
Number of 4 input LUTs	520	9,312	5%	
Number of occupied Slices	454	4,656	9%	
Number of Slices containing only related logic	454	454	100%	
Number of Slices containing unrelated logic	0	454	0%	
Total Number of 4 input LUTs	592	9,312	6%	
Number used as logic	399			
Number used as a route-thru	72			
Number used as Shift registers	121			
Number of bonded IOBs	16	232	6%	
Number of RAMB16s	3	20	15%	
Number of BUFGMUXs	1	24	4%	
Number of MULT18X18SIOs	3	20	15%	
Average Fanout of Non-Clock Nets	2.21			

The decimation filter performance has been ascertained using the hardware co-simulation that uses Chipscope Pro Analyzer in ISE. The digital output result from implementing the decimation filter in Spartan 3E by using the chipscope for 20 KHz analog signal is shown in figure 17.

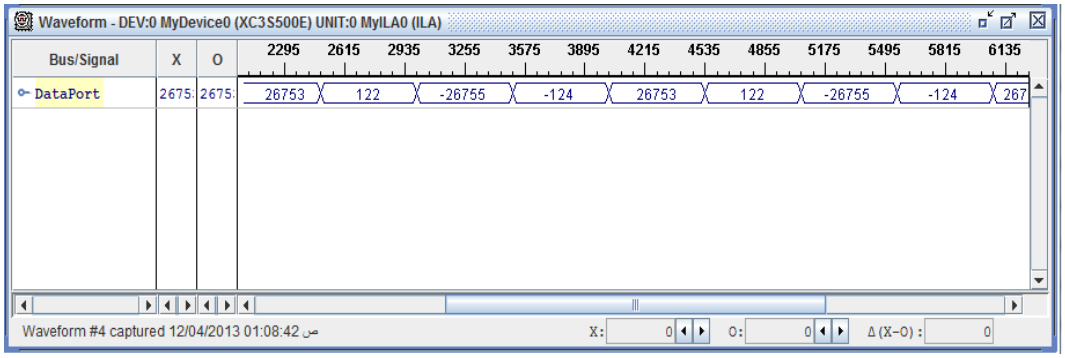


Figure (17): Result of implementation the decimation filter in Spartan 3E.

By comparing digital signal obtained using chipscope with the digital signal obtained using MATLAB Simulink, it can be seen that the two digital signals are very similar and this mean that generation and implementation of the VHDL code in Spartan 3E is performed without any error.

Because of similarity in time domain between two digital signals of simulation and implementation that shown in Figs(15),(17), it can be assumed that the output spectrum of implementing the decimation filter is the same as the simulated output spectrum.

5. Conclusion

A complete sigma delta ADC is designed using a first order Sigma-Delta modulator and a Digital decimation filter with an OSR of 512. The multistage architecture reduces the need for multiplication which needs very large area to implement in hardware and allows most of the filter hardware to operate at a lower clock frequency which have lower hardware

complexity when compared to a single state decimation filter . Digital decimation filter for Sigma Delta ADC is successfully implemented into Xilinx Spartan series FPGA. This ADC gives overall 15 bits resolution and SNR of 90.3 dB.

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Performance of Power-line Communications (PLC) In ALaboratory

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Abstract

Power line networkshave been proofed as a powerful, cheap, and suitable medium to deliver not only electricity or control signals, but also data and multimedia contents, as they use the available AC electrical wiring.This is easier than trying to run new wires, more secure,relatively inexpensive, and more reliable than radio wireless electrical wiring like 802.11b. In this contribution, the influence of electrical cable characteristics on the channel transfer function under various loading, and tabbing conditions are investigated by computer simulations using the ABCD matrix formulation. The performance of various coupling and filtering circuits were studied by simulation and experimental measurements. Further more practical measurements were performed on the electrical wiring in a typical laboratory to examine the performance of a simple PLC communication system, where bit error rate (BER) tests were also made.

تقييم أداء نظام اتصالات عبر خطوط القدرة (PLC) في مختبر

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الخلاصة

لقد أثبتت شبكة القدرة الكهربائية أنها وسط فعال لنقل ليس فقط التيار الكهربائي وإشارات السيطرة بل المعلومات والبيانات المتعددة. من فوائد استخدام شبكة نقل القدرة كوسط لنقل البيانات (PLC) هو أنها متوفرة أصلا في الأبنية حيث تتواجد مآخذ للقدرة. وهكذا فان استخدامها سيكون أسهل وأقل كلفة بالمقارنة مع تنصيب شبكة جديدة، فضلا عن أنه أكثر ضمانا من الشبكة اللاسلكية. يهدف هذا البحث الى دراسة تأثير خواص كابلات القدرة الكهربائية على قناة منظومة (PLC) تحت تأثير أحمال وتوصيلات مختلفة، باستخدام أسلوب خط النقل و (ABCD) ماتركس. تم تحليل مختلف عناصر منظومة الاتصال مثل دائرة الاقتران والترشيح، نظريا وبالمحاكاة على الحاسبة. كذلك تم اختبار بعض دوائر ومكونات المنظومة عمليا فضلا عن إجراء قياسات معدل الخطأ (BER) في تجربة اتصال داخل احد المختبرات الجامعية.

1-Introduction

During the last few decades the power line carrier (PLC) communication systems have being providing communication,at low bandwidth, for residential and commercial applications, through low and high voltage power lines. The modern networking technologies and office monitoring and automation, have led to an increasing need to provide solutions and improve services to the consumers at lower cost and better performance. The advantage of using (PLC) as a transmission channel is that the existing electrical wiring in a building can provide high speed network access points almost anywhere there is AC power outlet. Thus using the existing AC networks can offer fast, more secure, relatively inexpensive, and more reliable way compared to radio wireless like 802.11b.For most small office, and home applications, this is an excellent solution to the networking problems [1-5]. The PLC is hoped to become the standard internet access worldwide especially for 3rd world countries and for rural areas in modern countries where fiber-optics and DSL lines are not available [2].

Recently serious attention has been given to PLC for the purpose of communication and data networking. Performance of OFDM, multiuser, and embedded systems were investigated in PLC environments [6-9].Apart to the 2-way communication signal transfer, transmission of control signals in hotel[10], and buildings monitoring and automation systemshas been an active research interest recently[11].The investigations related to PLC systems have considered either the performance of various data transfer techniques [6-11], or the characteristics of the PLC network (as a channel) across the frequency band required by recent applications[1-3],[5]. Other researchers have considered the performance of the coupling circuit [12]. In [1,2], a multi-branch power line communicationchannel is modeled using ABCD matrix. The effects of multiple loads,multipath and mismatching were also investigated. The channel transfer function was investigated under various power line network conditions.

This contribution aims to study the capability of using the established electric power installation in a university laboratoryto communicate useful data. The PLC channel is analyzed theoretically and the performances of its various parts are studied by computer simulations. Further more practical measurements of some devices and circuits of the system as well as bit error rate (BER) tests for communication in a typical laboratorywere made.

2-Analysis of simple power line model:

A multi-branch PLC channel can be modeled as number of transmission line sections connected together. These sections orcells are formed of a 2-port network as shown in Fig. 1.The ABCD matrix formulation is used here for the analysis, where input current I_1, input voltage V_1, output current I_2 and output voltage V_2 can be related by the following [13]:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \quad (1)$$

The ABCD matrix of a cableof length l, characteristic impedance Z_0 and propagation constant γ is given as[13]:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh(\gamma l) & Z_0 \sinh(\gamma l) \\ \sinh(\gamma l)/Z_0 & \cosh(\gamma l) \end{bmatrix} \quad (2)$$

The input impedance, (V_1/I_1) is given by [1,2,13]:

$$Z_{in}=\frac{A Z_L+B}{C Z_L+D} \quad (3)$$

The transfer function is the ratio of the output to the input (V_2/V_1)[1,2,13]:

$$H=\frac{Z_L}{A Z_L+B+C Z_L Z_s+D Z_s} \quad (4)$$

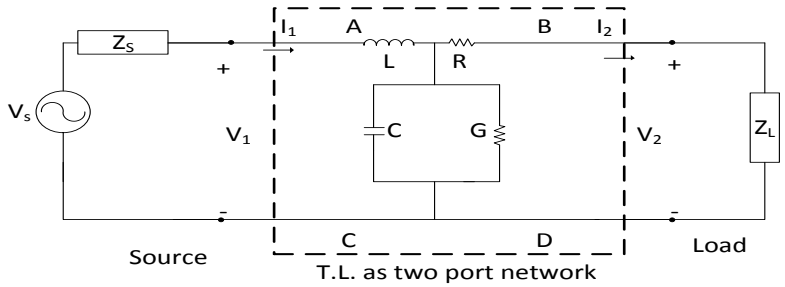


Figure (1):Modeling the PLC channel using transmission line model.

As the A, B, C and D parameters of a power line network are frequency dependent, then the input impedance, and transfer function will be also frequency dependent, and consequently influence the usable bandwidth. With the knowledge of the per-unit length parameters (R, L, C, and G) of the wiring line, and the ABCD matrix, it is easy to compute the transfer function of the PLC channel using Eqs. 1-4.

In practice, PLCnetwork usually have cables withmany tabs (branches)of different lengths and cable types, as necessitated by wiring requirements in the building. In such case, the chain rule, which involves multiplying the ABCD matrices of the serially connected sections, is used to determine the overall matrix. Aseries impedance has ABCD [1,2,13]:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & Z_s \\ 0 & 1 \end{bmatrix} \quad (5)$$

While that for a load impedance Z_p connected in parallel is:

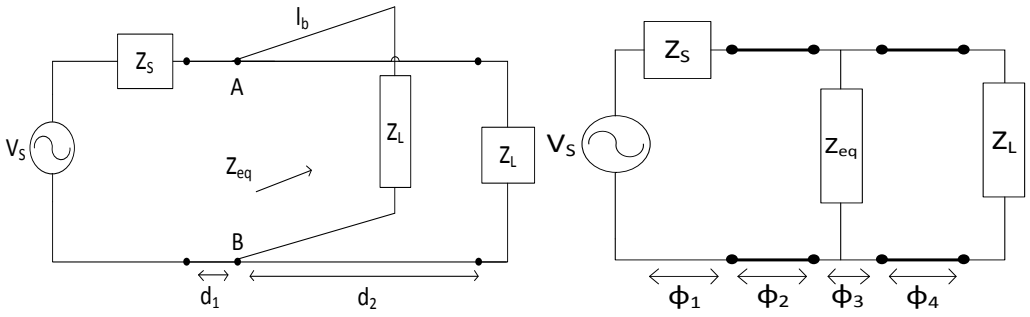
$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 1/Z_p & 1 \end{bmatrix} \quad (6)$$

A tabbing branch terminated with load impedance Z, as shown in Fig. 2, can be considered as a stub whose equivalent input impedance Z_{eq} is [13]:

$$Z_{eq}=Z_0\frac{Z+Z_0\tanh(\gamma_b l_b)}{Z_0+Z\tanh(\gamma_b l_b)} \quad (7)$$

Where Z_0 and γ_b are the characteristic impedance and the propagation constant of a branch of length l_b circuit respectively.

The network of Fig. (2-b*)* can be partitioned into four cascaded sections; Φ_1, Φ_2, Φ_3 and Φ_4. Thus the ABCD matrix for the transfer function can be calculated following the same procedure described in [1,2]. The characteristic impedances and propagation constants for



-a- -b-

Figure (2): Transmission line with a tapping branch (a), and its model (b).

the shown cable sections are used to find the values of the ABCD matrix, and then the transfer function of the PLC can be computed easily. However, as the number of sections increases, more complexity of the formulae andincreased time for calculations are faced. The performance of the various parts of the PLC channel are investigated for many cases of various cable lengths and types, certain number of branches, and loadingconditions, as shown in the following section.

3-Study of Sample Cases

The power line network is investigated here as a communication channel consisting of pieces of wires represented by transmission line circuits. Two types of cables, having the following parameters are consideredhere in the modeling of the PLC channel:

Cable type-1: R=1.9884Ω/m, G=0.01686nS/m, C=0.13394nF/m, L=362.81nH/m. This type of cable was used in [2].

Cable type-2: G=0.016 nS/m, C=0.15 nF/m, L=380 nH/m. The resistance/unit length (R)was given various values as depicted in the simulation results, in order to assess the effect of cable loss on the performance of the PLC channel. However, in [2] the loss effect was not investigated.

The channel models weresimulated using MATLAB software to calculate the channel performance using cable parameters and equations in section 2.The studied cases aredescribed in the following:

3.1 Case 1 (cable feeding a load):This simple case is a piece of cable connectinga voltage source and load as shown in Fig. (3-a). The calculated transfer functions for two types of loads, usinga 20m long cable of type-2areshown in Figs. (3-b& 3-c). It can be noticed from Fig. (3-b) that the frequency response has two regions; a low frequency region where the gain (transfer function magnitude) remains constant followed by high frequency region where the gain drops sharply. As the resistance R (or losses) decreases the cutoff frequency increases. Oscillations are observed for lower values of the resistance. However, Fig. (3-c) shows no oscillation since the line is matched to the load. The drop in gain is caused by the losses in the cable, which are higher for larger values of the resistance R, and higher frequencies.

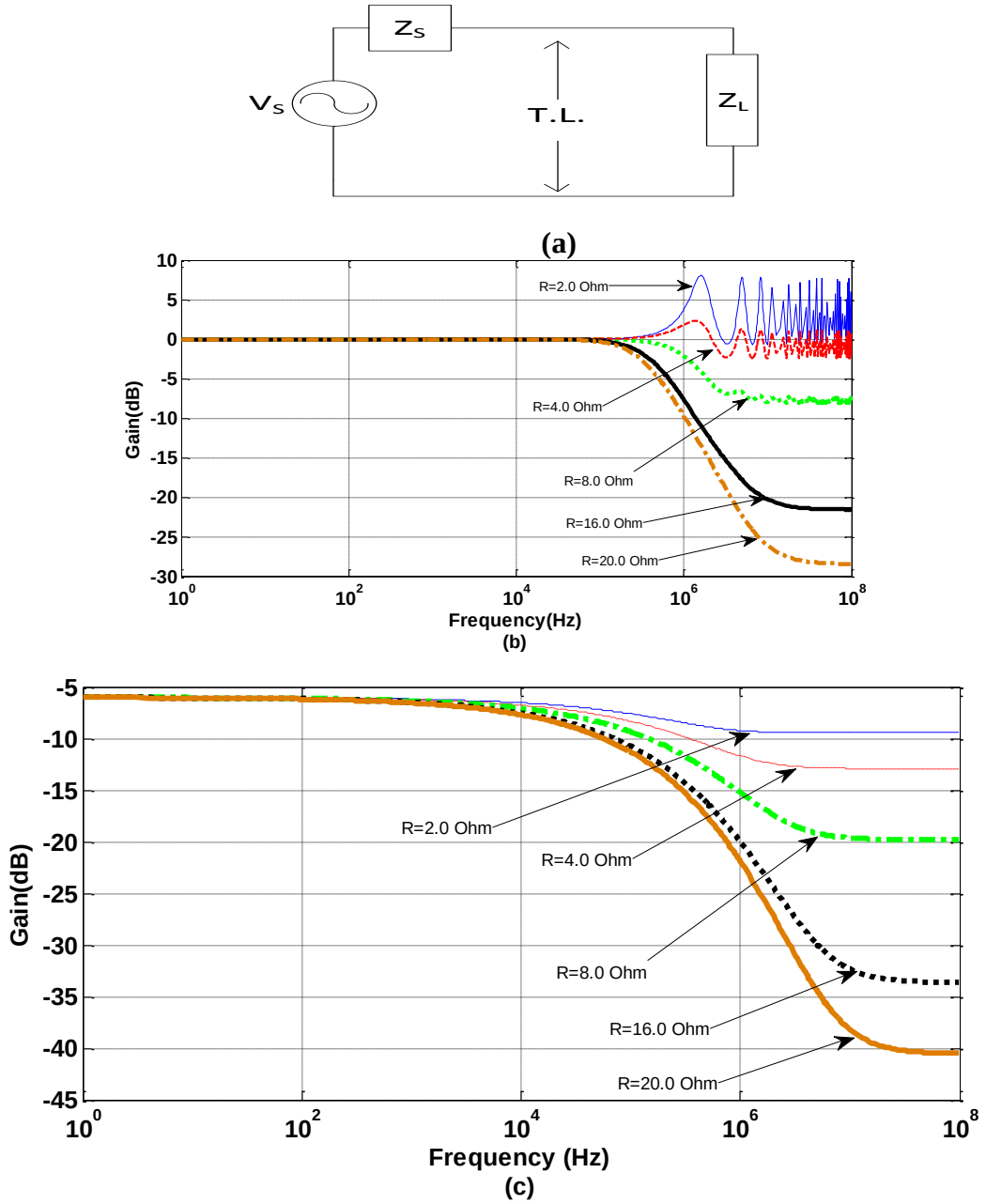


Figure (3): (a) Simple PLC channel as a transmission line circuit. (b) Transfer function magnitude (gain) of circuit-1 with length=20m, Zs=0 & $Z_L=\infty$, using cable type-2 with indicated values of resistance/m, (c) Transfer function magnitude of circuit1 with cable length=20m, Zs= Z_L =Z_0, using cable type-2 with indicated values of resistance/m.

Further study of the transfer function was performed to show the effect of varying the cable length, at various frequencies. The obtained results are shown Fig. (4). The general trend is a drop in gain as the length of the cable is increased. When the cable is unmatched, ripples are noticed in the gain as seen in Fig. (4-a) and Fig. (4-c). Figures (4-b) and Fig. (4-d) also show that the losses increaseas a function of cable length for matched cable.
Figure (5) shows the performance of the transfer function at higher frequencies. As frequency increases, the gain of the unmatched cable shows single resonance, as seen in Fig.(5-a), and multi resonances at higher freqency as clearly seen in Fig. (5-c). The losses

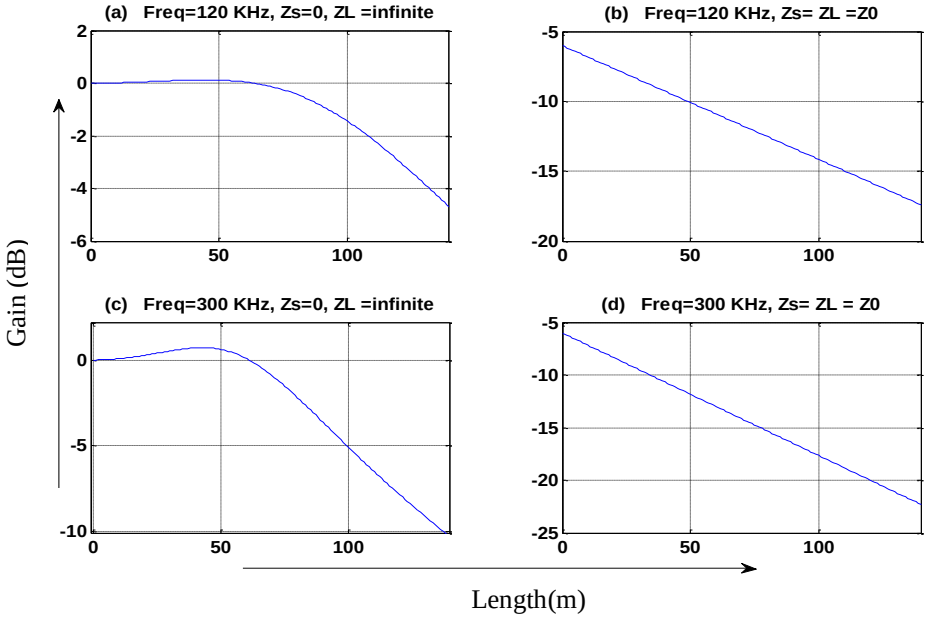


Figure (4): [illegible] versus cable length (m) at lower frequencies, using cable type-1

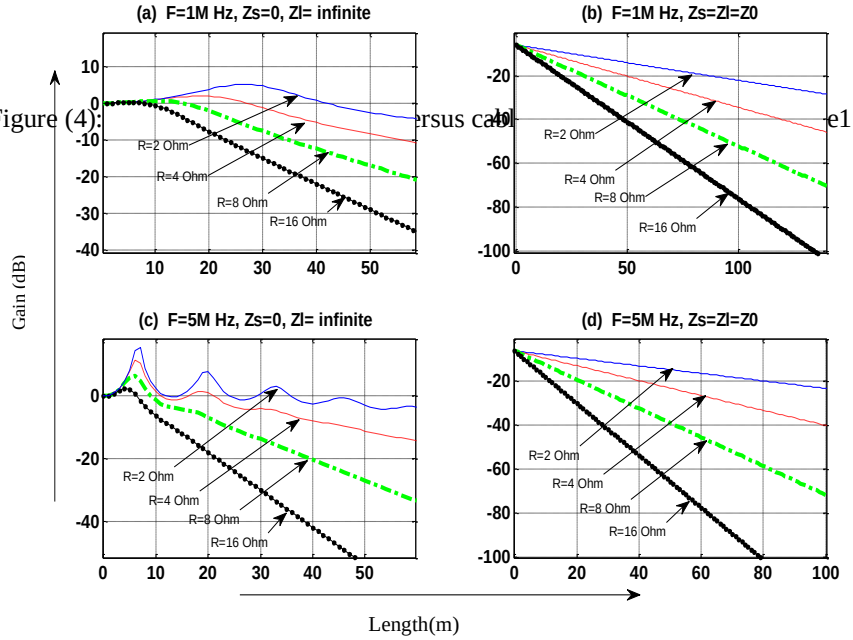


Figure (5): The variation of gain (dB) versus cable length (m) at higher frequencies, using cable type-2 having the indicated values of resistance/m.

also increased as frequency increased as exhibited by the increased slope of the gain as shown in Fig.(5-b) and Fig.(5-d). Faster drop in the gain is noticed as the resistance value inceases, as a result of higher losses.

3.2 Case 2 (effect of branching): This circuit represents the case of cable tabbing/branching. The branch, whose length is L_b and terminal load Z_b , divides the cable into two sections of lengths L_1, L_2, as shown in Fig. (6). For various values assigned to the parameters (Z_s, L_1, L_2, L_b., Z_b, Z_L), the effect of the branch (length and termination load) can be found as shown in Figs. (7). This figure show that the gain remains stable approximately up to 1MHz, after that it becomes more sensitive and changes widely with frequency. It can also beseen that, as Z_b decreases, the gain also decreases taking into account L_b =2m. It can also be seen that, as

the termination load becomes smaller, the gain decreases widely with L_b =2m. Figure 8 shows the effect of varying the branch load on the gain of the channel (source-load) for the indicated conditions. The gain shows smaller variation as the branch load increases.

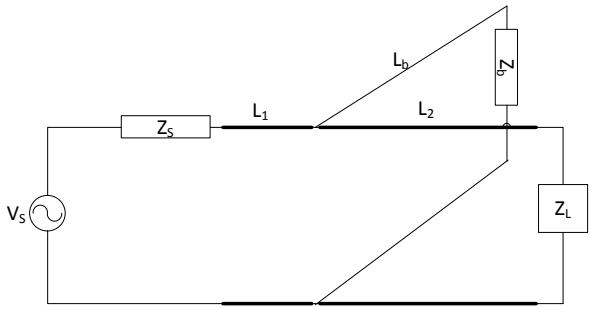


Figure (6):Case-2, a tabbing branch connected totransmission line.

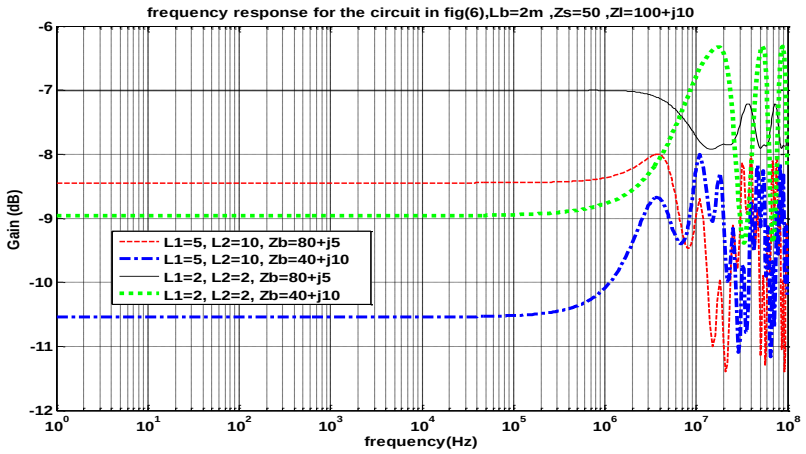


Figure (7): Frequency responses of transmission line with a tabbing branch, using cable type1.

An important question is that "what is the effect of increasing the length of the branch". For this purpose the gain was plotted versus length of the branch with Z_b=0 (the worst case value is for a short circuit), as Fig. (9)shows. It can be seen that, after branch length of 50m the effect of branch is negligible, however for Z_b>0, the above length decreases. The other noticeable result is that as the frequency is increased from1kHz to 1 MHz, the gain decreases.

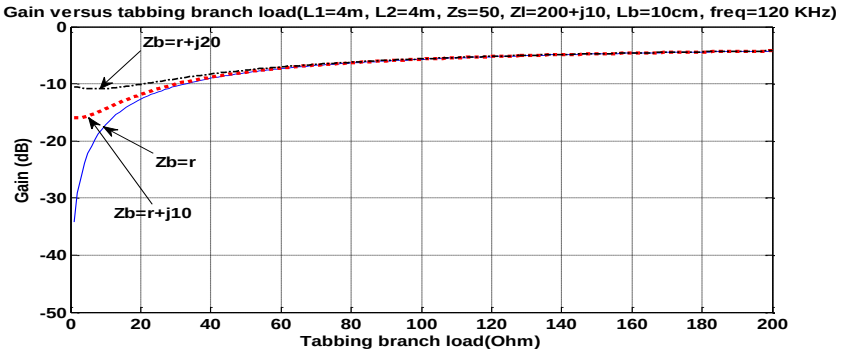


Figure (8): Relation between gain and the tabbing branch load, using cable type1.

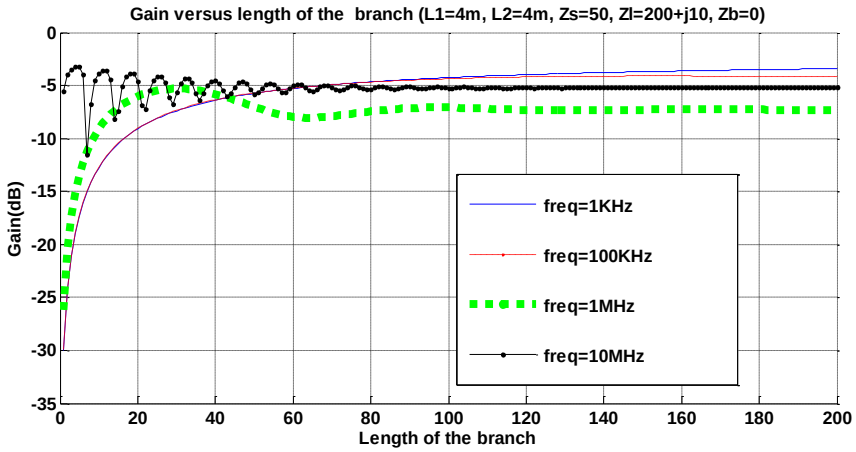


Figure (9): The gain versus length of the branch with Z_b=0 , using cabletype1

3.3 Case-3: This circuit is assumed to represent, as an example, two personal computers (PC) located at two rooms in a building, and it is wanted to connect them using PLC facilities. The equivalent circuit is shown in Fig. 10, where L_i represent pieces of wiring between loads Z_{bi} which are at distances L_{bi} from the transmission line/wire. Two cases are investigated here:

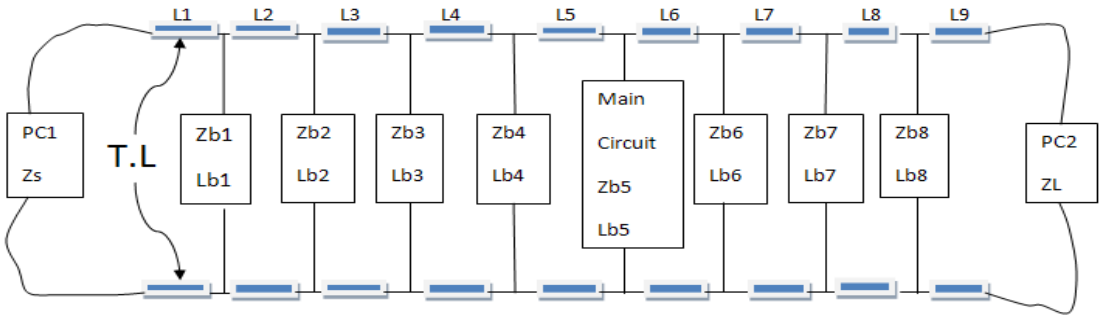


Figure (10): Model for connecting two PC's in two rooms, with PLC system.

In the first case the source and load impedances are assumed as : Z_s=30+j3 Ω, Z_L= (200+j10) Ω, respectively, while the suggested values for lengths and impedances of the cables and branches are listed in table (1). The gain remains stable at low frequencies, while above 100KHz, the gain decreases sharply, and the response can represent a low pass filter LPF as shown in Fig. 11.

Table (1):Values for lengths and impedances of the cables and bridge tabs

Bridge tab.No	Terminated load $Z_{b(\Omega)}$	Bridge tab Length(m)	Cable number	Cable Length(m)
1	100+j10	1	1	**8**
2	100+j10	100	2	0
3	100+j10	100	3	0
4	100+j10	100	4	0
5	5-j2	100	5	0
6	100+j10	100	6	0
7	100+j10	100	7	0
8	100+j10	100	8	0
9	--------	--------	9	0

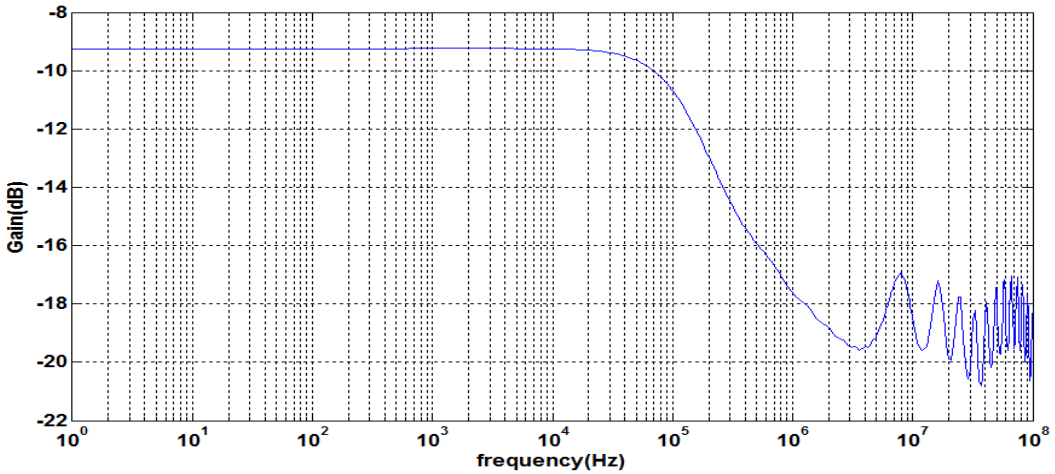


Figure (11): Gain of the transfer function for case-3, for the parameters shown inTable 1, using cable type1.

In the second case the source and load impedances are assumed as; Z_s=30+j3Ω, Z_L= (150-j10) Ω, and the suggested values for lengths and impedances of the cables and branches are listed in Table (2).It can be seen from Fig. (12) that, the losses have increased, in comparison with those shown in Fig. 11, due to increasing the cable resistance. High frequency resonance behavior appeared at some critical frequencies.

Table (2): Values for lengths and impedances of the cables and branches

Bridge tab.No	Terminated load $Z_{b(\Omega)}$	Bridge tab Length(m)	Cable number	Cable Length(m)
1	100+j10	1	1	0.5
2	100−j10	1	2	1
3	100+j10	1	3	0.5
4	100−j10	1	4	1
5	5-j2	10	5	0.5
6	100+j10	1	6	1
7	100−j10	1	7	0.5
8	100+j10	1	8	1
9	--------	--------	9	0.5

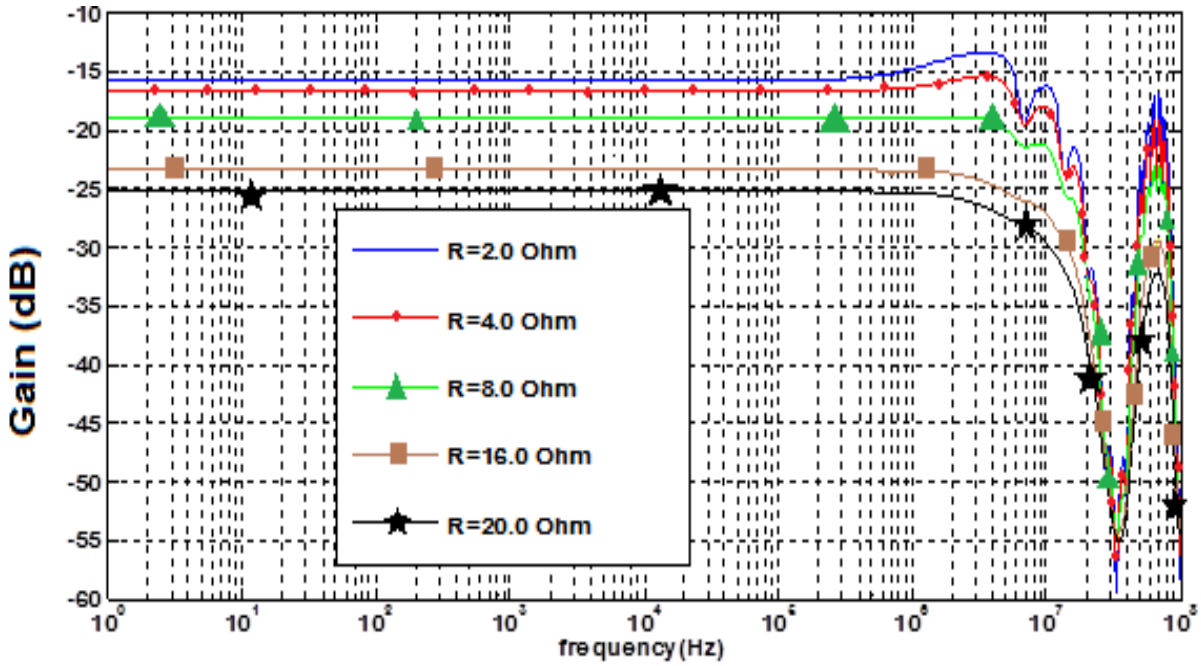


Figure (12):Gain of the transfer function of case-3, using cable type-2, having the indicated values of resistance/m, and cable lengths shown in Table 2

4- The Coupling Circuit

The interface circuit to the power distribution network is a critical part of any (PLC) system. As there are high voltages, different values ofimpedances, high amplitudes and intermittent disturbances, the coupling circuit requirescareful considerationsto achieve acceptable transmission at the required bandwidth, while at the same time insure standard safety level. The PLC systems operate at the two extremesenvironments; very low frequency,with high current and voltage levels of the power signal,and much higher frequencies at very low current and voltage levels in the communication signal. The coupling circuit has to provide adequate isolation of the PLC system from the power wiring system, which can be achieved through inductive or capacitive coupling. Inductive coupling is known to be rather lossy up to several decibels, but it is safer and easier to install. Capacitive coupling, on the other hand, offers the required high-pass filtering and it is easy and compact to design. The two approaches are often integratedto combine their benefits.

A typical coupling circuit can have both coupling capacitors and a coupling transformer as shown in Fig (13)[12].A combination of diodes is used herefor protection from over voltage and spikes.

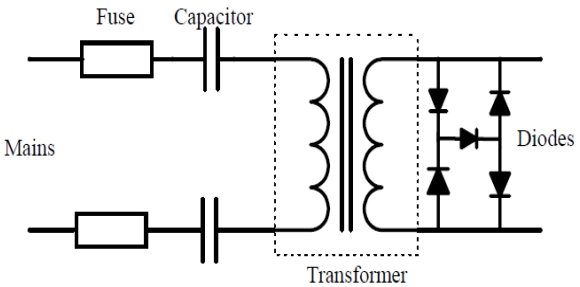


Figure (13): Typical broadband coupling circuit with protection diodes [12].

Inductive coupling circuits inject the PLC signal into the power distribution wiringusing a ferrite transformer. This is desired when the mains impedance is low at the

signal injection point, which occurs when several power branches are connected together. The transformer offersadequate isolation and safety.

The iron core transformer usually operates in the low frequency band for an efficient transfer of power and isolation.A typical transformer of this type was selected for testing, its frequency response was measured, and the obtained result is shown Fig.(14.a) . It can be seen that iron core transformer cannot be used to couple high frequency (above few tens of kHz) signals. The shown voltage gain is due to the transformer turns ratio, which peaks at resonance frequency of about 8.5 kHz.This response shows much lower range compared to the ferrite transformers used in [12].

Ferrite core transformers are widely used at high frequencies. One available transformer was selected for measurements and theobtainedresults are shown in Fig. (14.b). It can be seen from the figure that, the response is rather good at high frequencies in comparison with that of the iron core transformer of Fig. (14.a). For this transformer, signal frequencies of up to few MHz's can be coupled. The gain in the output voltage is due to turns ratio.Two resonances at 0.7 kHz, and 5MHz can be noticed.Although the achieved bandwidth is lower than that obtained in [12], but response here is more flat.

In general, the ferritetransformer is used in series with a capacitor to compensate for its very low input impedance at low frequencies, thus preventinglarge input current that can saturate its BH curve,and may defect its primary coil. Theseries capacitor acts as a high pass filter preventing the 50 Hz mains current.Alternatively a notch filter can be used to decouple the 50 Hz mains voltage. Figure 15 shows typical notch filter and its equivalent circuit.

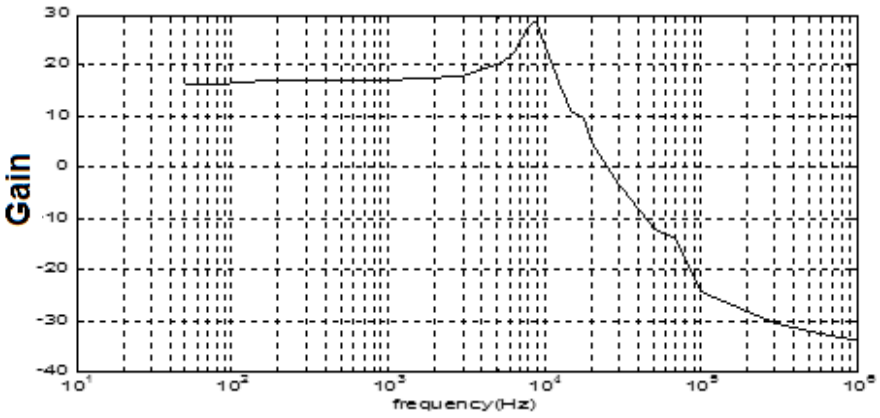


Figure (14.a) Measured frequency response of an iron-core transformer, having turns ratio of (10:1).

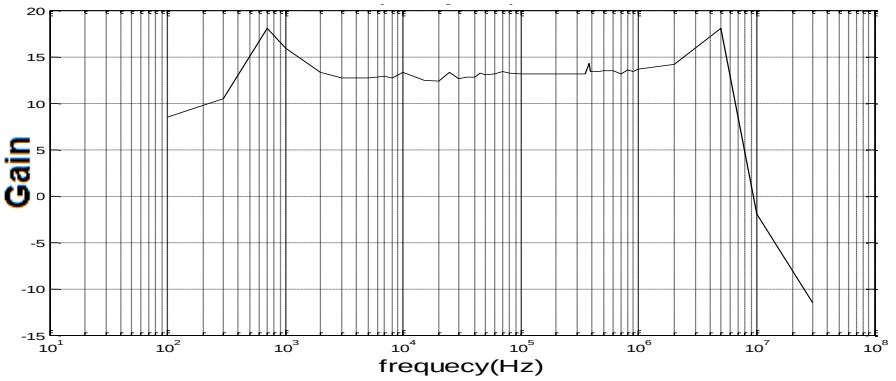


Figure (14.b) Measured frequency response of the used ferrite core transformer, with turns ratio of (5:1).

The calculated transfer function,and input impedance for the filter circuit of Fig. (15)have been plotted as a function of frequency as shown in Figs. (16) and (17).As can be seen the filter can strongly attenuate the 50 Hz signal, while all other frequencies above 1kHz

pass without any appreciable loss. The band reject width is about (285 Hz) and maximum attenuation is about (50 dB). As shown in Fig. (17), the input impedance is constant at about (630Ω) for all frequencies above (100Hz).

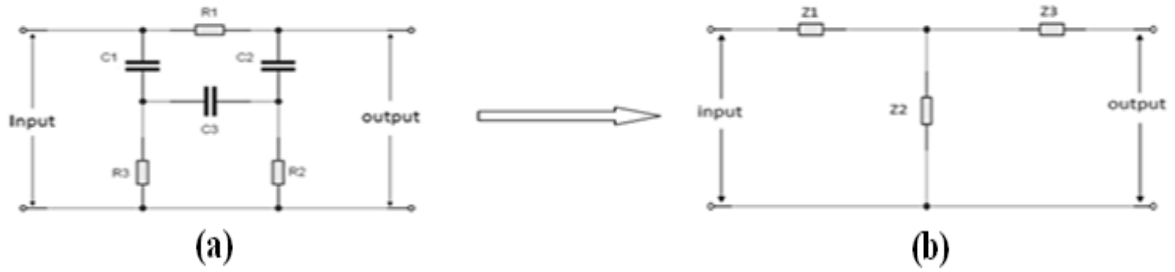


Figure (15) Circuit diagram of the notch filter (a), and itsequivalent circuit(b).

Multistage design of the notch filter gives many advantages.The calculated transfer function and input impedance for the 3-stages are compared to those obtained by single stage as shown in Figs (16) and (17).As noticed from Fig (16) the attenuation is greatly increased and the band of (47 – 52 Hz) is notched by about 80 dB below those above 2 kHz. This is sufficient to reject the 50 Hz signal.For the frequencies above 2 kHz the input impedance for the 3-stage filter is one half that of single stage and equal to (50 Ω).
The following two configurations for the coupling circuit are investigated here;

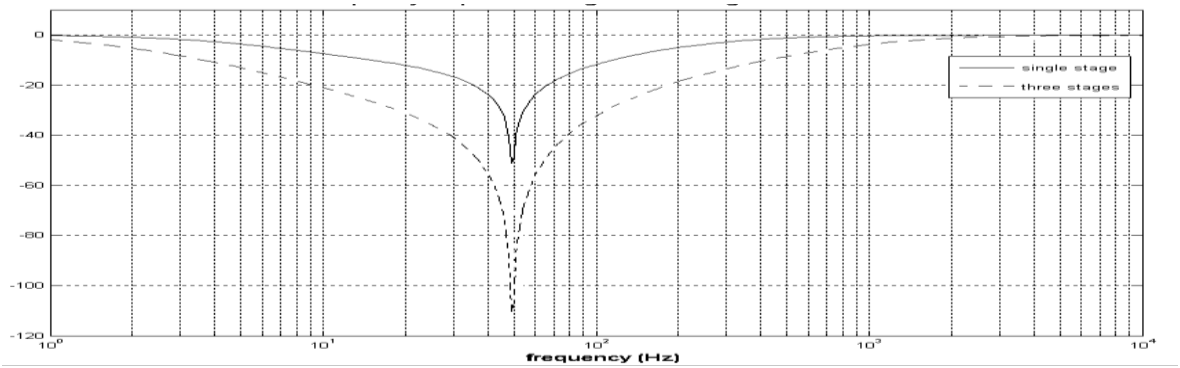


Figure (16): Frequency responses of the single and 3-stages notched filters.

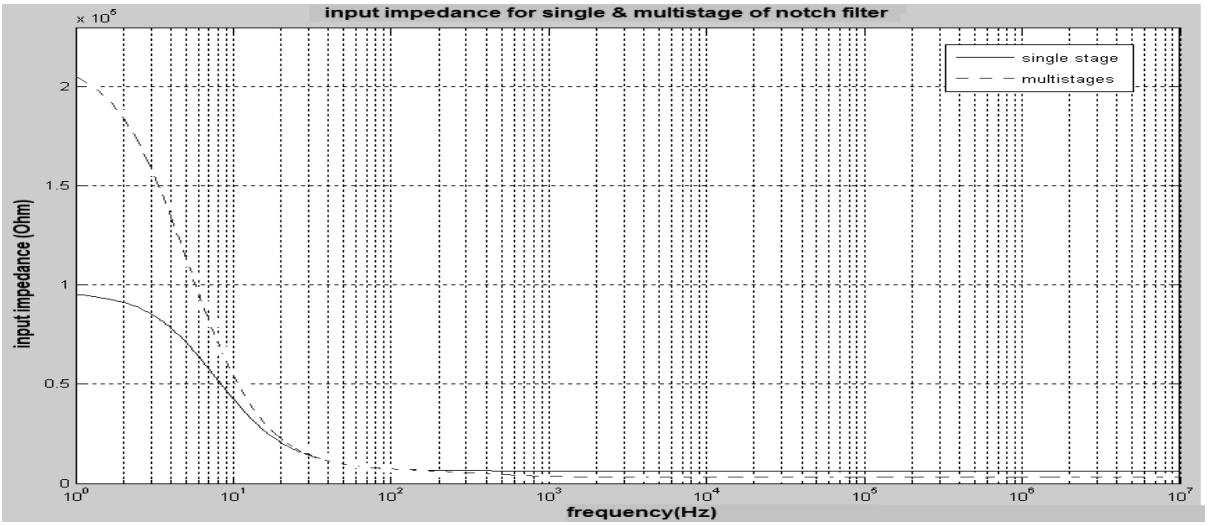


Figure (17): Input impedance responses of the single and 3-stage notched filters.

The first coupling circuit: For this purpose the RC-circuit without the ferrite transformer was chosen. In this design a single stage of notch filter was connected in cascade with four stages of high pass filter as shown in Fig. (18). The transfer function for this circuit is shown in Fig. (19). The 50 Hz has been strongly attenuated with constant gain achieved for frequencies above 10 kHz. Thus an efficient coupling was obtained practically using this configuration, therefore, this design was used to measure the frequency response of the practical PLC channel.

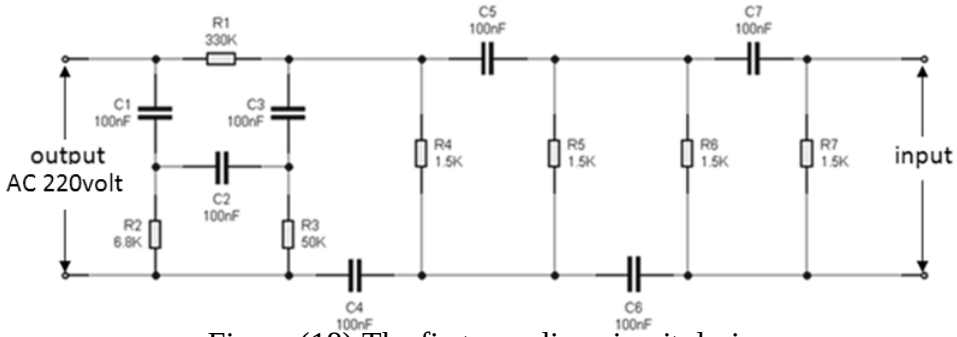


Figure (18):The first coupling circuit design

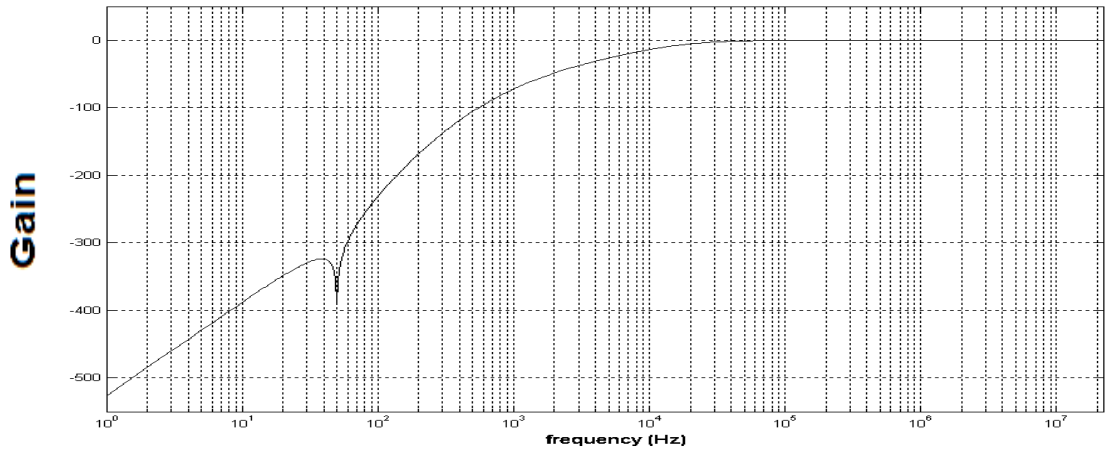


Figure (19): frequency response of the first coupling circuit design

The second coupling circuit:A voltage stepping up in passive circuit can be obtained using transformer, thus in the second coupling circuit, the notch filter was connected directly to the primary coil of a ferrite transformer as shown in Fig. (20). The measured frequency response for the circuit of Fig. (20) is shown in Fig. (21).Figure (21) shows that, the input signal can be boosted up to an acceptable level to offer the required performance, the voltage gain for the flat top portion is approximately equal to 12dB or 4.5 voltage ratio.

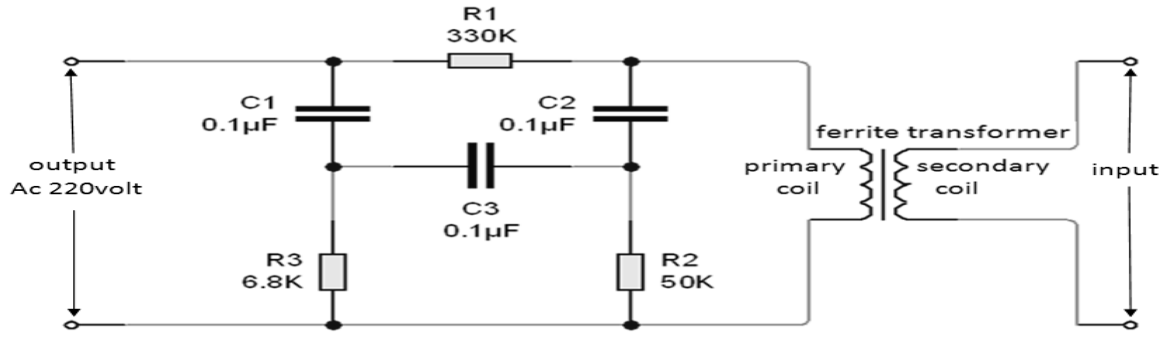


Figure (20):The second coupling circuit design

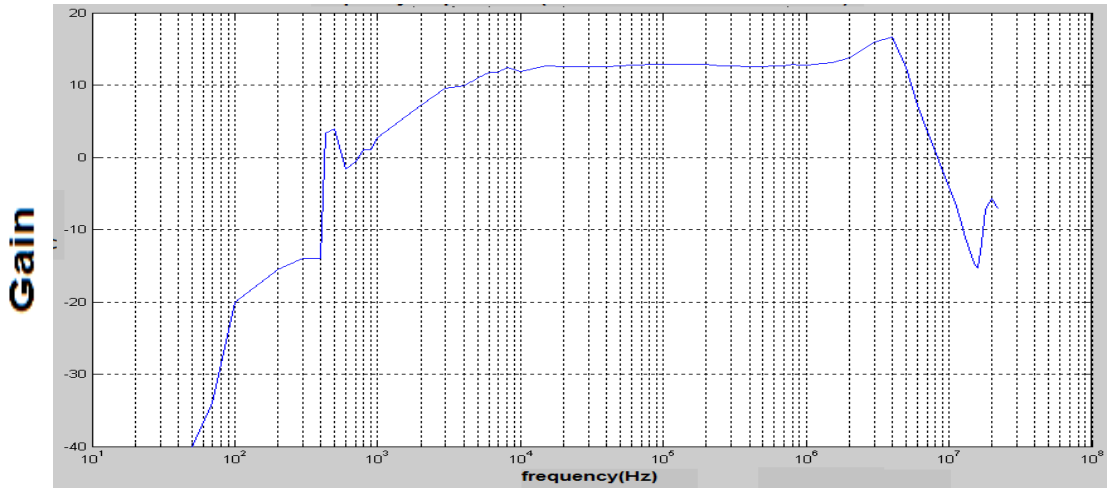


Figure (21): Frequency response for the second coupling circuit design

5-Measurements of BER on a Sample PLC Network:

Practical measurements were performed under normal laboratory environment. This simple test is aimed to assess the mains wiring in a typical laboratory, where there are many branches to the test benches.The used equipment were; function generator, oscilloscope, bit error rate (BER) measuring set (Anritsu Model MS315A). The coupling circuit thatwas used to inject the PLC signal into the mains network isthe same as that shown in Fig. (18). Two coupling circuits for transmitter and receiver were used in the measurements as shown in Fig. 22-a. The measured frequency response is plotted in Fig. (22-b).The bit error rate,was then measured in a typical laboratory, where two AC sockets were used for transmission and reception the using BER measuring set. The specifications of the injected test signal were, digital waveform, AMI format and clock rate =8.44 Mbps. Two measurements were performed; the first was when the mains power supplying the laboratory was off, thus there is no 50Hz signal. The other measurement was under normal working condition. The measured results are listed in Table 3, which show reduced BER due to the mains power voltage.

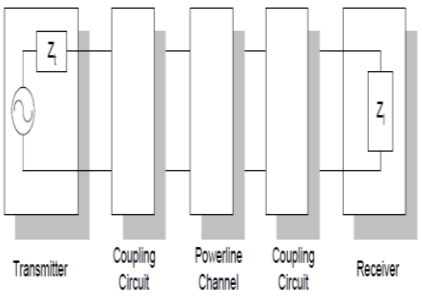


Figure **(22.a)**Sample PLC

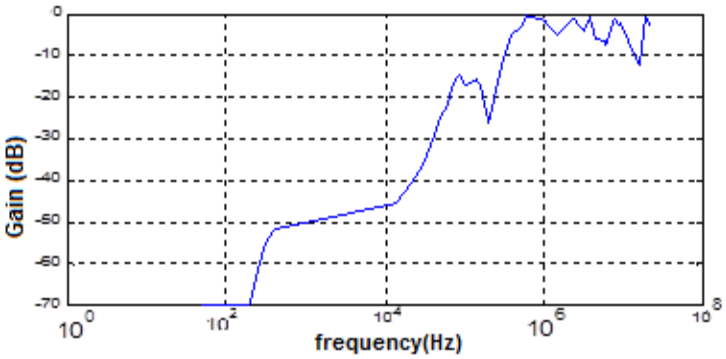


Figure **(22.b)**Measured transfer function of PLC

Table (3): Results of measuring the BER for the actual PLC network.

Case	Bit Error Rate
Without power signal	BER < 10^{-7}
With power signal	10^{-6}< BER<10^{-3}

Conclusions:

The modeling of a simple PLC channel has been demonstrated using the ABCD matrix approach, and MATLAB to calculate the transfer function for investigating the performance at various working conditions. Theeffects of cable lengths, number of tabbing branches, resistance of the cableswere investigated. The results show that longer cables, and higher resistance of them, as well as number of branches result in increased attenuation and limitation of transmission frequency.Theoretical and practical assessments of coupling circuits using iron and ferrite transformers, and notch filters showed better performance of ferrite transformer. Adequate rejection of the 50 Hz power signal can be achieved.Measurements on an example of PLC system in a university laboratory showed that such system is feasible. More comprehensive test in local building can assess the ability of the mains networks to offer PLC communications.

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Design and Fabrication of A Single Layer Dual Band Microstrip Patch Antenna For GPS Applications

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Abstract

In this paper design and fabrication of a single layer dual band microstrip antenna for GPS applications has been presented. This proposed antenna operates at the two bands of GPS systems (L1=1.575 GHz and L2=1.227 GHz). The antenna has a square shape, which contains four triangular slots and two lines from both sides, in addition two slots from above and below the patch down the center. The proposed antenna provides good return loss S_{11}, Axial Ratio, impedance behavior, farfield radiation pattern and gain. The simulation and measured results showed good agreement. The designed antenna has been analyzed using CST® Microwave studio version 2010.

Keyword: Circular polarization; Dual-frequency; Global Positioning System Antenna (GPSA); Microstrip antenna.

تصميم وتصنيع هوائي الشريحة الرقيقة احادي الطبقة ثنائي الحزمة لاستخدامه في النظام الكوني لتحديد المواقع

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كلية الهندسة / جامعة الموصل / العراق

الملخص

في هذا البحث تم تصميم وتصنيع هوائي الشريحة الرقيقة احادي الطبقة ثنائية الحزمة لاستخدامه في النظام العالمي لتحديد المواقع. الهوائي المقترح يعمل عند الترددين (1.227 GHZ & 1.575 GHz) وذو شكل مربع بالأساس محتوي على اربعة شقوق مثلثة وخطين على جانبي الرقعة مع شقين من اعلى واسفل الرقعة. يقدم الهوائي المقترح فقد ارجاع ونسبة محورية وموائمة ونمط اشعاع وربح جيد ومناسب لاستخدام هذا الهوائي في نظام الـ GPS. تم الحصول على نتائج عملية مقاربة الى حد كبير مع النتائج النظرية. تم استخدام برنامج CST® في تصميم الهوائي.

I. Introduction

Global positioning system (GPS) is one of the intelligent transport system (ITS) applications. Most current GPS receivers only use the Ll frequency of 1.575 GHz with right hand circular polarization. However, in some applications that need more accurate information, differential GPS is employed and an antenna is required to cover both L1 and L2 (1.227 GHz). Many applications in communications and radars require circular or dual linear polarization, and the flexibility afforded by microstrip antenna technology has led to a wide variety of designs and techniques to fill this need [1]. The ideal radiation pattern of a terminal user GPS antenna is shown in Figure 1. The pattern is a broadside unidirectional beam. Constant coverage should be maintained in azimuth. To reduce the reception of multipath signals, it is necessary that the antenna pattern have deep nulls along the horizontal. Therefore, the elevation pattern should be nearly constant down to an angle of 10^o, 15^o from horizontal.

Microstrip patch antennas have been widely used in many circular polarization (CP) applications due to low profile, low weight and useful radiation characteristics.

The fundamental advantages of circular polarization are its high penetration capability compared with linear polarization and its ability of establishing a reliable signal link irrespective of the antenna orientation of the device. Therefore, circular polarization delivers better connectivity with both fixed and mobile devices [2, 3].While circular polarization microstrip antennas are used more widely in mobile communication and GPS systems, because they can restrain the interference of rain and fog and resist the multipath reflections [4]. The CP microstrip antennas can be realized by using either singled-feed or dual-feed, and the major advantage of single-feed designs is their simple feed structures, which do not require external phase shifter. Many single-band CP microstrip antennas with single-feed are presented in [1]. To have a circular polarized radiation, the orthogonal field components should be of equal magnitude and having a phase difference of 90^o, so it is a great challenge to satisfy the circular polarized radiations conditions at two different bands.

Lately, slots are extremely used in microstrip antenna designs [5 - 6]. In this paper, a single layer microstrip antenna for GPS applications is presented. Details of the proposed antenna and simulated results are presented and discussed.

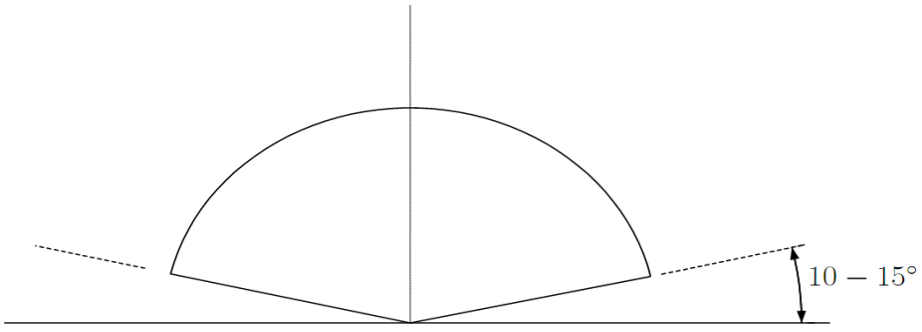


Figure (1): GPS nominal radiation

II. Antenna Structure and Design

The geometry of the proposed slot dual-band antenna is illustrated in Figure 2. The thickness of the substrate used is 1.6 mm, FR-4 substrate (ε_r =4.4 , tangent loss = 0.025). A 50ohm coaxial probe feed is located along the direction 45° to the centerlines of the square patch, location feed (5 , 5) .The ground plane and the substrate have the square area size of 98 mm * 98 mm . In order to obtain a circular polarization characteristics, a square shape antenna has been chosen. The dimensions of the antenna (L&W) are calculated according to the following equations [3]:

$$w = \frac{v_o}{2f_r}\sqrt{\frac{2}{\varepsilon_r+1}} \quad (1)$$

$$\varepsilon_{reff} = \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2}\left(1+12\frac{h}{w}\right)^{-\frac{1}{2}} \quad (2)$$

Where W is the width of the patch, f is target center frequency, v_o is the speed of light in a vacuum and the effective dielectric constant can be calculated by the equation:

$$\frac{\Delta L}{h} = 0.412\frac{(\varepsilon_{reff}+0.3)(\frac{W}{h}+0.264)}{(\varepsilon_{reff}-0.258)(\frac{W}{h}+0.8)} \quad (3)$$

Where the ε_r dielectric constant of the substrate and h is the thickness of the substrate. The fringing field around the periphery of the patch electrically makes the antenna larger than its physical dimensions. Δl takes this effect in account and can be expressed as:

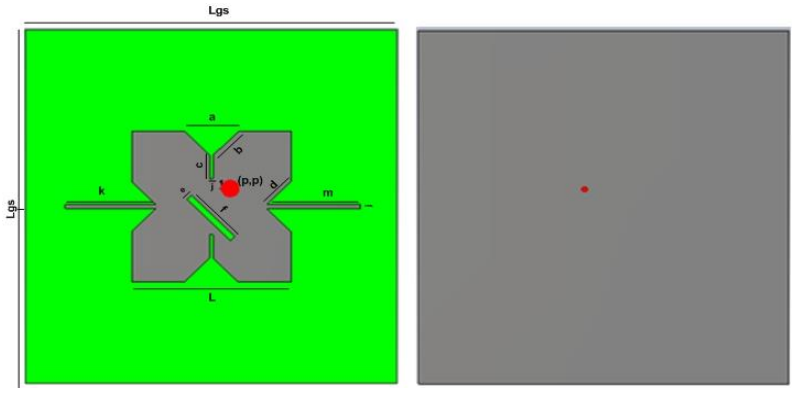
$$L = \frac{1}{2f_r\sqrt{\varepsilon_{reff}}\sqrt{\mu_o\epsilon_o}} - \Delta L \quad (4)$$

L is the length of the patch.

Table 1 shows the optimum design parameters of the proposed antenna.

Table (1): The parameters of the proposed antenna

Parameter	L	a	b	c	d	e	f	k	m	Lgs
Value in mm	41.87	10.23	7.3	8	7	1.7	16.5	32	34	98



Front view Back view

Figure (2): The proposed antenna

III. Simulation Results

The return loss of the proposed antenna is shown in Figure 3. At resonant frequencies of 1.575 GHz and 1.227 GHz the antenna had return loss of -21.085 dB and -21.289 dB respectively.

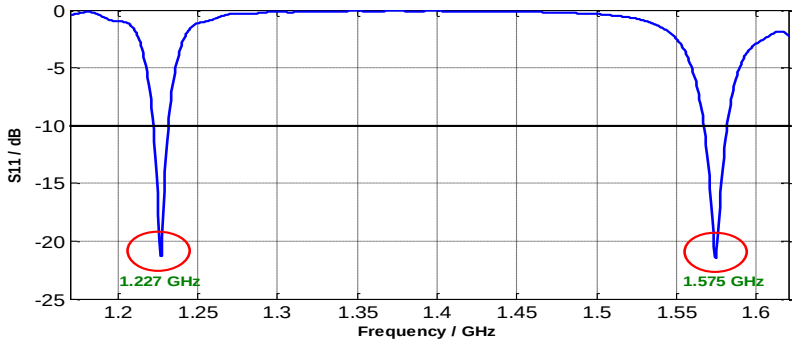


Figure (3): Return Loss of the proposed antenna

Figure 3 shows that the antenna is matched for 1.575GHz and 1.227GHz.
$RL_{1.575GHz}$ = -21.08 dB gives that 0.78 % of the incident power is reflected.
$RL_{1.227GHz}$ = -21.289 dB gives that 0.74 % of the incident power is reflected.

The bandwidth of the proposed antenna is:
For L1 (1.575 GHz) = 15 MHz from1.567GHz to 1.582GHz.
For L2 (1.227 GHz) = 10 MHz from 1.222GHz to 1.232 GHz.

The smith chart has two axes. The horizontal line is the resistance axis and the circular boundary is the reactance axis. By studying the smith chart, it shows how the antenna is good matched. The simulation results show the normalized value for the impedance (Z_s), where Z_s =1 in the smith chart represents the impedance of the antenna $Z_{antenna}$ =50 Z_s .

Figure 4 shows that the antenna is good matched at 1.575GHz and 1.227GHz since the blue point is near Z_s = 1. Figure 4 shows $Z_{antenna}$ = 42.1+1.6i Ω at 1.575GHz and for 1.227GHz $Z_{antenna}$ = 58-4.1$i\Omega$.

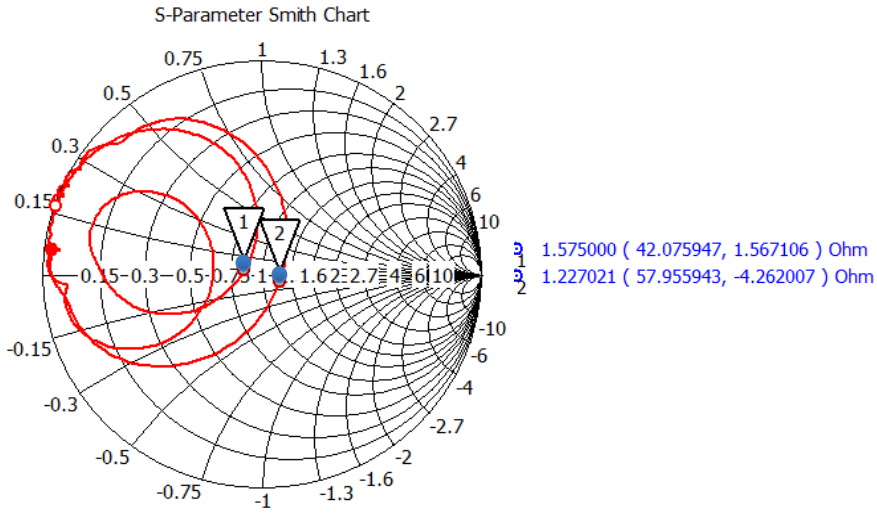


Figure (4): Smith Chart of the single layer dual band microstrip antenna.

The typically desired value of VSWR to indicate a good impedance match is 2.0 or less. Figure 5 shows the VSWR of the proposed antenna. The VSWR of the 1.575GHz is 1:1.19 and 1:1.18 for 1.227GHz.

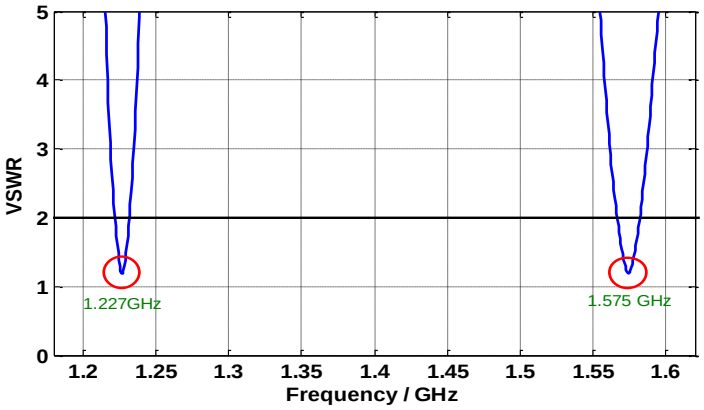


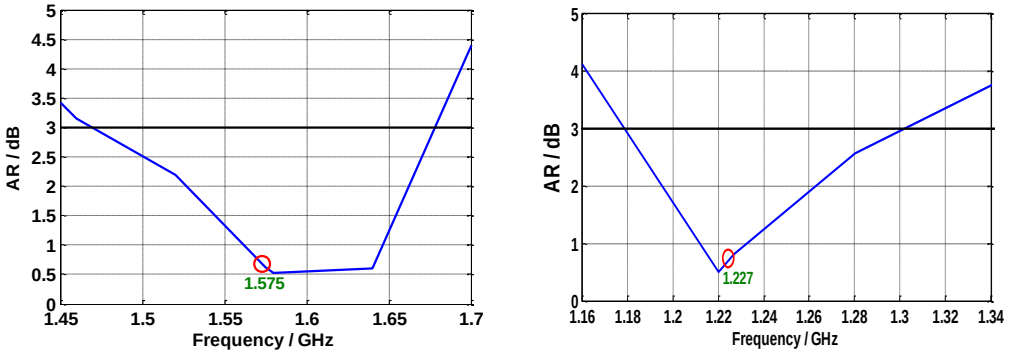
Figure (5): VSWR of the proposed antenna

The CP (Circular Polarization) antenna could have many different types and structures where the basic operation principle is to radiate two orthogonal filed components with equal amplitude but in phase quadrature. CP of the signal has advantages in terms of wireless signal propagation [7].

Figure 6 shows the antenna axial ratio versus frequencies (1.575GHz & 1.227 GHz) with 3 dB.

$AR_{1.575GHz}$ = 0.6dB (< 3dB)

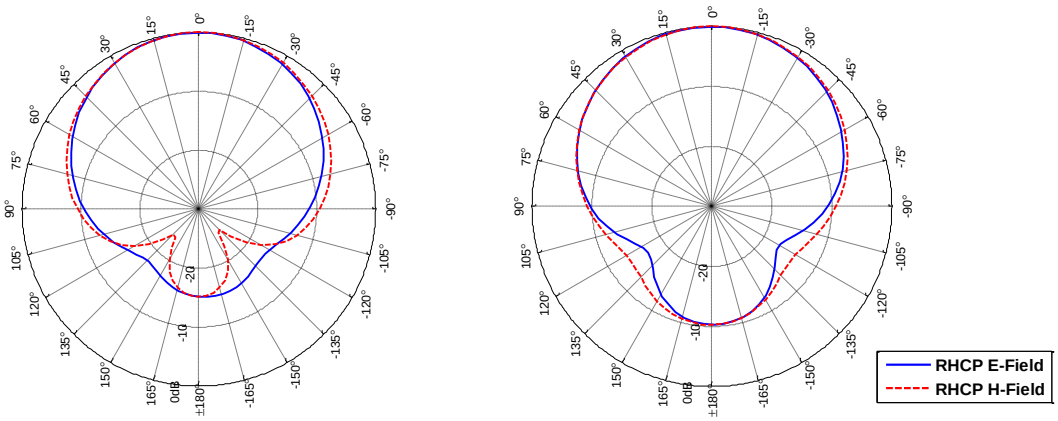
$AR_{1.227GHz}$ = 0.8dB (< 3dB)



a- 1.575GHz **b- 1.227GHz**

Figure (6): Axial Ratio versus frequency

Figure 7 shows the RHCP (Right Hand Circular Polarization) radiation pattern for proposed antenna.

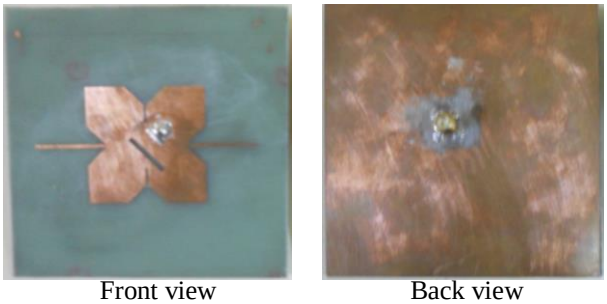


a- 1.575GHz b- 1.227GHz

Figure (7): RHCP for proposed antenna

IV. Practical Results

Figure 8 illustrate the fabricated proposed antenna and Figure 9 illustrate the transmitter and receiver positions in the anechoic chamber. The used spectrum analyzer (GSP-830, GWINSTEK 9KHz – 3 GHz) was placed outside the chamber and connected to the receiver through SMA cable. The antenna in the receiver side was placed on a turn table with remote control to scan the antenna by 360^{o} from outside the chamber. Wires, turn table and other parts were covered by absorbing material to reduce reflections. The signal generators used to supply the transmitter antennas was (Anritsu/ MG3670B/ 2.2 GHz). The far field patterns of the proposed antenna was measured in anechoic chamber in the department of Electrical Engineering/University of Mosul.



Front view Back view

Figure (8): The fabricate of proposed antenna

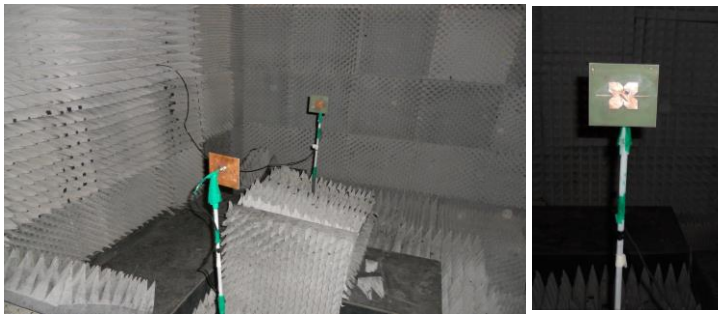


Figure (9): The transmitter and receiver positions in the anechoic chamber

The radiation patterns were measured in both E- and H-planes. The measured results compared with simulation results are shown in Figure 10. Good agreement is noticed between simulation and experimental results. It can be noticed that the patterns shows better agreements in the H-plane as compared to the E-plane.

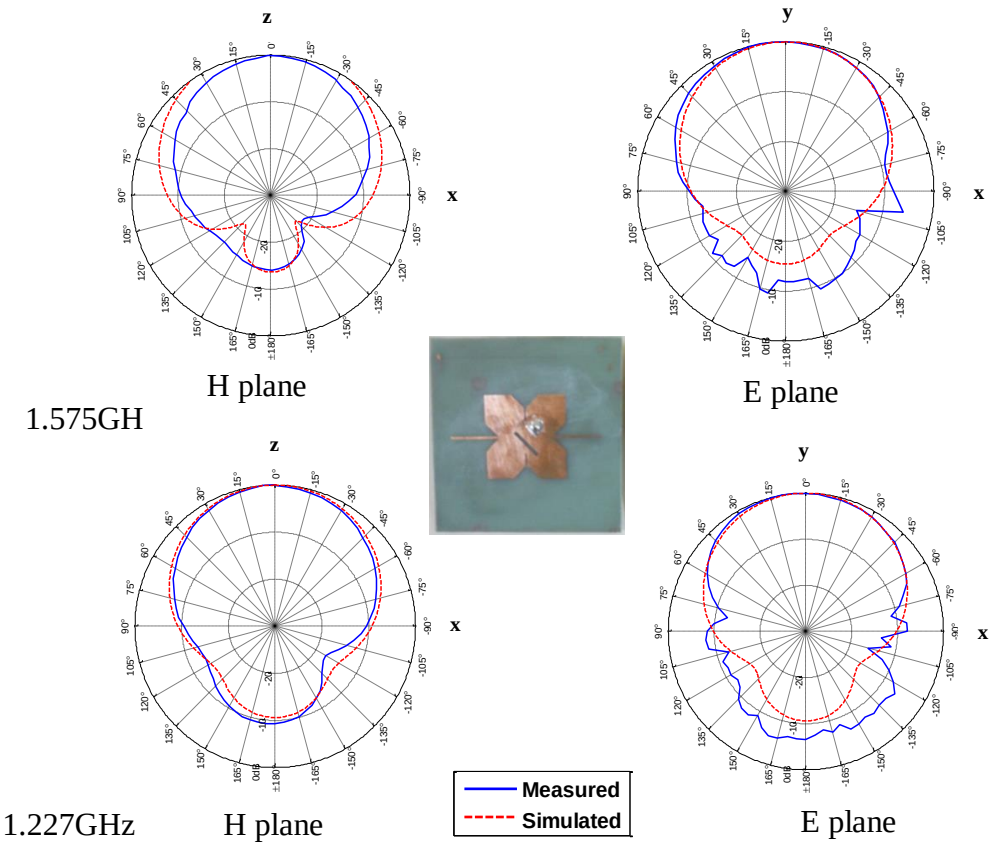
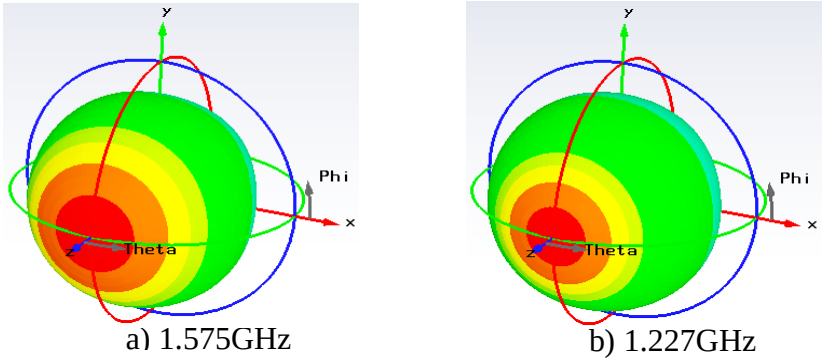


Figure (10): Radiation Pattern of the proposed antenna

For further evaluation of the volumetric radiation patterns, the three dimensional variations of the radiated fields for the proposed antennas were calculated and are shown in Figure 11. Figure 11 gives more appreciation of the field shape as compared to those of the 2-D representations.



a) 1.575GHz b) 1.227GHz

Figure (11): The 3-D patterns of proposed

The gain is a useful measure describing the performance of the proposed antennas. It is a measure that takes into account the efficiency of the antenna as well as its directional capabilities. The gain of the proposed antenna was calculated from the far field patterns using the CST package, and the obtained gains versus frequency are shown in Figure 12.

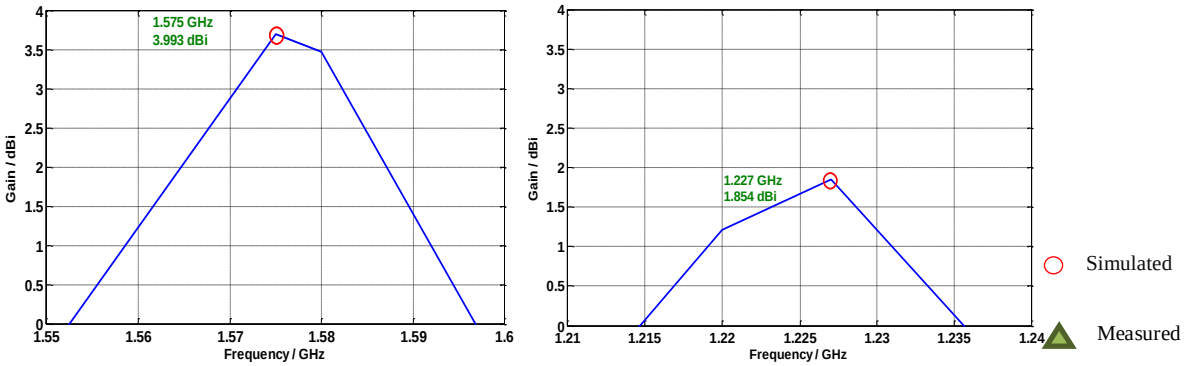


Figure (12): Gain versus frequency of the proposed antenna
a- 1.575 GHz b- 1.227 GHz

Table 2 shows Comparison between the measured and simulated gain for the proposed antennas.

Table (2): Comparison between the measured and simulated

Frequency / Antenna	1.575GHz	1.227GHz
Simulated Gain	3.993	1.854
Measured Gain	2.6	2.2

Figure (13) Shows the efficiency of the proposed antenna. The proposed antenna achieved efficiency of (60%) for the L1(1.575GHz) band while the efficiency drops to (47%) at frequency of L2(1.227 GHz)

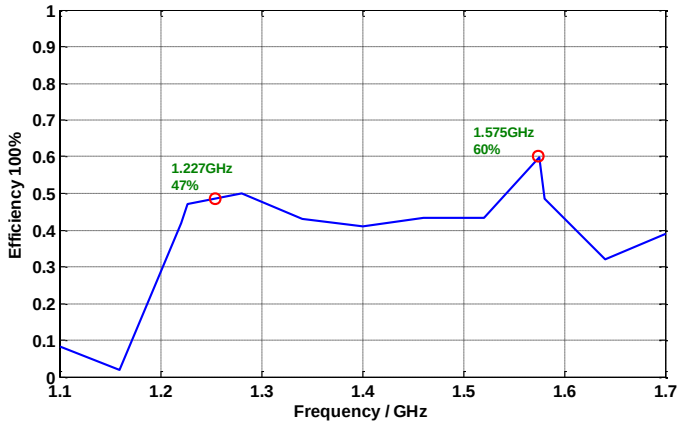


Figure (13): Efficiency of the proposed antenna

V. Conclusion

In this paper a single feed single layer dual-band circular polarized slotted patch antenna is proposed. The antenna is fabricated on a FR4 substrate of overall dimensions 98* 98mm. The thickness of the substrate is 1.6 mm with a relative permittivity of 4.4. The proposed antenna exhibits impedance bandwidth of 15MHz at 1.575GHz and 10MHz at 1.227GHz. Measured gains at the broadside direction at L1 and L2 are about 2.6 and 2.2 dBi, respectively. From the results, it is seen that the proposed antenna achieves good dual band performance and the antenna has a hemispherical radiation pattern with a good circular polarized, this makes the proposed antenna design suitable for use in the GPS applications. The simulation and measured results showed good agreement.

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Implementation of Encoding and Decoding H264/AVC Standard Simulation Using MATLAB Ready-Made According to the Theory of the Three-Step Search

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Abstract

The video coding standards are being developed to satisfy the requirements of applications for various purposes, better picture quality, higher coding efficiency, and more error robustness. The new international video coding standard H.264 /AVC aims at having significant improvements in coding efficiency, and error robustness in comparison with the previous standards such as MPEG-2,H261, H.263,H264. Video stream needs to be processed from several steps in order to encode and decode the video such that it is compressed efficiently with available limited resources of hardware and software. Each step can be implemented with different algorithms to accomplish required task. All advantages and disadvantages of available algorithms should be known to implement a codec to accomplish final requirement. The purpose of this project is to implement all basic building blocks of H.264 video encoder and decoder. The significance of the project is the inclusion of all components required to encode and decode a video in Matlab .
Key Word:H264/AVC ,intra frame(I-frame) , inter frame(P-frame)

تنفيذ المشفر وفك التشفير للمعيار H264/AVC باستخدام محاكاة MATLAB الجاهزة وفق خوارزمية الخطوات الثلاث

د. محمد حازم الجماس نور حمدون

الخلاصة

تم تطوير معايير تشفير الفيديو لتلبية متطلبات التطبيقات المختلفة وللحصول على جودة صور أفضل واستغلال اكبر قدر ممكن من النطاق الترددي مع تقليل نسبة الأخطاء. طورت المنظمة الدولية للمعايير الفيديو القياسية معيار يعرف H.264 / AVC يهدف إلى وجود تحسينات كبيرة في كفاءة الترميز، ومتانة خطأ بالمقارنة مع المعايير السابقة مثل MPEG-2، H261، H.263، H264. يحتاج الفيديو لعمليات معالجة من عدة خطوات من أجل تشفير وفك التشفير بحيث يتم ضغط بكفاءة مع محدودية الموارد المتاحة من الأجهزة والبرمجيات. ويمكن تنفيذ كل خطوة مع خوارزميات مختلفة لإنجاز المهمة المطلوبة. الغرض من المشروع هو تنفيذ جميع المحتويات الأساسية لتشفير الفيديو H.264 ووحدة فك التشفير وإدراج جميع المكونات المطلوبة لتشفير وفك تشفير شريط الفيديو باستخدام محاكاة Matlab.
المصطلحات الأكثر أهمية: المعيار H264/AVC، الإطار الأولي(I-frame)، الإطار (P-frame)

1- المقدمة

نظرا لتطور وسائل الاتصالات ومجالات عرض الصور والفيديو لا بد أن يقابله تطور تقني في معدل تخفيض البيانات يعتبرH264 (المعروف أيضا باسم MPEG-4 الجزء AVC/10 لترميز الفيديو المتقدم)، أحدث معيار مستخدم لضغط الفيديو، ليصبح معيار الفيديو المفضل في السنوات المقبلة.

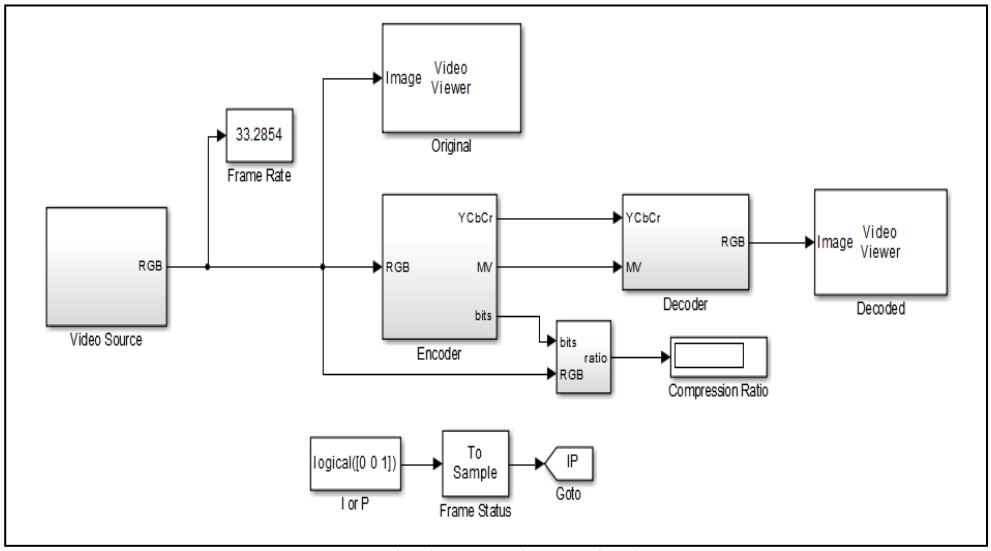
H.264 هو من المعايير المرخصة دوليا من قِبل (MPEG- ISO/IEC -ITU-T) ضمن كفاءة تفوق المعايير السابقة. ويمكن للمعيار H.264 تقليل حجم ملف الفيديو الرقمية أكثر من 80 ٪ مقارنة مع تقنيات ال JPEG وتصل إلى 50٪ أكثر من مع MPEG-4 الجزء 2 القياسية لكن يعتمد على نوعية مستوى الملف المستخدم الخاص بالمشفرH264 . وهذه النسبة من تقليل البيانات تعني استغلال اكبر حيز ممكن للنطاق الترددي الخاص بنقل البيانات وكذلك سعة التخزين المطلوبة لحفظ البيانات ، لا يمكن الاعتماد فقط على عمليات التشفير لا بد من وجود في الطرف المقابل محاكاة خاصة يمكن لها فك الرموز المشفرة وهذا ما يسمى (عملية فك التشفير). لقد اختلفت طرق التشفير من ناحية الأداء الخواص والكفاءة وإمكانية الاستعمال، حيث الطرق المستخدمة لتشفير الصور ذات الأحجام الصغيرة أو الكبيرة تختلف عن طرق تشفير المستخدمة للفيديو وهذا أيضا ينطبق على عملية فك التشفير وبعد عدة أبحاث وجد أن انسب الطرق المستخدمة لنقل معلومات الفيديو أو الصور ذات الأحجام الكبيرة هي (كبس المعلومات) أي تقليص المعلومات لكن بشرط أن لا يسبب في تغير المعلومات المتضمنة الأصلية لان في هذه الحالة عملية إعادة المعلومات تكون مستحيلة وعلى هذا الأساس تم بناء المشفرات وأجهزة فك التشفير.نتيجة للكفاءة التي تقدمها هكذا نوعيات من المشفرات توقع انتشارها على نطاق واسع في عدة مجالات ،وتم بالفعل إدخال H264 في الأدوات الإلكترونية الجديدة مثل الهواتف المحمولة ومشغلات الفيديو الرقمية، واكتسبت قبولا سريع من قبل المستخدمين النهائيين. ودخل أيضا كمساعد من النوع التطوري في الخدمات العامة مثل تخزين الفيديو على الانترنت وشركات الاتصالات وكاميرات المراقبة المستخدمة في المعامل الصناعية ، وبسبب تقبل هذه النوعية من المشفرات مدى واسع من الإطارات خلال الثانية ((60/30/25(fps) تم التوسع بها في تطبيقات مراقبة الطرق السريعة والمطارات، لكن يعد النوعية المستخدمة والأكثر شيوعيا لمدى الإطارات هو((30/25 (fps)، أن معظم الجدل القائم حول التقنيات المستخدمة لعملية تشفير المعلومات هو مدى سرعة ودقة الصور والفيديو بعد عملية التشفير وهل يمكن إعادة المعلومات بشكل كامل إذا تم اختزالها إلى النصف؟. سوف تتم الإجابة من خلال هذا البحث الذي يتضمن تمثيل المشفرH264 وفك التشفير لإعادة البيانات الأصلية باستخدام برنامج المحاكاة MATLAB لتحقيق نظام متكامل من تشفير البيانات وإعادتها بنفس كفاءة المستخدمة للنظام الأصلي.

2- عملية التشفير

عملية التشفير أو ما تسمى ضغط الفيديو هو تخفيض وإزالة بيانات الفيديو الزائدة بحيث ملف الفيديو الرقمي يمكن إرساله بفعالية أي بأقل نطاق ترددي ممكن الحصول علية وبأقل مساحة تخزينه. وتنطوي عملية التشفير على تطبيق خوارزمية لمصدر الفيديو لإنشاء ملف مضغوط وبتالي يكون على استعداد للنقل أو تخزين. لتشغيل ملف مضغوط يتم تطبيق خوارزمية عكسية لإنتاج الفيديو الذي يظهر تقريبا نفس المحتوى مصدر الفيديو الأصلي. ويطلق على زوج من الخوارزميات التي تعمل جنبا إلى جنب في ترميز الفيديو بتسمية (التشفير / فك التشفير). أنظمة فك التشفير وتشفير الفيديو كما في الشكل(1)، تقوم بتطبيق معايير مختلفة عادة ما تكون غير متوافقة مع بعضها البعض، أي أن محتوى الفيديو الذي تم ضغطه باستخدام معيار واحد لا يمكن أن يكون ضغط مع معيار مختلف. على سبيل المثال، الخوارزمية الخاصة بفك التشفير لمعيار MPEG-4 الجزء 2 لن تعمل مع خوارزمية التشفير الخاصة بمعيارH.264. ويعود السبب لأن خوارزمية واحدة لا يمكن أن تعمل على فك تشفير الإخراج من خوارزمية أخرى بشكل صحيح ولكن من الممكن تنفيذ العديد من خوارزميات مختلفة في نفس البرامج أو الأجهزة، التي من شأنها تمكين صيغ متعددة ليتم ضغطها.إذن اختلاف طرق التشفير يعتمد على الخوارزميات المختلفة التي تعطي كفاءة مختلفة،قد تختلف النتائج التي يمكن الحصول عليها من المشفر للمعيار الواحد بالاعتماد على التصميم أي يمكن لوحدة التشفير تحتوي على عدة مستويات كما في (H264) تعطي نسبة ضغط مختلفة لنفس المعيار الواحد ويمكن استرجاع البيانات في جهة المقابلة لوحدة فك التشفير بخوارزمية واحدة لجميع المستويات وتعتبر هذه الخاصية من المميزات المهمة لأنها تمكننا من استخدام عدة تطبيقات لمعيار واحد، بينما وحدة فك

التشفير هيا على عكس وحدة التشفير عند تصميمها يجب ان تكون متوافقة مع وحدة التشفير بصورة تامة لتمكننا من استعادة البيانات بشكل صحيح.

يمكننا استنتاج صفتين أساسيتين لغرض استعمال تشفير الفيديو الأولى تمكننا عملية التشفير بتعامل مع الفيديو ذو الصيغة الرقمية ونقلة وخزنة في بيئة لا يمكن لها أن تدعم معلومات الفيديو إذا كانت في حالتها ما قبل التشفير وهذا يلعب دورا مهما في الوقت المستغرق لعملية معالجة البيانات المستلمة حيث قبل عملية التشفير لا يمكن الحصول على الوقت الحقيقي فقط في حالة استخدام معلومات ذات أحجام صغيرة،إما الصفة الثانية مكنتنا من استغلال النطاق الترددي للقناة لنقل أكثر من فيديو حيث سابقا لا يمكن نقل فيديو واحد بصورة كاملة.إذن أصبح الهدف الرئيس من عملية كبس المعلومات هو الحصول على كفاءة عالية مع اقل خطأ ممكن خلال عملية التشفير والذي يمكننا من إعادة البيانات بصورة سليمة وهذا الهدف جعل من ابتكار عدة مشفرات للوصول إلى الكفاءة المثالية.



الشكل (1) المشفر وفك التشفير

3- مستويات H264

ركز الفريق المشترك لتطوير في تحديد عمل H.264 على إيجاد حل بسيط ومرن يمكنه أن يشمل مختلف التطبيقات من خلال استخدام معيار واحد، كما هو الحال في معايير الفيديو وغيرها، وتكمن هذه المرونة في توفير الإمكانيات لعدة profiles (تتمثل بمجموعات من الخوارزميات الخاصة بضغط البيانات) وlevels (المستوى الخاص لمجموعة تطبيقات).

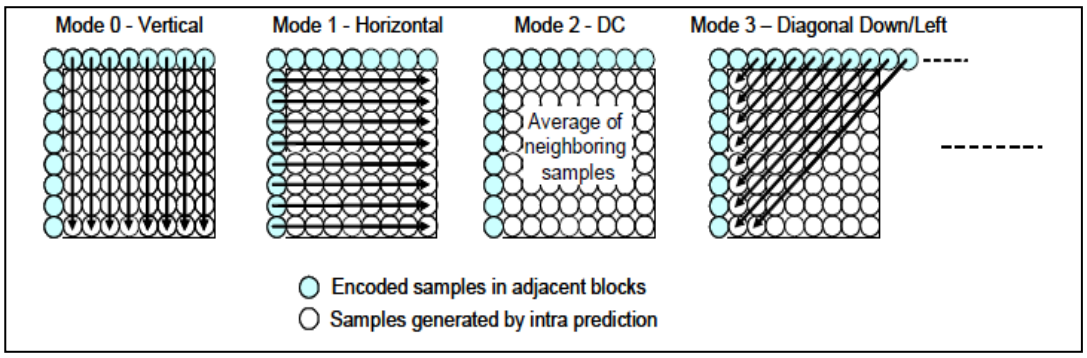
H.264 يحتوي على سبعة profiles، كل profile يستهدف فئة معينة من التطبيقات ويعرض طريقة تشفير معينة والتي يقابلها وحدة فك التشفير حيث كل profile لدية وحدة تشفير/فك التشفير خاصة بة،كما ذكرنا سابقا أن لكل profile يمتلك تطبيقات مختلفة وعلى سبيل المثال بعض أنواع الكاميرات الشبكية الخاصة للمراقبة وأجهزة تشفير الفيديو تستخدم baseline profile،الذي يستعمل بشكل واسع بسبب الأداء الجيد خلال الزمن الحقيقي ويعطي زمن تنفيذ منخفض وهو عامل مهم جدا في الزمن الحقيقي ،H.264 يحتوي على 11 نوع من المستويات أو درجة من القدرة على الأداء وعرض النطاق الترددي ومتطلبات الذاكرة. يعرف كل مستوى معدل التشفير البت في الكتلة خلال الثانية الواحدة لنوعية الإطارات تتراوح بين QCIF إلى HDTV.

4- أنواع الإطارات

اعتمادا على الملف الشخصي الخاص بالـ (H.264)، وجد انه يتكون من أنواع مختلفة من الإطارات مثل (I-B-P)، ويمكن استخدامه في التشفير للحصول على الكفاءة المطلوبة وفيما يلي توضيح الصيغة النظرية لكل نوعية من الإطارات.

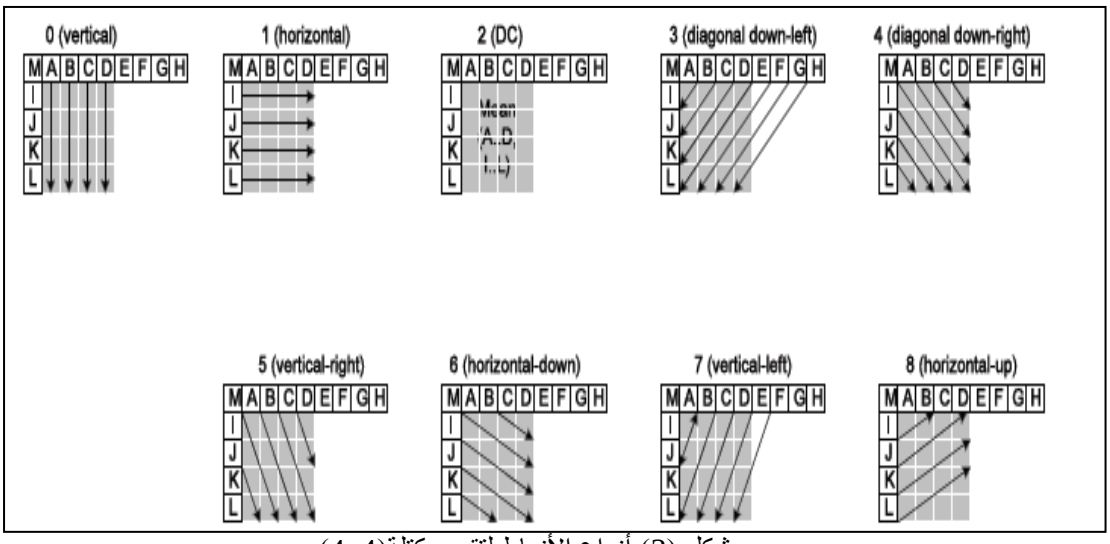
- (I-intra frame) هو إطار مستقل بذاته أي يمكن تشفيره وفك التشفير بصورة مستقلة بدون الحاجة إلى صورة أخرى كمصدر لاسترجاع المعلومات،الصورة الأولى من الفيديو تتمثل لهذا النوع من الإطارات،ويعتبر أل(-I

frame)هو نقطة بداية لعرض الفيديو وكذلك له أهمية في تزامن استرجاع المعلومات إذا حدث أي تلف في نقل تيار البت(bit stream)،العيب في هذا الإطار انه يستهلك اكبر عدد ممكن من البت للتشفير لأنه يأخذ الإطار بصورة كاملة ولكن من ناحية أخرى نسبة الخطأ تكون قليلة. طريقة التشفير هذا النوع من الإطار يمتلك خاصيتين بالاعتماد على طريقة تقسيم الكتلة إما (16x16) أو (4x4) ولكن بصورة عامة تتمثل بتحويل الإطار من صيغة(RGB) إلى صيغة(YCbCr) ويفصل كل عنصر عن الأخر من التمثيل الأخير ويتم التعامل معه بصورة مفردة،الغاية بتمثيل صيغة الفيديو((YCbCr(4:2:0) هو تقليل الحساسية للعين حيث العين تستجيب للسطوع قبل الألوان لذا نجد أن عنصر (Y)يمثل رمز السطوع (luminance) بينما أل(CbCr) يمثل الألوان (chrominance) يؤخذ عنصر أل Y بحجمه الكامل بينما باقي العناصر تخفض نسبة البت إلى نصف كمية البت الموجودة في عنصر(Y)أي إذ كان حجم العنصر(Y) هو 16x16 فأن باقي العناصر تكون بحجم 8x8 ،وهذا يعني انه نوع مضمن من التشفير قبل عملية التشفير الرئيسية. عملية التشفير كما ذكرنا سابقا أنها تعتمد على التقسيم الإطارات ،يقسم الإطار إلى عدة كتل بحجم 16x16 ويمتلك 4أنواع من الأنماط للتشفير كما في الشكل (2).



شكل(2) أنواع الأنماط لتضمين كتلة التقسيم(16x16)

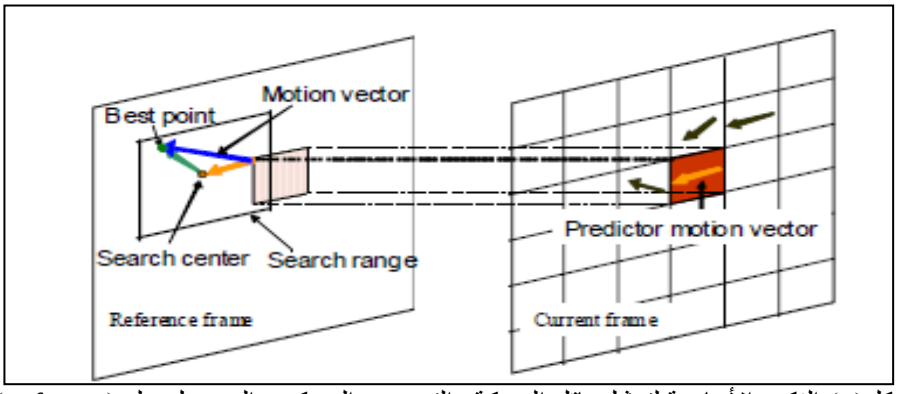
لكن في حالة تقسيم الإطار إلى 4x4 فأنة يمتلك 9 أنماط،كما في الشكل (3)



شكل (3) أنواع الأنماط لتقسيم كتلة(4x4)

يتم اختيار احد الأنماط بالاعتماد على التطبيق والكفاءة المطلوبة لعملية التشفير ومدى قبول نسبة الخطأ،في اغلب الأحيان مقدار نسبة الخطأ للفيديو تكون ذات مرونة أعلى مقارنة لنسبة الخطأ في حالة الصورة الواحدة،في هذا البحث تم استخدام حجم كتلة 16x16 ونمط الأول(Vertical mode).

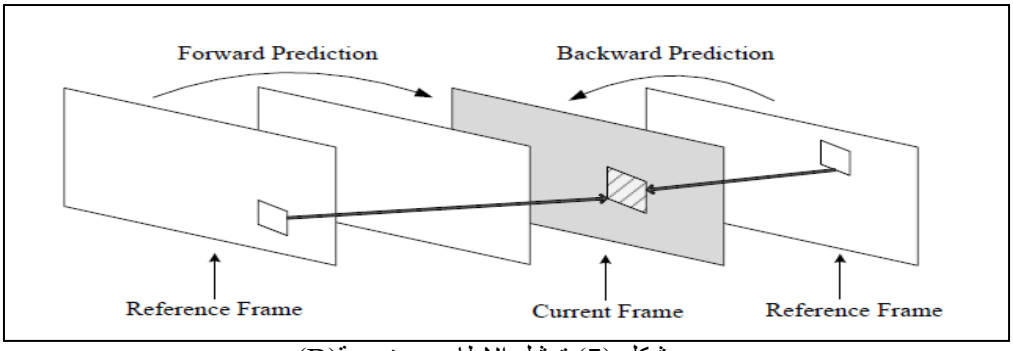
- (P- Inter Frame) الإطار التنبؤي(predictive inter frame) مشتق من الإطار الحالي لتسلسل الفيديو يتميز هذا الإطار بتقليل الزيادة الزمنية بين الإطارات على عكس النوعية السابقة حيث يعمل فقط ضمن الحيز المكاني للبكسل، مبدأ عمله يعتمد على النظرية المتعبة لكن بصورة أساسية يتم مقارنة الكتلة من الإطار الحالي مع الكتلة من الإطار السابق ويتم البحث على مركز الكتلة إلى أن يتم التطابق اعتمادا



شكل(4) الفكرة الأساسية لتمثيل ناقل الحركة والتعويض الحركي والحصول على(P-frame)

على النظرية المتبعة وهذا ما يسمى ب(matching block)، جميع النظريات تمتلك أساس واحد وهو البحث على أفضل تطابق ممكن وهذا ما يسمى تخمين الحركة ((motion estimation (ME)، بعد إيجاد أفضل تطابق تطرح الكتلة الحالية من الكتلة الأصلية والمتبقي يعرف بأسم التعويض الحركي (motion compensation)، الرابط بين موقع الكتلة الحالية مع الكتلة الأصلية هو ناقل الحركة (vector(MV) motion) كما في شكل(4)، يؤخذ كُلاً من التعويض الحركي مع ناقل الحركة ويشفر وينقل وبهذا تتم عملية التشفير.

- B-frames(bi-predictive inter frame) هذه النوعية من الإطارات تكون وسطية أي ما بين (I,B frames) ويستخدم في المستويات العالية للحصول على كفاءة مثالية لكن نسبة التعقيد فيها أعلى من النوعيات السابقة حيث يتبع الأساس في العمل اخذ مقارنة مابين أكثر من مصدر للكتلة الواحدة ،بمعنى أخر يتنبأ من المصدر الأصلي والمصدر المتوقع كما في الشكل (5).



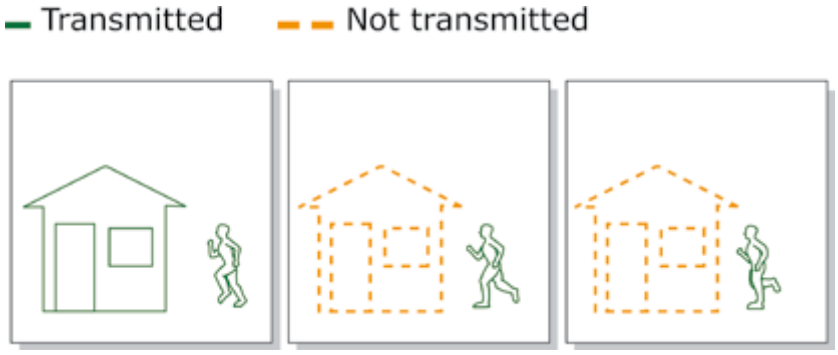
شكل (5) تمثيل الإطار من نوعية(B)

عند استرجاع المعلومات في عملية فك التشفير يكون(I-frame)الأسبق في فك التشفير ويليها (B-P frames) في حالة استخدامها، يكون فك التشفير يعتمد احدهما على الأخر في استرجاع المعلومات من الإطار الأصلي.

H264 يمتلك عدة طرق في التشفير إما أن يستخدم تشفير(I-frame) بمفردة أو يستخدم (I&P) أو(I&B&P) ولكل طريقة لها خواصها، في حالة استخدام الطريقة الأولى فأن كمية البت المشفرة تكون عالية مقارنة مع الحالات الأخرى لكن نسبة الخطأ قليلة لان كل إطار يشفر بصورة منفردة بدون الاعتماد على الإطار السابق وتستخدم هذه الطريقة في بعض التطبيقات التي بحاجة إلى دقة عالية كما في كاميرات مراقبة السجون والبنوك لتمكن من الحصول على أوضح صورة خلال عملية التكبير كما في الشكل (6).

شكل (6) تشفير الفيديو باستخدام المواقع المكانية للصور

لكن في حالة استخدام الطريقة الثانية كما في شكل(7) فتمتلك خواص أنها تقلل عدد البت المشفر وكذلك ونسبة الخطأ مقبولة وتستخدم هذه الطريقة في ضغط الفيديو بصورة عامة والكاميرات، أما في النوعية الثالثة تكون أكثر تعقيدا من كلتا الطريقتين لكنها تمتلك نسبة تقليل البيانات المشفرة بصورة اكبر وتحتوي على تأخير أعلى من الطريقتين بسبب عملية البحث عن التطابق لأكثر من مصدر.

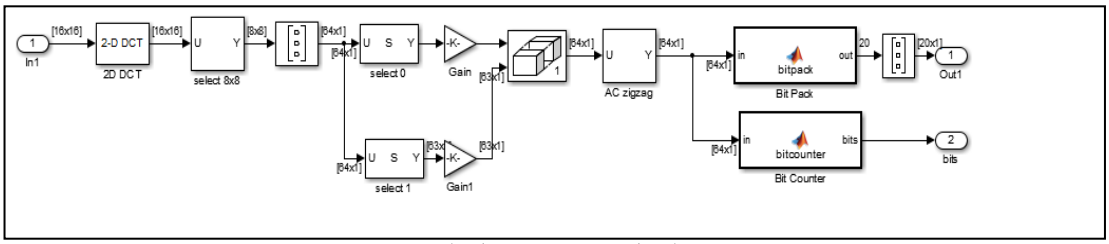


شكل (7) الصورة الأولى تمثل الإطار (I-Frame) ويشفر بمفردة،
الصورة الثانية والثالثة فقط يشفر الجزء المتحرك

5- عملية التشفير وفك التشفير باستخدام محاكاة MATLAB الجاهزة

تحدثنا في السابق عن نوعية الإطارات وكيفية عملية تشفيرها في H264 تقسم عملية التشفير إلى طريقتين الأولى هي عملية تشفير ألـ (I-frame)والثانية خاصة بـ (P-frame) يتميز ألـ (I-frame) بأن تشفيره مكانيا مع اختيار نوعية محددة من الأنماط بحيث كل المعلومات اللازمة لإعادة بنائه يتم تشفيرها داخل الجزء هذا الإطار للتيار البتH264.

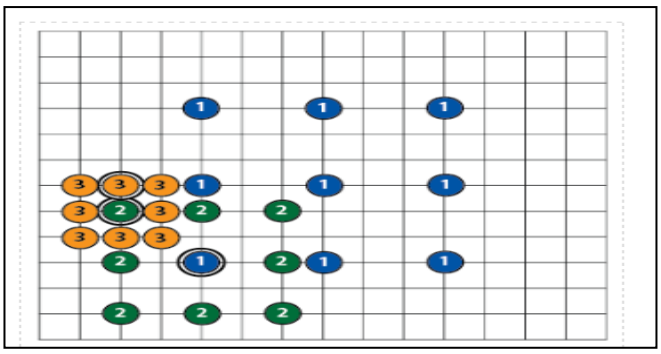
تتم معالجة كل كتلة من الإطار بشكل مستقل ومنفصل عن الأخرى تؤخذ كتلة 16x16 منفصلة ويطبق عليها النمط الأول (النمط العمودي) ويدخل إلى جيب التمام (DCT). هذا التحويل يولد تمثيل كل كتلة 16x16 في مجال التردد بدلا من المجال المكاني. إن القيم الناتجة من عملية DCT عادة ما تتألف من عدد قليل من القيم الكبيرة والعديد من القيم الصغيرة وتمثل الأحجام النسبية لهذه المعاملات مدى أهمية كل كتلة لإعادة المعلومات في مرحلة فك التشفير بصورة دقيقة بعد هذه العملية تتدخل المعاملات إلى التقريب كما في الشكل (8).



الشكل(8) دائرة تمثيل المشفر

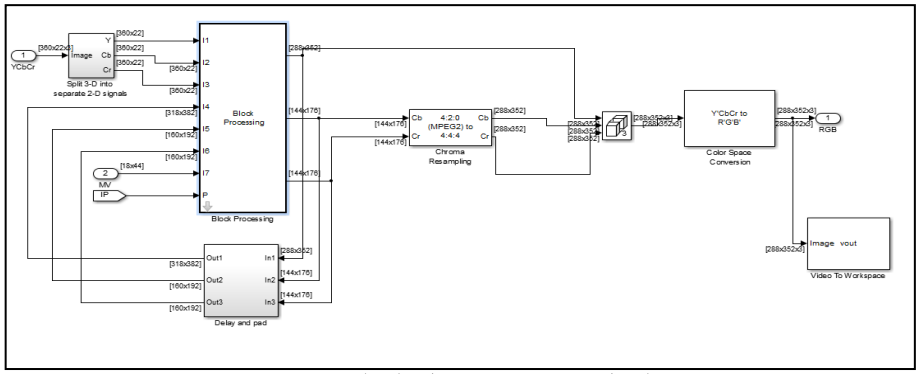
أما الطريقة الثانية تتمثل بتشفير (P-frame) ، وكما ذكرنا سابقا أن التشفير لهذا النوع من الإطار هو تشفير زمنيا وهذا يعني أنه يستخدم ارتباط بين الإطار الحالي و الإطار(أو الإطارات) الماضية لتحقيق ضغط.
ويتم تحقيق التشفير الزمني باستخدام ناقلات الحركة (motion vectors). الفكرة الأساسية هي أن تطابق كل كتلة في الإطار الحالي بمساحة 16x16 بكسل في الإطار المرجعي الماضي، التطابق هنا يمكن حسابه بطرق كثيرة، ولكن في (H264) يستخدم مقياس بسيط وأكثر شيوعا هو مجموع الفروق المطلقة (SAD). الإزاحة من الحركة الحالية إلى الحركة الماضية يتم تمثيلها في الإطار المرجعي إلى قيمتين (ناقلات أفقية ،ناقلات عمودية) يتم البحث للعثور على أفضل ناقلات الحركة في المساحة المحددة للبحث فقط. عند إيجاد اقل قيمة للمجموع الفرق يتم التطابق بين الكتل وتتم هذه العملية ضمن عدة خوارزميات أحداها خوارزمية الخطوات الثلاث للبحث عن المجاورات للكتل المراد مطابقتها مع الكتل التنبؤية حيث تبدأ بخطوات بحث اكبر من نصف خطوات البحث المستخدمة في الطرق السابقة وتكون آلية العمل كما يلي :

- تتم المقارنة مع تسع نقاط في كل مرة من خطوة البحث، ثلاثة نقاط في المركز وستة نقاط على الجوانب.
- تقل مساحة البحث من جانب واحد بعد كل خطوة ويتوقف البحث عندما يكون حجم مساحة البحث بكسل واحد.
- في كل خطوة بحث جديدة تتحرك مساحة البحث لإيجاد أفضل تطابق للمركز الكتلة عن البحث السابق ،الدوائر الزرقاء المتمثلة برقم واحد كما في شكل(9) تمثل الخطوة الأولى من الخطوات الثلاث وعند إيجاد اقل مجموع فروق مابين الكتلة الحالية والسابقة تبدأ الخطوة الثانية والمتمثلة بدوائر الخضراء وأيضا يتم البحث حول اقل مجموع فروق إلى أن يصل البحث إلى مستوى بكسل واحد المتمثل بدوائر البرتقالية والأخيرة تمثل نهاية البحث لهذه النظرية .



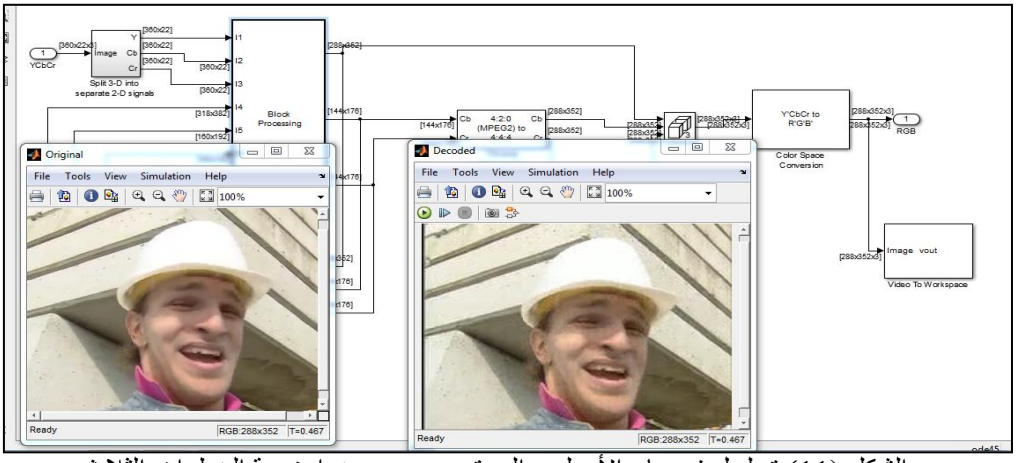
الشكل (9) نظرية الثلاث خطوات

ناقلات الحركة هي وسيلة بسيطة لنقل الكثير من المعلومات، ولكنها ليست دائما تعطي التطابق الكامل. لإعطاء أفضل جودة إعادة، يؤخذ ناتج الطرح مابين كتلة الإطار الأصلي والكتلة للإطار المتنبأ والناتج يشفر، عملية التشفير مشابه بالضبط لعملية تشفير (I-frame) لكن الاختلاف يكون في عملية التقريب ومن خلال النتائج العملية كما في الشكل (10) ووجد أن نسبة الضغط70%من الحجم الأصلي .



الشكل (10) دائرة تمثيل فك المشفر

في الشكل (11) يبين تشفير وفك التشفير لتسلسل فيديو فورمان ونلاحظ أن الصورة في حالة التشفير وفك التشفير تمتلك الخواص ذاتها



الشكل (11) تسلسل فورمان الأصلي والمسترجع ضمن خوارزمية الخطوات الثلاث

6- الاستنتاج

يعرض H.264 خطوة كبيرة إلى الأمام في مجال تكنولوجيا ضغط الفيديو. ويوفر التقنيات التي تمكن الكفاءة لضغط أفضل، نظرا لقدرات التنبؤ الأكثر دقة، فضلا عن تحسين القدرة على تقليل الأخطاء. أنه يوفر إمكانيات جديدة لخلق أجهزة تشفير الفيديو التي تمكن من الحصول على جودة عالية للفيديو وارتفاع معدلات الإطار خلال الثانية الواحدة ودقة أعلى في معدلات بت (مقارنة مع المعايير السابقة)، ومن خلال النتائج العملية لمحاكاة الماتلاب وجد أن نسبة ضغط البيانات خلال الوقت الحقيقي تصل إلى 70% من حجم الفيديو الأصلي ضمن زمن تنفيذ 261.89 s وأعلى قيمة يمكن الحصول عليها لنسبة الإشارة إلى الضوضاء تصل إلى 42db كما موضح في الشكل (12).

Simulink Profile Report: Summary

Report generated 14-Aug-2013 16:15:47

Total recorded time:	261.89 s
Number of Block Methods:	623
Number of Internal Methods:	5
Number of Model Methods:	9
Number of Nonvirtual Subsystem Methods:	71
Clock precision:	0.00000004 s
Clock Speed:	2501 MHz

To write this data as untitlednoorProfileData in the base workspace click here

Function List

Name	Time		Calls	Time/call	Self time	
simulate(untitlednoor)	261.89447880	100.0%	1	261.8944788000000	0.00000000	0.0%
simulationPhase	248.94639580	95.1%	1	248.9463958000000	4.10282630	1.6%
untitlednoor.Outputs.Major	242.37875370	92.5%	302	0.8025786546358	0.28080180	0.1%
untitlednoor/Encoder/Block Processing (AtomicSubSystem.Outputs.Major)	133.25605420	50.9%	301	0.4427111435216	0.04680030	0.0%
untitlednoor/Encoder/Block Processing/Block iterator (ForIteratorSubSystem.Outputs.Major)	133.20925390	50.9%	301	0.4425556607973	51.55833050	19.7%
untitlednoor/Decoder/Block Processing (AtomicSubSystem.Outputs.Major)	107.21948730	40.9%	301	0.3562109212625	0.00000000	0.0%
untitlednoor/Decoder/Block Processing/Block iterator (ForIteratorSubSystem.Outputs.Major)	107.20388720	40.9%	301	0.3561590936877	44.44468490	17.0%

H.264 هو من المتوقع أن يحل محل المعايير الضغط الأخرى والأساليب المستخدمة اليوم. كما أصبح شكل H.264 أكثر الأنواع المتاحة على نطاق واسع في، الكاميرات الشبكية، أجهزة تشفير الفيديو، الفيديو، إدارة البرامج، مصممي

الأنظمة في الوقت الحاضر، ومنتجات الفيديو الشبكية التي دعم كل H.264 و Motion JPEG هي مثالية لأقصى قدر من المرونة والإمكانيات التكامل.

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Hardware Implementation of Artificial Neural Network for Data Ciphering

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Abstract

This paper introduces the design and realization of multiple blocks ciphering techniques on the FPGA (Field Programmable Gate Arrays). A back propagation neural networks have been built for substitution, permutation and XOR blocks ciphering using Neural Network Toolbox in MATLAB program. They are trained to encrypt the data, after obtaining the suitable weights, biases, activation function and layout. Afterward, they are described using VHDL and implemented on Spartan-3E FPGA using two approaches: serial and parallel versions. The simulation results obtained with Xilinx ISE 9.2i software. The numerical precision is chosen carefully when implementing the Neural Network on FPGA. Obtained results from the hardware designs show accurate numeric values to cipher the data. As expected, the synthesis results indicate that the serial version requires less area resources than the parallel version. As, the data throughput in parallel version is higher than the serial version in rang between (1.13-1.5) times. Also, a slight difference can be observed in the maximum frequency.

Keywords: Back propagation, Ciphering, Encryption, FPGA, Neural Network

التنفيذ المادي للشبكة العصبية الاصطناعية المستخدمة لاغراض تشفير البيانات

مأمون عبد الجبار تقى أحمد فتحي سحر لازم قدوري

الخلاصة

يقدم هذا البحث التصميم و التنفيذ المادي لعدد من تقنيات التشفير متعدد الاجزاء على مصفوفة البوابات المبرمجة حقليا. لقد تم بناء شبكات عصبية و تدريبها بطريقة الانتشار العكسي لكل من التشفير الابدالي و التعويضي و التشفير بطريقة XOR باستخدم صندوق العدة للشبكات العصبية المتوفرة في برنامج ال MATLAB. دربت هذه الشبكات لتشفير البيانات بعد الحصول على الاوزان والتخطيط و دوال التفعيل المناسبة. تم استخدام الشبكات المدربة لبناء كيان مادي بواسطة لغة وصف الكيان المادي VHDL و طبقت على اداة مصفوفة البوابات المبرمجة حقليا ال Spartan-3E باستخدام منهجيتين هما المتسلسلة والمتوازية. تم الحصول على نتائج المحاكاة بواسطة برنامج ISE 9.2i. انّ الدقّة العددية استخدمت بعناية عندما طبّقت الشبكة العصبية على FPGA. حيث ان النتائج المستحصلة من التصميم المادي تظهر قيم عددية دقيقة لتشفير البيانات. كما هو متوقّع، تشير نتائج التمثيل بأنّ المنهجية المتسلسلة تحتاج الى مساحة اقل من المنهجية المتوازية. كما ان إنتاجية البيانات بالمنهجية المتوازية أعلى من المنهجية المتسلسلة بمقدار (1.13-1.5) مرة. كما ويلاحظ وجود إختلاف طفيف في التردد الأقصى بين المنهجيتين.

1. Introduction

The problem of protecting information has existed since information has been managed. However, as technology advances and information management systems become more and more powerful, the problem of enforcing information security also becomes more critical. The massive use of the communication networks for various purposes in the past few years has posed new serious security threats and increased the potential damage that violations may cause. A violation to the security of the information may jeopardize the whole system working and cause serious damages. Advances in artificial neural networks (ANNs) provide effective solutions to this problem [1].

Artificial Neural Network can be defined as "a parallel, distributed information processing structure consisting of processing elements (which can possess local memory and can carry out localized information processing operations) interconnected via unidirectional signal channels called connections". ANN becomes more and more popular in the Artificial Intelligence (AI) field these decades since it can be used for security network, image processing, pattern recognition, fingerprint analysis and many other problems' solving.

Nowadays, feed forward ANN has the widest and most comprehensive application among all the ANN models. Back propagation Neural network (BPNN) is a typical feed forward structure. Nonetheless, there are no definite rules for the choice of how many hidden layers and neurons, no promising convergence and it may take very long time for the iterative training procedures [2].

There are different kinds of electronic implementations of ANN: digital, analog, hybrid, and each one have specific advantages and disadvantages depending on the type and configuration of the network, training method and application. For digital implementations of ANN there are different alternatives: custom design, digital signal processors, and programmable logic. Among them, programmable logic offer low cost, powerful software development tools and true parallel implementations. Field programmable gate arrays (FPGA) are a family of programmable logic devices based on an array of configurable logic blocks (CLB), which give a great flexibility in the development of digital ANNs [3].

The paper focuses on realizing the neural network for multiple blocks ciphering techniques on the FPGA (Field Programmable Gate Arrays). A back propagation neural networks have been trained for substitution, permutation and XOR blocks cipher to encrypt the data, after obtaining the suitable weights, biases, activation function, and layout.

This paper is organized as follows: Section 2 displays much work has focused on implementing artificial neural networks on FPGA to solve the security problems. Section 3 consists of the ciphering blocks which will be implemented in this paper. Section 4 introduces the overview of artificial neural network. Section 5 contains the simulation of neural network for blocks ciphering, which are explained in section 3, using MATLAB program. Section 6 presents an FPGA implementation of the neural network for blocks ciphering where, the implementations are done in parallel and serial manners. Section 7 shows the results of parallel and serial versions for hardware implementations. Finally, conclusions are illustrated in section 8.

2. Related Works

Recently, much work has focused on implementing artificial neural networks on reconfigurable computing platforms to solve the security problems. Reconfigurable computing is a means of increasing the processing density above and beyond that provided by general-purpose computing platforms. Field Programmable Gate Arrays (FPGAs) are a medium that can be used for reconfigurable computing and offer flexibility in design like software but with performance speeds closer to Application Specific Integrated Circuits (ASICs) [4]. Some of these works are arranged as follows:

In 2007, B. Chandra el at. [5] discussed the possibility of employing Neural Networks for identification of Cipher Systems from cipher texts. Cascade Correlation Neural Network and Back Propagation Network have been employed for identification of Cipher Systems. Very large collection of cipher texts were generated using a Block Cipher (Enhanced RC6) and a Stream Cipher (SEAL). Promising results were obtained in terms of accuracy using both the Neural Network models but it was observed that the Cascade Correlation Neural Network Model performed better compared to Back Propagation Network.

In 2008, S. Sadeghian el at. [6] described an innovative form of cipher design based on the use of recurrent neural networks. The proposed cipher had a relatively simple architecture and, by incorporating neural networks, it released the constraint on the length of the secret key. The design of the symmetric cipher was described in detail and its security was analyzed. The cipher was robust in resisting different cryptanalysis attacks and provides efficient data integrity and authentication services. Simulation results were presented to validate the effectiveness of the proposed cipher design.

In 2009, M.B. Abdelhalim el at. [7] approved a modified implementation of Rijndael AES encryption standard based on the fact that any FPGA includes built in memory block; therefore they stored all the results of the fixed operations within the memory modules. The modification gave an 11% reduction in area and 25% increase in speed (Throughput) compared with the original design. Their design gave the highest throughput and area utilization over all the Iterative Looping based FPGA implementations.

In 2010, G.Sivagurunathan el at. [8] deliberated classical substitution ciphers, namely, Playfair, Vigenère and Hill ciphers. The features of the cipher methods under consideration were extracted and a back-propagation neural network was trained. The network was tested for random texts with random keys of various lengths. The cipher text size was fixed as 1Kb. The results so obtained were encouraging.

In 2011, Siddeeq. Y. Ameen el at. [9] attempted to implement Rijndael AES cryptosystem using ANN. In the design of the NN performs encryption and decryption processes using of symmetric key cipher. The key used in both encryption and decryption processes was the initial weights for neural network and then trained to its final weight with a fast and low cost algorithm, such as Levenberg – Marquardt Algorithm. The final weights of neural network represented the final key that can be used for encryption and decryption

processes. Simulation results showed the closeness of the results achieved by the proposed NN-based AES cryptosystem with that of the normal AES.

In 2012, Khaled Alallayah et al. [10] discussed the methods of block Simplified DES (SDES) crypto systems. They constructed a Neuro-Identifier mode to achieve two objectives: the first one is to emulate construction Neuro-model for the target cipher system, while the second is to (cryptanalysis) determine the key from given plaintext-ciphertext pair.

3. Ciphering Blocks

With the advent of the computer, ciphers need to be bit-oriented in addition to character-oriented. This is so because the information to be encrypted is not just text; it can also consist of numbers, graphics, audio, and video data. It is convenient to convert these types of data into a stream of bits, encrypt the stream, and then send the encrypted stream. In addition, when text is treated at the bit level, each character is replaced by 8 (or 16) bits, which means the number of symbols becomes 8 (or 16). A modern symmetric cipher is a combination of simple ciphers. In other words, a modern cipher uses several simple ciphers to achieve its goal. These simple ciphers first will be discussed [11].

3.1 XOR Cipher

One of ciphering blocks is called the **XOR cipher** because it uses the exclusive-or operation. Figure 1 shows an XOR cipher.

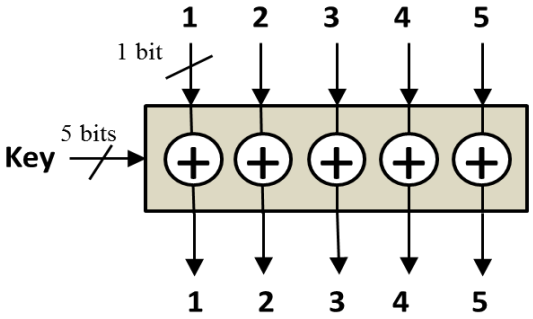

Figure 1 XOR cipher

An XOR operation needs two data inputs plaintext, as the first and a key as the second. In other words, one of the inputs is the block to be the encrypted, the other input is a key; the

result is the encrypted block. In an XOR cipher, the size of the key, the plaintext, and the cipher text are all the same. XOR ciphers have a very interesting property: the encryption and decryption are the same. This encryption technique is appropriate for binary signals and it encrypts each pixel (bit) individually [12].

3.2 Substitution Cipher: S-box

The input to an S-box is a stream of bits with length *N;* the result is another stream of bits with length *M.* So, N and *M* are not necessarily the same. Figure 2 shows an Example of S-box.

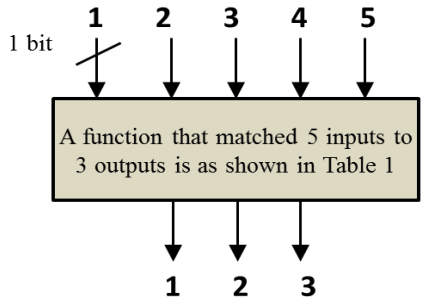

Figure 2 an example of S-box

The S-box is normally keyless and is used as an intermediate stage of encryption or decryption. The function that matches the input to the output may be defined mathematically or by a table [11].

Thus ***S-box*** which is applied in this paper is the function defined in Table 1 and the output of this ***S-box*** is determined as follows:

The first and last bits of ***input bits*** represent in base 2 a number in the range 0 to 3. Let that number be *i*. The middle 3 bits of ***input bits*** represent in base 2 a number in the range 0 to 8. Let that number be *j*. Look up in Table 1 the number in the *i*'th row and *j*'th column. It is a number in the range 0 to 8 and is uniquely represented by a 3 bit block. That block is the output of ***S-box***. For example, for input 01011 the row is 01, that is row 1, and the column is determined by 101, that is column 5. In row 1 column 5 appears 5 so that the output is 101 [13, 14].

Table 1 an example of S-box function

	Column No.							
Row No.	1	2	3	4	5	6	7	8
1	0	5	1	6	5	7	6	0
2	0	3	3	5	4	0	6	7
3	1	0	2	0	3	4	7	4
4	4	3	3	0	0	6	3	4

3.3 Transposition Cipher: P-box

A P-box (permutation box) is for characters and for bits parallels. For characters, their locations are changed, for example, a character in the first position of the plaintext may appear in the tenth position of the cipher text. A character in the eighth position may appear in the first position. In other words, a transposition cipher reorders the symbols in a block of symbols. For bits parallels, it transposes bits. Two types of permutations can have in P-boxes: the **straight permutation and expansion permutation** as shown in Figure 3.

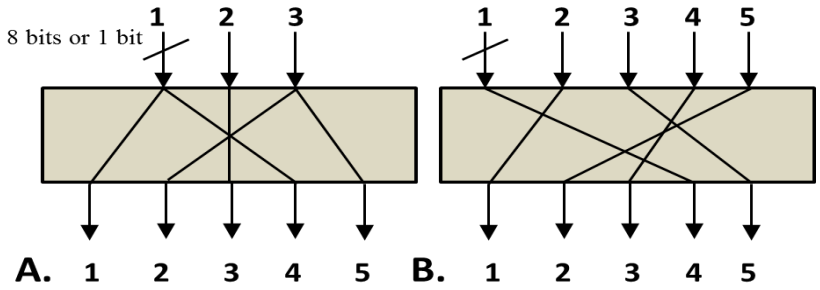

Figure 3 P-box A. expansion permutation B. straight permutation

A straight permutation cipher or a straight P-box has the same number of inputs as outputs. In other words, if the number of inputs is *N*, the number of outputs is also *N*. In an expansion permutation cipher, the number of output ports is greater than the number of input ports [11].

4. Artificial Neural Networks

An Artificial Neural Network (ANN) is an information processing paradigm that is inspired by the way biological nervous systems process information. An interesting feature of the ANN models is their intrinsic parallel processing strategies. However, in most cases, ANN is implemented using sequential algorithms that run on single processor architecture, and does not take advantage of the inherent parallelism. Another important feature of an artificial neural network is its ability to be learned by examples. Every time a neural network is made, training is needed to 'teach' it to give a specific output if a specific input is given [15].

One of the most useful algorithms of ANN training is back propagation network that uses back propagation learning algorithm. Back propagation (or back prop) algorithm is one of the well-known algorithms in neural networks. The back propagation neural network is essentially a network of simple processing elements working together to produce a complex output. These elements or nodes are arranged into different layers: as shown in Figure 4 [1, 3]:

- Input layer propagates a particular input vector's components to each node in middle layer.
- Middle layer nodes compute output values, which become inputs to the nodes of output layer.
- The output layer nodes compute the network output for the particular input vector.

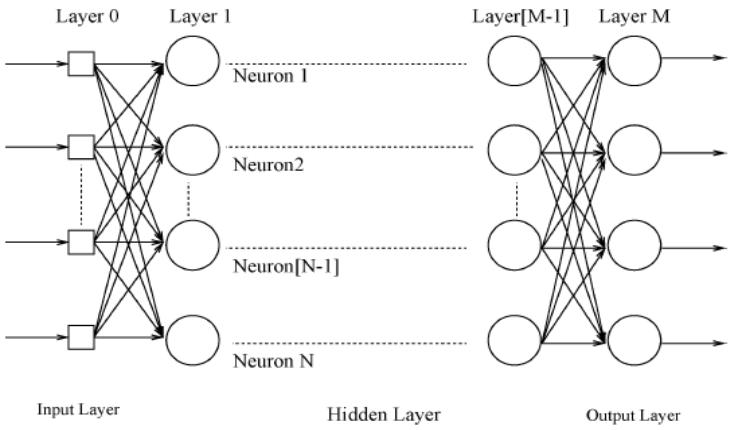

Figure 4 Back propagation architecture

5. Simulation of Ciphering System

Multilayer back-propagation neural networks are used to simulate the blocks ciphering that are explained in section 3; the data set has been used with different inputs length. The neural network used in the encryption process is a 3-layer feed-forward network implementing the back propagation algorithm. The number of neurons each layer are shown in Table 2. Neural Network Toolbox in MATLAB program is used to implement the neural network for blocks ciphering. Training was conducted until the mean square error MSE fell below e-20 or reached a maximum iteration limit of 10000 as shown in Figure 5. The mean square error denotes the error limit to stop NN training. The MSE is the average of NN target output subtracted by the desired target output from all the training patterns. Two training algorithms are used; the *traingdx* which updates weight and bias values according to gradient descent momentum and an adaptive learning rate, the second is *trainlm* which is a network training function that updates weight and bias states according to Levenberg-Marquardt optimization. The output layer activation function is the pure line activation function. In the learning process, one thousands of data set are used to train the neural network.

Table 2 summary of simulation results of ciphering system in MATLAB

Cipher Block	Length of each inputs in bits	No. of inputs	No. of Hidden layer neurons	No. of outputs	Activation function of hidden layer	Training algorithm
Straight 1-bit	1	5	5	5	Pure line	traingdx
Straight 8-bits	8	5	5	5	Pure line	traingdx
Expansion 1-bit	1	3	3	5	Pure line	traingdx
Expansion 8-bits	8	3	3	5	Pure line	traingdx
S-box	1	5	10	3	Log sigmoid	trainlm
XOR	1	5	10	5	Log sigmoid	trainlm

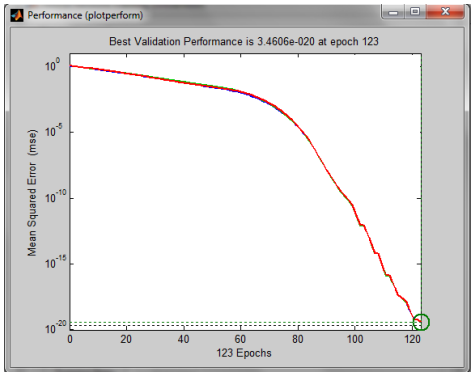

Figure 5 the training process: the number of epochs with the MSE

6. FPGA Realization of Ciphering System

According to the normal structures of Neural Network, the hardware implementation is grander to the software approach because it can yield improvement of ANN's features, especially parallelism. Moreover, FPGA is a digital device with reconfigurable properties and flexibility. The back propagation neural networks for multiple blocks ciphering are implemented in this paper using one of the largest Xilinx FPGA devices, SPARTAN-3E, XC3S500E. This device has a capacity of (4656) logic slices and can operate at a maximum clock speed of 50MHz.

For the ANN implementation, fixed point computations with two's complement representation and different bit depths are chosen for the stored data (inputs data, weights, outputs, activation function, etc). It is necessary to limit the range of different variables:

- The length of inputs data depend on the type of block cipher as indicated in table 2 (1 or 8 bits are chosen)
- The length of each Weight is 16 bits (5 for integer part and 11 for fraction part).
- The length output from adder and multiplier, and activation function depend on the layer (hidden or output) and the type of block cipher shown in table 2.

The design is characterized by the hardware description language VHDL as neural network architecture, finally the output of the neural network architecture passes through the output layer. The internal structure of each hardware neuron is composed of set of adders and multipliers to get the cumulative sum of the inputs multiplied by their weights and added to the bias of that neuron. The final cumulative sum then processed by the activation function of that neuron. In the following subsections, both a serial and a parallel version of the ANN architecture are described for 8-bit straight block cipher, the characteristics of this block cipher are shown in table 2.

6.1 Parallel Version

The parallel architecture describes a kind of 'node parallelism', in the sense that it requires one hardware unit per neuron when working at a determined layer. With this strategy, all the neurons of a layer work in parallel and therefore get their outputs simultaneously. This

is not a fully parallel strategy because the outputs for different layers are obtained in a serial manner.

Since the data transmission between layers is serial, every functional unit will also need some local storage for output data. The data in the parallel registers are introduced to the single activation unit. The output of the activation unit is either used as output of the neurons in hidden layer or it is stored in the output array RAM.

For the 8-bit straight block cipher, where 5 neurons exist at a hidden layer and 5 at the output layer, 5 hardware units are required. All hardware units will work in parallel when computing the outputs of the hidden layer, and the same ones will work when the output layer is computed. Given that all hardware units work in parallel for each input data, they need access to the associated weights simultaneously, and hence, the weight arrays RAM should be private for each neuron. For this reason, the 3-bit counter is used to address 5 arrays RAM for each layer. The parallel structure of the 8 bit straight block cipher is shown in figure 6.

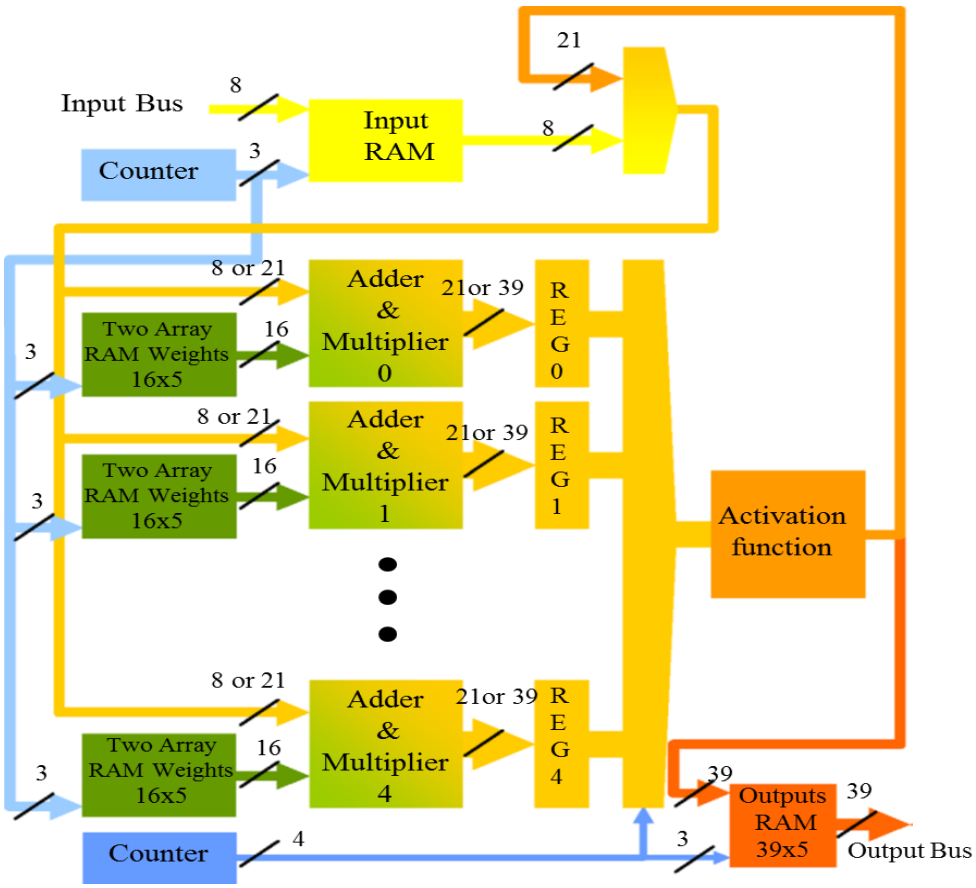

Figure 6 the structure of the parallel neural network

6.2 Serial Version

The serial architecture has been designed to estimate the minimum area required to implement the ANN, although this implies a large execution time. Therefore, this serial version of the ANN consists in a single hardware neuron unit that carries out all the computations for every the neuron. The inputs of the hardware neuron unit are both the input

data (plaintext) and their associated weights, which have been stored in separate array RAM. There is a number of array RAM to store the weights for each neuron, the number of these array RAM depend on the number of neurons at hidden and output layers in each block cipher. In addition, two separate ones to store the output of neuron in hidden and output layers. By separating the array RAM, the ANN will be able to read from the array RAM associated with input layer and to write the output of the hidden neurons in the same clock cycle. The activation function output is stored either in the hidden array RAM or in the output array RAM, depending on the layer of the computed neuron.

The addressing arrays RAM have been carried out by two 3-bit counters. The first 3-bit counter addresses the arrays RAM when reading them, and the second 3-bit counter addresses them when arrays RAM writing. The 6-bit address of the weights arrays RAM is computed by merging the addresses of two 3-bit counters. Figure 7 shows the structure of the serial version for the straight 8 bit block cipher shown in table 2.

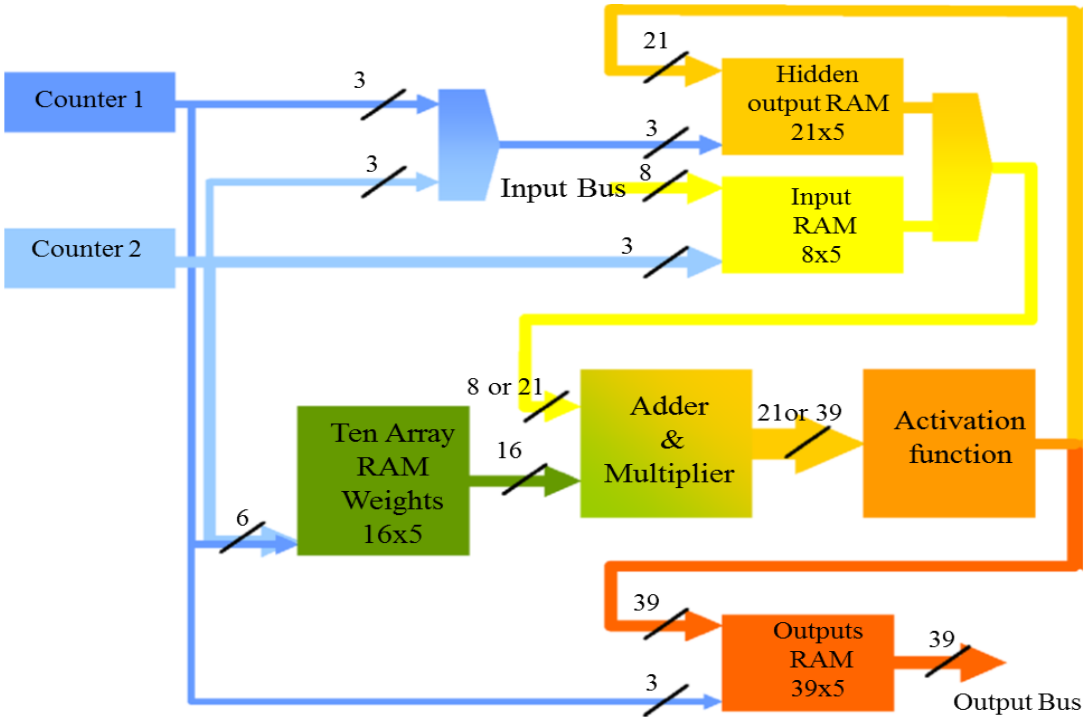

Figure 7 the structure of the serial neural network

7. Results

After designing the neural networks, the testing shows that the NNs can be used actively as a tool for data ciphering. In the other hand, the hardware design of the networks gives a low error rate when comparing the numeric values with those obtained in software. Table 3 shows a comparison among real, MATLAB and FPGA numeric values for different ciphering techniques.

Tables 4 and 5 show the implementation results obtained after synthesizing both serial and parallel versions of the ANN for multiple blocks cipher. The results of each

implementation can be characterized by the same parameters like (number of slices, maximum no. of clock, etc.) in order to make comparisons between the different implementations easier. As expected, results indicate that the serial version, with only a hardware unit, requires less area resources than the parallel one, where a hardware unit per hidden neuron was included. In the parallel version, the data throughput is higher than the serial version rounding (1.13-1.5) times, mostly due to the reduced number of clock cycles needed for each input data evaluation. After synthesizing the design, a slight difference can be

observed in the maximum clock frequency, this is due to the different maximum combinational paths of the two approaches.

Table 3 comparisons among real, MATLAB and FPGA results for different block ciphering techniques

Cipher block	Real values	MATLAB values	FPGA values	Cipher block	Real values	MATLAB values	FPGA values
Straight 1-bit	0	-0.000044	-0.00012	Straight 8-bits	204	204.0003	203.9930
	1	1.0001	1.0001		234	234.0003	233.9879
	0	-0.000054	-0.00006		107	106.9993	107.0052
	1	0.99983	0.9997		124	124.0006	123.9846
	1	0.99988	0.9998		36	35.99945	35.9879
Expansion 1-bit	1	1.000006	1	Expansion 8-bits	17	16.9985	17
	1	1.000006	1		221	221.0048	221
	0	-0.000019	0		148	148.004	147.9926
	1	1.000006	1		17	16.9985	17
	1	1.000006	1		221	221.0048	221
S-box	1	1.000003	0.9883	XOR	1	0.999992	0.9733
	0	0	0		1	1.000042	0.9688
	0	0	0		1	0.99994	0.9420
					0	0.000011	-0.0097
					0	-0.000004	-0.0300

From table 4, it can be seen that the straight block cipher method use all the available multipliers of the Spartan-3E FPGA, the other methods use less number of the available multipliers. In the parallel structure of the neural network, the output of each layer is available in the same clock, this give a high throughput for the input and hidden layers. The final output takes more clock cycles because each output neuron needs one clock cycle to be read from the output array RAM.

From table 5, it can be noted that XOR and S-box block cipher require large resources area because they have great numbers of neurons in their structures shown in table 2. In the serial structure of the neural network, the output of each neuron of each layer is available in the one clock, this give a less throughput for layer one and the hidden layer. As, the final output for each neuron in the output layer take one clock cycle to be read from the output

array RAM. Table 6 shows the speed up ratio for the blocks cipher which are designed in parallel and serial version.

Figure 8 shows the time diagram of the parallel implementing for an 8-bit straight ciphering block. While, figure 9 shows the time diagram of the serial implementing for an 8-bit expansion ciphering block.

Table 4 the obtained results of FPGA resources for multiple blocks cipher using the parallel implementation

	Straight 1-bit		**Straight 8-bit**		**Expansion 1-bit**		**Expansion 8-bit**	
Logic Utilization	Used	Utilization	Used	Utilization	Used	Utilization	Used	Utilization
Number of Slices	325	6%	315	6%	205	4%	178	3%
Number of Slice Flip Flops	78	0%	78	0%	78	0%	78	0%
Number of 4 input LUTs	629	6%	609	6%	392	4%	344	3%
Number of MULT18X18SIOs	20	100%	20	100%	12	60%	12	60%
Number of GCLKs	1	4%	1	4%	1	4%	1	4%
Maximum Frequency (MHz)	46.640		46.491		61.712		61.448	
Maximum No. of clocks	7		7		7		7	
Throughputs (Mb/s)	259.8514		259.0213		343.824		342.3531	

Table 5 the obtained results of FPGA resources for multiple blocks cipher using the serial implementation

	Straight 1-bit		**Straight 8-bit**		**Expansion 1-bit**		**Expansion 8-bit**		**S-box**		**XOR**	
Logic Utilization	Used	Utilization	Used	Utilization	Used	Utilization	Used	Utilization	Used	Utilization	Used	Utilization
Number of Slices	188	4%	184	3%	131	2%	104	2v	401	8%	385	8%
Number of Slice Flip Flops	85	0%	85	0%	84	0%	84	0%	45	0%	114	1%
Number of 4 input LUTs	323	3%	317	3%	208	2%	160	1%	787	8%	753	8%
Number of MULT18X18SIOs	10	50%	10	50%	6	30%	6	30%	15	75%	13	65%
Number of GCLKs	1	4%	1	4%	1	4%	1	4%	1	4%	1	4%
Maximum Frequency (MHz)	48.940		49.202		61.866		69.897		30.461		30.487	
Maximum No. of clocks	11		11		9		9		14		16	
Throughputs (Mb/s)	173.5145		174.4435		268.086		302.887		97.91036		85.74469	

Table 6 speed up ratio for multiple blocks cipher

	Straight 1-bit	Straight 8-bit	Expansion 1-bit	Expansion 8-bit
Speed up Ratio	1.5714	1.5714	1.285	1.285

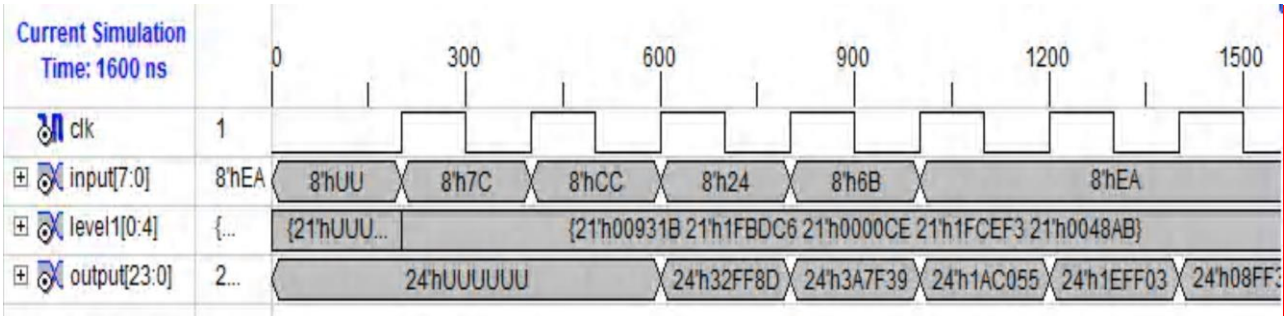

Figure 8 Time diagram of the parallel implementing for an 8-bit straight ciphering block

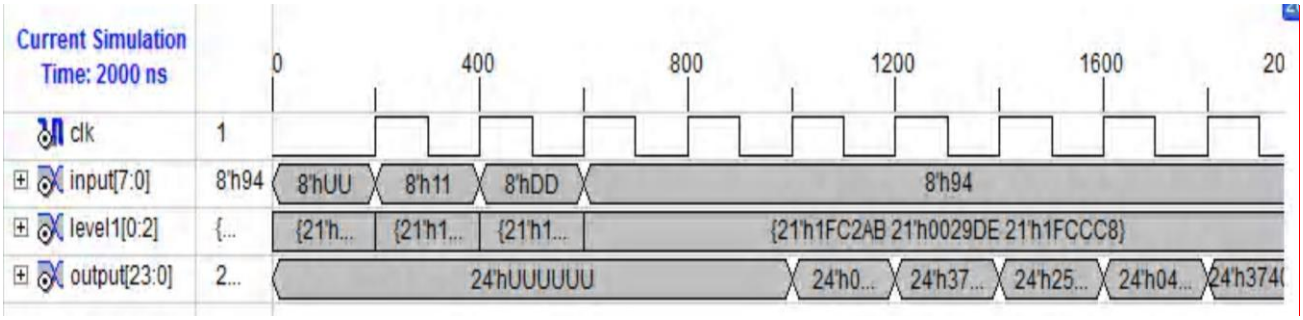

Figure 9 Time diagram of the serial implementing for an 8-bit expansion ciphering block

8. Conclusions:

Artificial neural networks have been trained to act as a cryptography system. Different block ciphering techniques have been realized using ANNs. The NNs have been described in VHDL and implemented on the FPGAs using two approaches: serial and parallel versions. Implementing the cryptography system on FPGA makes it faster, reliable and the method of ciphering can be changed easily by altering the weights of the neurons. The numerical precision have been chosen carefully when implementing the ANN on FPGAs. Higher precision gives more accurate results but takes more FPGA resources. Obtained results from the hardware designs have shown accurate numeric values to cipher the data. As expected, the results indicate that the serial version, with only a hardware unit, requires less area resources than the parallel one. As, the data throughput in parallel version is higher than the serial version in rang between (1.13-1.5) times. Also, a slight difference can be experimental in the maximum frequency.

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Modeling and Performance Analysis of (HEMT) Transistors Based on GaN and GaAs Using Silvaco Software

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Abstract

The gallium nitride high electron mobility (HEMT) is showing great promises as the enabling technology in the development of military radar systems, electronic and communication system. This paper aims to model and perform analysis for Gallium Nitride (GaN) and Gallium Arsenide (GaAs) High Electron Mobility Transistor (HEMT) Semiconductors. The model was set up with dimensions to match the physical device using (8 micron) width and a (1 micron length) with (1 micron channel length). Doping level represent uniform (n. type) concentration (1e14 / Cm^3) and (T=300 K) for both models.

A computer model is created with the commercially available Silvaco software package for an AlN/ GaN and GaAS/AlGaAs HEMT, has been designed for the purpose of studying (Id-Vd) and (Id-Vg) further more (C-V) characteristics with different gate biasing voltage. The drain, gate and substrate currents were calculated for the designed structure. It is found that the drain current of GaN transistors is (0.24 A) while it is (0.0024 A) for GaAs at same drain source voltage. The output power for GaN about (1.2W) while it is (0.012W) for other one, which represents (100 times) larger than that of GaAs. Finally its very clear that transistors structured by GaN material gives good specification to operate as a perfect material could be depended to build high power and high frequency for future telecommunication requirements.

نمذجة وتحليل أداء ترانسستر (HEMT) المبني على GaN and GaAs باستخدام برامجيات سيلفاكو

الملخص

ان ترانزستورات التحركية العالية للالكترون لمادة نتريد الكاليوم اظهرت ميزات كبيرة لتكنولوجيا تطوير انظمة الرادار العسكرية والانظمة الالكترونية وانظمة الاتصالات. يهدف البحث الى نمذجة وتحليل اداء لترانزستورات اشباه الموصلات المبنية من مادتي نتريد الكاليوم وارسنايد الكاليوم المعتمدة على تقنية التحركية العالية للالكترون. النموذج صمم بابعاد (8 مايكرون للعرض) و (1 مايكرون للطول) وطول قناة بمقدار (1 مايكرون). ان مستوى التطعيم من نوع التركيز المنتظم للمانحات (n. Type) وبمقدار (1 e14/cm^3) عند درجة حرارة (300 كلفن).

تم عمل نموذج بواسطة برمجيات (Silvaco) النسخة التجارية، لعمل نموذجين احدهما يتكون من مادتي (AlN/GaN) والاخر من (GaAs/AlGaAs) تم تصميمهما لدراسة خواص كل من تيار المصرف مع فولتية المصرف وفولتية البوابة، اضافة الى خواص الفولتية مع المتسعة ولقيم فولتية بوابة مختلفة. في هذا البحث تم حساب تيارات المصرف والبوابة والركيزة (Substrate)، وذلك بسبب تأثيرها المباشر على عمل النموذج. اوضحت الدراسة بان تيار المصرف يزداد بصورة طردية الى اعلى قيمة (0.24A) ، لنموذج نتريدكاليوم بينما كانت قيمته (0.0024A) عند نفس فولتية المصدر لنموذج ارسنايد الكاليوم. اما بالنسبة للقدرة الخارجة لكل نموذج فقد كانت (1.2W) لنتريد الكاليوم مقابل (0.012W) لارسانيد الكاليوم، اي ان القدرة الخارجة للنموذج الاول اكبر بمقدار (100 ضعف) عن النموذج الثاني، مما سبق اعلاه فأن مادة نتريد الكاليوم تتمتع بمواصفات جيدة لبناء ترانزستورات يمكن اعتمادها في مجال القدرة والترددات العالية في علم الاتصالات.

1. Introduction

Silicon based semiconductor devices are rapidly reaching the theoretical boundary of operation and are becoming unsuitable for future communication requirements. The scope of semiconductor devices has been expanded by wide band gap devices such as Gallium Arsenide (GaAs) and gallium nitride (GaN) to include the possibility of high power and high frequency operation [1].

Gallium Arsenide MOS transistors have long been employed as the technology of choice for high power PAs due to excellent cost and performance ratios in modern base station and repeater systems [2]. But as the limits of operability of these devices are reached, there will be a need for a semiconductor material that can fulfill the high frequency and high power requirements. Interest today is gallium nitride (GaN) HEMTs as one of promising candidates for high power RF applications. GaN HEMT transistors exhibit very high power densities, high electron saturation velocity, high operating temperature, and high cutoff frequency compared with any other technologies [3,4].In this paper three types of current are simulated (drain, gate and substrate currents), furthermore three primary capacitors (gate-source, gate-drain, source-drain capacitance) for the two models.

2. Device Characteristics

To predict the channel potential 1-D Poisson's equation could be written as:

$$\frac{d^2\psi(y)}{dy^2} = -\frac{q}{\varepsilon_s}Nd \quad (1)$$

Where $\psi(y)$ is the potential distribution in (y) direction, q, the electron charge, $\boldsymbol{\varepsilon_s}$,material permittivity, Nd, doping concentration in the channel. This differential equation can be solved numerically under specified boundary conditions:

$$\psi(0) = Vgs - Vbi \quad (2a)$$
$$d\psi(y)/(dy)|(y = h) = 0 \quad (2b)$$
$$\psi(h) = V(x) - \Delta \quad (3b)$$

Where Vbi is the built-in potential, Vgs the gate-source voltage, V(x), the channel potential voltage at any point (x), h, is the distance from surface to the edge of gate depletion region, and (Δ), the depth of Fermi-level below the conduction band in the undepleted channel region is illustrated in the figure below[6].

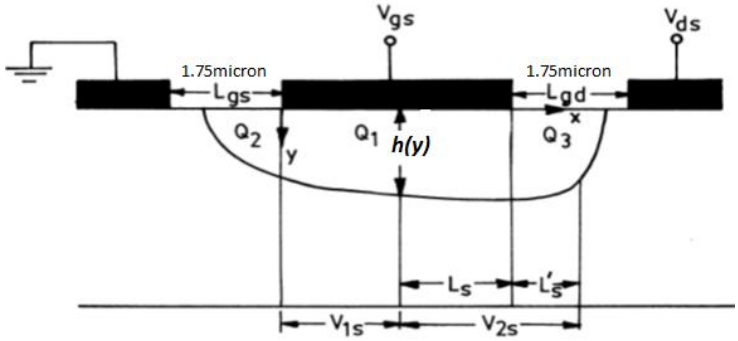

Figure (1): Depletion region Extension

2.1. I-V Characteristics

The linear region of the channel under gate contains drain-source current which affected mainly by source and drain resistances expressed as:

$$\int_0^L I_{ds}\ dx = qZ\mu \int_{I_{ds}\ Rs}^{Vds-Ids\ Rd} Nd(a-h)dV \quad (3a)$$

$$I_{ds} = \frac{qZ\mu\ Nd\ a}{L}\left(\left(Vds - Ids(\ Rs + Rd\ ) - \frac{2}{3V_P^{1/2}}\ [\ (\ Vbi - Vgs + Vds - I_{ds}R_d\ )^{3l2}]\right)\right) \quad (3b)$$

Where I_{ds} is the drain-source current, $\mu$the electron mobility, a, the active channel thickness, L and Z, the gate length and width respectively, Vds, the applied drain-source voltage, Rs and Rd the parasitic source and drain resistances, and Vp, the pinch off voltage[7].

Silvaco software solve the above equations to get the value of current, according to the considered values of (Rs and Rd).

At higher drain-source voltage, the electric field in the conducting channel increased which leads to velocity saturation. There is substantial extension of the depletion region beyond the gate forming high field region at the drain side of the channel.

To model this high field region, silvaco software consider the gate length modulation effect and the potential in this region calculated from (2-D Laplas equation). 2-D potential ((x, y) in the high region, keeping only the first term of the series as shown below:

$$\psi(x,y) = \frac{2a}{\pi}\ Es\ Cos\left(\frac{\pi y}{2a}\right)\ Sinh\ \left(\frac{\pi(x-L)}{2a}\right) \quad (4)$$

Where $Es = \frac{V_{sat.}}{\mu}$ is the velocity saturation field with, $V_{sat.}$ As the saturation velocity.

2.2. C-V Characteristics

The capacitance-voltage (C-V) characteristic is one of the important electrical properties. It includes the information of charge in the device. In this model, internal device capacitances are calculated on the basis of simplified charge distribution under the gate [8].

Mathematically, it can be written as:

$$Cgs = \left|\frac{\partial Q1}{\partial Vs}\right| + \left|\frac{\partial Q2}{\partial Vs}\right| + \left|\frac{\partial Q3}{\partial Vs}\right| \quad (5)$$

Where Q1, Q2, and Q3 are internal space charge distributions, as shown in Fig.(1), and the above expression calculated at gate-drain potential (V_{gd}) constant.

$$Q1 = \frac{q\ Z\ Nd\ a\ L}{2}\left(\left(\frac{Vbi-Vg+Vs}{Vp}\right)^{1/2} + \left(\frac{Vbi-Vg+Vd}{Vp}\right)^{1/2}\right) \quad (6)$$

$$Q2 = \frac{\pi}{4}(\ q\ Z\ Nd\ a^2)\left(\frac{Vbi-Vg+Vs}{Vp}\right) \quad (7)$$

$$Q3 = \frac{\pi}{4}(\ q\ Z\ Nd\ a^2)\left(\frac{Vbi-Vg+Vd}{Vp}\right) \quad (8)$$

Where Vs, Vg, and Vd are source, gate and drain potentials, respectively. Substituting above equations in Eq.(5), one obtains:

$$Cgs = \frac{Z\,L}{2\sqrt{2}}\left(\frac{q\,\varepsilon_s\,Nd}{Vbi-Vgs}\right)^{1/2} + \frac{\pi}{2}\varepsilon_s\,Z \quad (9)$$

$$Cgd = \frac{Z\,L}{2\sqrt{2}}\left(\frac{q\,\varepsilon_s\,Nd}{Vbi-Vgd}\right)^{1/2} + \frac{\pi}{2}\varepsilon_s\,Z \quad (10)$$

C-V characteristics can be measured using quasi-static C-V or split C-V technique. The difference between two methods is in the applied test frequency. In quasi-static C-V measurement, test frequency is very low and can be regarded as quasi DC signal. In the case of device which has slow charge response, quasi-static C-V method is useful to characterize its low mobility charge behavior.

The split C-V measurement has been developed to study interface states in weal inversion and mobility extraction. It measures capacitance between the gate and source-drain (Cgs, Cgd) and the capacitance between the gate and the substrate of the device [5].

A good C-V model is essential from microwave application point of view. Hence in the present model, Silvaco software used empirical relations for Cgs and Cgd to provide the best compromise between accuracy, flexibility and savings (CPU) execution speed, the supposed empirical relations are used and are given as [6][9]:

$$Cgs_{(emp.)} = Cgso\left(\frac{e^{A1*Vgs}+B1\,(Vgs+Vds)*10^{C1*(Vgs+Vds)}}{1+D1(Vgs*10^{C1*Vgs})}\right) \quad (11)$$

$$Cgd_{(emp.)} = Cgdo\left(\frac{e^{A2*Vds}+B2\,(Vds+Vgs)*10^{C2*(Vgs+Vds)}}{1+D2(Vds*10^{C2*Vds})}\right) \quad (12)$$

Where $Cgso$ and $Cgdo$ are device capacitances at Vgs = Vds = 0V and can be obtained from Eq.(9) and (10). The parameters (A-D) are fitting parameters, which control the variation of capacitances with bias.

3. Modeling Structure Processes

The following steps are essential to make a transistor model based on Lombardi CVT model and Schockley Read Hall (SRH model) by silvaco software.

1. Set grid dimensions. First step in the modeling process, specifying the model dimensions using (X,Y mesh commands).

x. mesh loc= - 4 spac = 0.5 y. mesh loc = - 0.005 spac = 0.001

2. Determine regions number. Meaning different material types and its deposition boundaries as illustrated in the table below.

Table (1): Deposition boundaries for each needed material in Silvaco software.

Region No.	Material Type	Ymin(Micron)	Ymax(Micron)
1	SiO_2	0	0
2	GaN	0	0.005
3	AlN	0	0.1
4	GaN	0.01	1.0

3. Define model parts locations. electrode command is used to define the location of gate, Source and drain.

Electrode name = source x.min = - 4 x.max = - 2.25 y.min = - 0.005 y.max = 0.01

Electrode name = gate x.min = - 0.5 x.max = 0.5 y.min = - 0.005 y.max = 0.01
Electrode name = drain x.min = 2.25 x.max = 4 y.min = - 0.005 y.max = 0.01

4. Mobility model. It's very common in (MOS) model to use (Lombardi CVT model) for non-planer devices, furthermore the Shockley Read Hall (SRH) model used to represent carrier generation-recombination process, which should be used in most simulation conditions to fix minority carrier life time[5].

The schematic structure for GaN and GaAs HEMT is shown in figure (2).

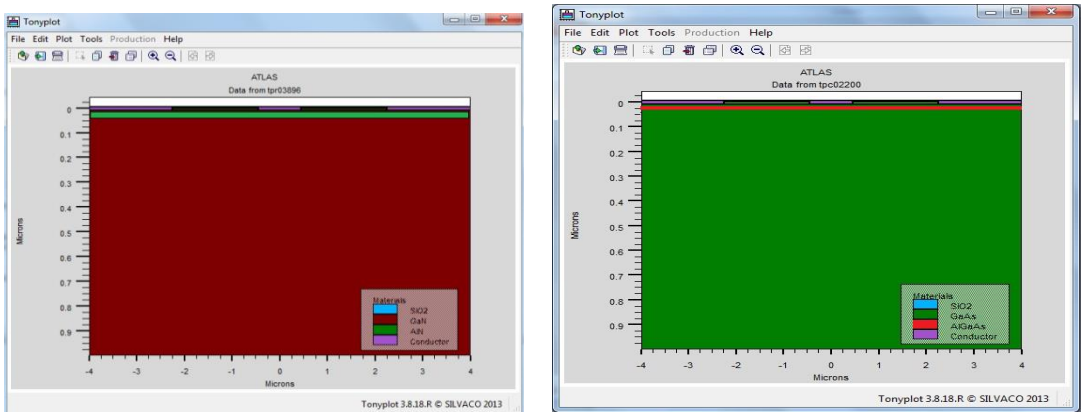

Fig.(2): Schematic structure for GaN and GaAs HEMT by Silvaco software

4. Simulation Results

4.1. Simulation results based on silvaco software for (I-V) diagrams of the two models, where drain voltage (0 to 5 V) and four different gate source voltage applied (0, -1, -2, -3 V), were shown in Fig.(3).

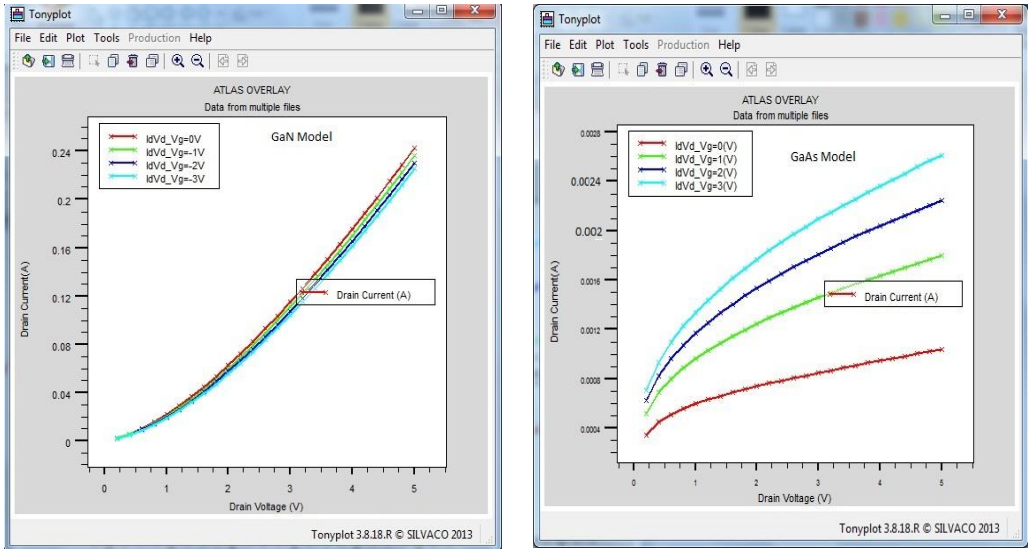

Figure (3): (Ids-Vds) current for different voltage gate (Vgs)

It can be seen that from the above figures that the drain current of GaN is (100 times) larger than of GaAs and it will increase as the drain voltage increases, while GaAs drain current seems going to saturation region as the drain voltage increases, which gives the best suitability for GaN materials in the power applications. Another good parameter for comparison between the two models is (Ids-Vgs) curve as shown in Fig.(4).

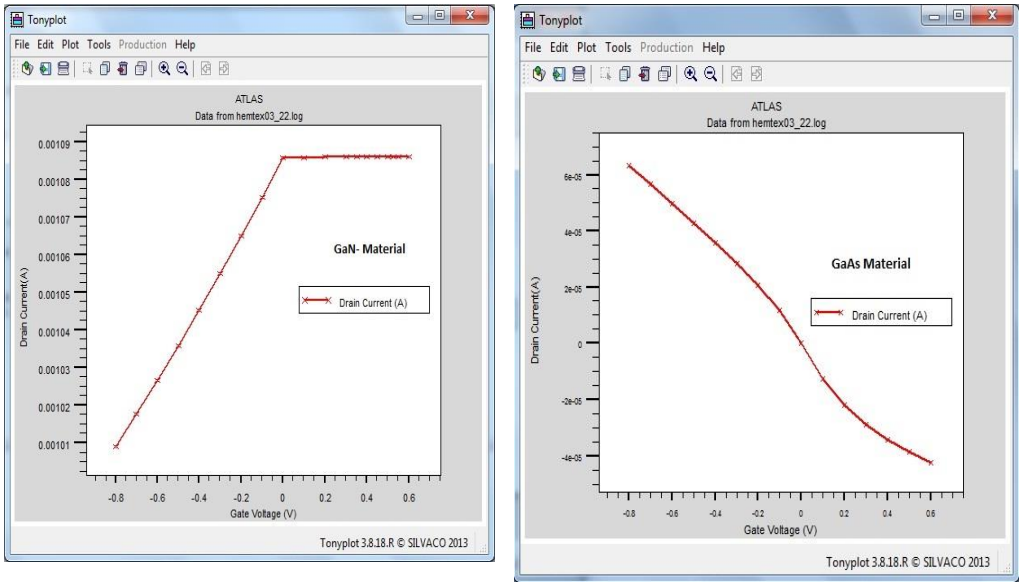

Figure (4): Ids-Vgs for two models.

From other side to study the effect of the currents flow, three types of currents are collected in one diagram, as shown in figure (5).

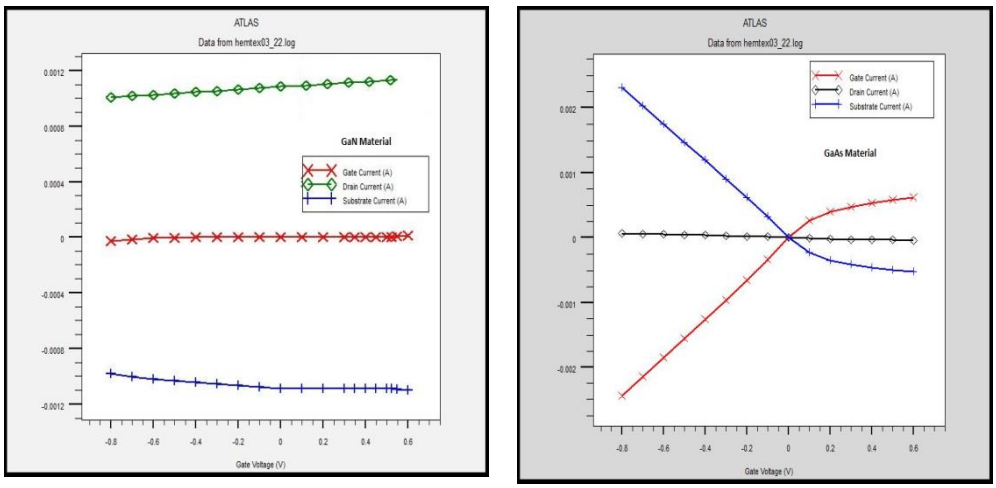

Figure (5): Comparison between three types of currents for the two models

From figure (5), the three currents (Ids, Igs and substrate current) have parallel characteristics for GaN model, while they intersect at zero gate voltage for gaAs model.

4.2. The results of (C-V) characteristics for any model have special important to designers, because it gives clear view for the frequency domain. The internal gate-source capacitance(Cgs) is very important for microwave applications because of its significant impact on both input device and ultimate frequency performance.

Figure (6) illustrates the variation values of C_{gs} in the two suggested models.

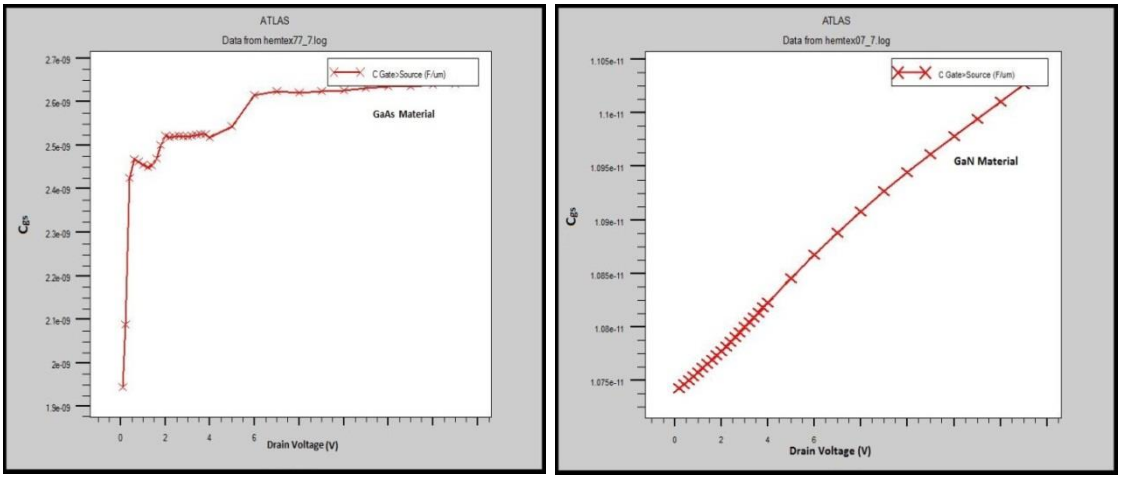

Fig. (6): min.Cgs=1.9nF, Max=2.6nF min.Cgs=10.75Pf, Max= 11.05Pf

Figures (7) and (8) express a comprise in (C-V) characteristics for the two models

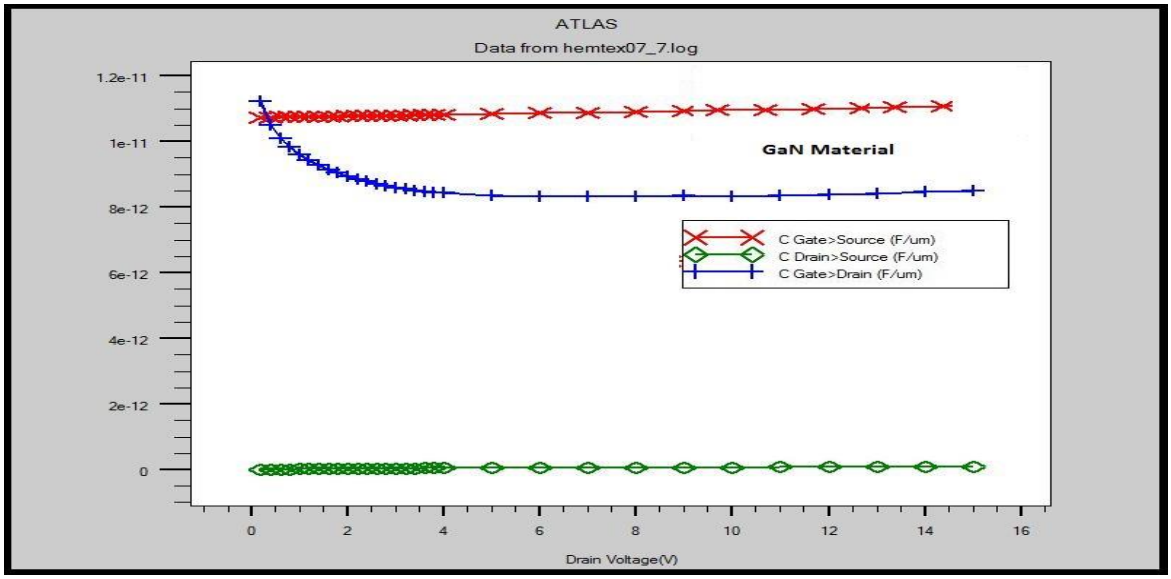

Fig. (7): Three types of capacitance (Cgs, Cgd, and Cds) for GaN model

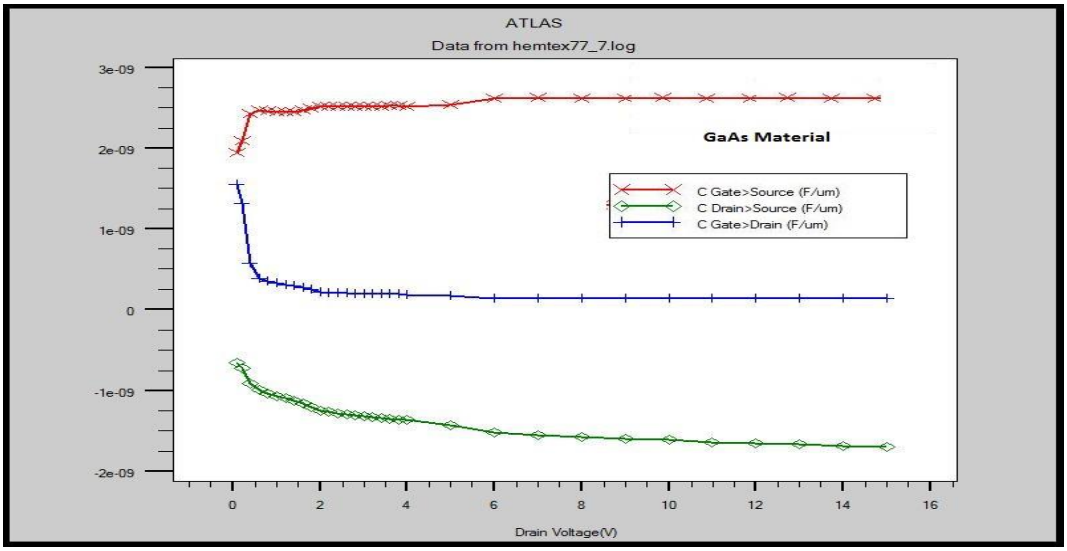

Fig.(8): Three types of capacitance (Cgs, Cgd, and Cds) for GaAs model

5. Results And Discussion

Fig. (1) shows depletion region extraction with three primary sector (Q1, Q2, Q3) which the device impacts under their effects. Fig.(2) shows modeling schematics for GaN and GaAs materials at T=300K, Table (1) explains doping layers in (y-axis), 1-D Poisson's equation used to predict the channel potential, (I-V) characteristics shows good progress for GaN upon GaAs model, since current drain for GaN increases ascending and goes over to reach saturation region while it increases very slow for GaAs model. From other view drain current for GaN model is (100 times) more than that of GaAs model for same drain voltage, which give good advantages in power applications. (Ids- Vgs) characteristic shown in fig(4), reveals Ids increases proportionally with gate voltage for GaN model, while it is proportional inversely with in GaAs model.

A good C-V model is essential from microwave application point of view. Hence in the present model, Silvaco software uses empirical relations for Cgs and Cgd to provide the best results, which shows (10-12 Pf) value of Cgs for GaN model while it was (2-3 nf) for GaAs one.

6. Conclusion

In this paper, an attempt is made to analyze and models two HEMT transistors based on famous materials GaN and GaAs with typical dimensions (8x1 micron) and (1 micron) for channel length. The output power for GaN is greater than that of GaAs(100 times).For (I-V) characteristics, GaN shows large current drain according to drain voltage. This high current and output power makes this model very suitable for power amplifier applications. The (C-V) characteristics was calculated and it is found that the value of Cgs and Cgd are (10-12 Pf), which seems to be less sensitive to temperature and frequency variations. The designed structure of GaN HEMT can be a good solution for telecommunication system that requires high frequency and high power which gives good promises that can be used as good alternative of travelling wave tube (TWT) in recent future.

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Simulation of The CdTe/CdS Nanothickness Solar Cell With ZnTe As A Back Contact Buffer Layer to Enhance Efficiency

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Abstract

In this paper, Zinc-Telluride(ZnTe) thin film direct energy band gap is used as a back contact buffer layer with a final back contact Molybdenum (Mo) in a CdTe / CdS nanothickness solar cell. This work is study and investigates the effect of Zinc-Telluride on the power conversion efficiency, and the effect of the absorber layer thickness on the performance of the cell is. This can be done by using the simulation program SCAPS – 1D version 3.2.00 (2012).The comparison between the efficiency of the cell with and without using ZnTe as a buffer layer is discussed.

Keywords: Back contact, Efficiency enhanced, SCAPS – 1D, Solar cell, ZnTe.

محاكاة لخلية شمسية رقيقة نوع CdTe /CdS ذات سمك نانوي باستخدام زنك تيلورايد كطبقة حاجز الاتصال الخلفية مع تحسين الكفاءة

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الخلاصة

في هذا البحث تم استخدام مادة الزنك تولورايد ZnTe ذات فجوة الطاقة المباشرة على القاعدة نوع مولبدينيوم Mo تعمل كطبقة عازلة خلفية في خلية CdTe/CdS الرقيقة. والهدف من هذا العمل هو دراسة تأثير استخدام مادة الزنك تولورايد على أداء الخلية الشمسية وأثره على كفاءة القدرة التحويلية وبيان تأثير سمك طبقة الامتصاص CdTe على أداء الخلية. تم تحقيق النتائج باستخدام برنامج المحاكاة الحاسوبي SCAPS VRSION 3.2.00 وكذلك تمت مقارنة كفاءة الخلية بوجود طبقة ZnTe وعدم وجودها .

Introduction:

When the solar cell is illuminated, part of the incident light is reflected and the rest is transmitted or absorbed [1].The energy of the absorbed photon can be transferred to an electron in the valence band of a semiconductor, which is brought to the conduction band, when the photon energy is larger than the band gap energy E_g of the semiconductor ($hv>E_g$).The photon is absorbed during this process and an electron–hole pair (EHP) is generated. Photons with energy smaller than E_g, however, cannot be absorbed and the solar cell is transparent for light with wavelengths larger than the cut off wavelength (λ_c) [2].

$$\lambda_c = hc_o/E_g \quad (1)$$

h is the blank's constant = 6.626×10^{-34} j-s.
c_o is the speed of light in vacuum = 3×10^{8} m/s.
E_g is the energy gap of the semiconductor (eV).

The absorption of light can be described by relating the radiation intensity (I_o) falling on a semiconductor surface to the intensity ($I(y)$) that remains after the light penetrated distance (y) using Lambert-Beer's law [1]:

$$I(y) = e^{-\alpha y} \quad (2)$$

The parameter α, which is a function of the wavelength of the light, is a characteristic of the material, and is called as the absorption coefficient (cm^{-1}).The value of the absorption coefficient must be high for the absorber material used in a solar cell device, so that most of the light is absorbed in a useful way.

Wide band CdS (Eg = 2.4eV) has been used as the window material together with several semiconductors such as CdTe [3]. Therefore it also permits the absorber layer to receive the photons of lower energy to give rise to electron hole pairs up on illumination with the solar light. Depending on the thickness of the CdS some of the light below the 510 nm can still pass through to the CdTe giving additional current to the device. The reduction of layer thickness is then important to gain more photons in CdTe [4].

CdTe absorber layer should be electrically p-type to form the p-n junction with n-CdS. It has an energy band gap of 1.45 eV which gives the highest theoretical efficiency. It is sufficient to absorb the useful part of the solar. Since CdTe has lower carrier concentration than the CdS, the depletion region is mostly within the CdTe layer and in this region most of the carrier generation and collection occur [4]. Since CdTe is a semiconductor with a high electron affinity (χ = 4.5 eV) and high energy bandgap, a high work-function metal is required to make good ohmic contact to CdTe. A typical metal with a high work-function ($\varphi m \geq 5.9$ eV) is required to make an ohmic contact to CdTe. But mostly they do not have work functions large enough to make good ohmic contacts to CdTe, and tend to form Schottky, or blocking barriers. To overcome this obstacle is to either reduce the barrier or moderate its width by heavily doping extra buffer layer of different potential material in between the CdTe and metal back-contact interface. The specific back contact buffer materials have been chosen for this work for CdTe solar cell are Zinc Telluride (ZnTe) [5].

Zinc Telluride, p-type semiconductor with a direct band gap of 2.26 eV has been used for this purpose. The formation of ohmic contacts to ZnTe is easier due to its lower work function and the ability to dope it highly p-type [6]. Another attractive quality of ZnTe is the very low valence band discontinuity of –0.14 eV with CdTe. Thus it provides no hindrance to the flow of holes towards the contact. ZnTe can be used as a back contact material to get higher solar energy conversion efficiency in CdTe cells [6].

Solar Cells characteristics [7]:

There are certain parameters to be mentioned in the I-V characteristics of a solar cell.

1. Overall Current (I)

Overall current is determined by subtracting the light-induced current from the diode dark current and can be expressed as: Overall current (*I*=Diode dark current (*I*D)-light-induced current (I_L)

$$I = I_0\left[\exp\left(\frac{eV}{kT}\right) - 1\right] - I_L \quad (3)$$

where Io is the saturation current, which is also known as the leakage or diffusion current I_o ~ 10 E- 8Amp. for good solar cells ; e is the charge on an electron and hole and k is Boltzmann's constant. Both I_l and I_o depend on the structure of solar cells.

2. Short Circuit Current (Isc)

Short circuit current is the light-generated current or photo current, I_l. It is the current in the circuit when the load is zero in the circuit. It can be achieved by connecting the positive and negative terminals by copper wire.

3. Open Circuit Voltage (Voc)

Open circuit voltage is obtained by setting I= 0 in the expression for overall current i.e. I=0 when V=V_{oc}.

$$V_{oc} = \frac{kT}{e}\ln\left(\frac{I_L}{I_0} + 1\right) \quad (4)$$

The open circuit voltage is the voltage for maximum load in the circuit.

4. Fill Factor (FF)

The "fill factor", more commonly known by its abbreviation "FF", is a parameter which, in conjunction with V_{oc} and I_{sc}, determines the maximum power from a solar cell. The FF is defined as the ratio of the maximum power from the solar cell to the product of V_{oc} and I_{sc}. Graphically, the FF is a measure of the "squareness" of the solar cell and is also the area of the largest rectangle which will fit in the IV curve. The FF is illustrated below.

$$FF = \frac{P_{max}}{V_{oc} \times I_{sc}} = \frac{I_{max} \times V_{max}}{V_{oc} \times I_{sc}} \quad (5)$$

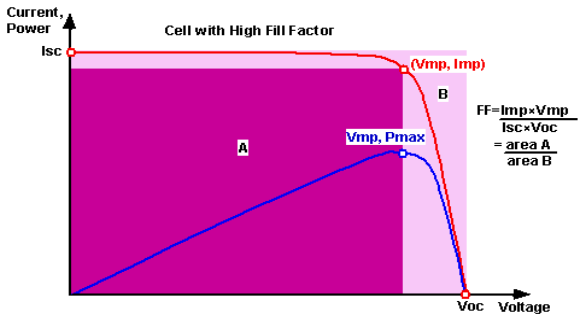

Fig. (1): Characteristic curve for determining the fill factor

5. Maximum Power (p_{max})

No power is generated under short or open circuit. The power output is defined as

$P_{out} = V_{out} * I_{out}$ (6)

The maximum power (p_{max}) provided by the device is achieved at a point on the characteristics, where the product *IV* is maximum. Thus

$P_{max} = I_{max} * V_{max}$ (7)

The maximum possible output can also be given as

$P_{max} = V_{oc} * I_{sc} * FF$ (8)

6 . Solar Cell Efficiency (ηec)

The solar cell power conversion efficiency can be given as

$$\eta_{ec} = \frac{P_{max}}{P_{in}} = \frac{I_{max} \times V_{max}}{Incident\ solar\ radiation \times Area\ of\ solar\ cell} = \frac{V_{OC} \times I_{SC} \times FF}{I(t) \times A_C} \quad (9)$$

Where Imax and Vmax are the current and voltage for maximum power, corresponding to solar intensity (I(t))measured in w/ m^2. Ac is the area of the cell.

Methods of efficiency enhancement:

There are several methods used for enhancement the power conversion efficiency in solar cells and these methods may be adopted for optimizing the performance of a solar cell [8]. Such as : Reflection by a mirror, tracking the sun, antireflection coating technologies deposition method , polycrystalline Silicon, multiband and Impurity Photovoltaic Cells ,thermo photovoltaic and thermo photonic devices, and reduction the loss.

Solar Cell Simulation:

The typical structure of CdTe / CdS solar cell with the back contact buffer material ZnTe shown in Fig. 2 is used to investigate the cell output performances.

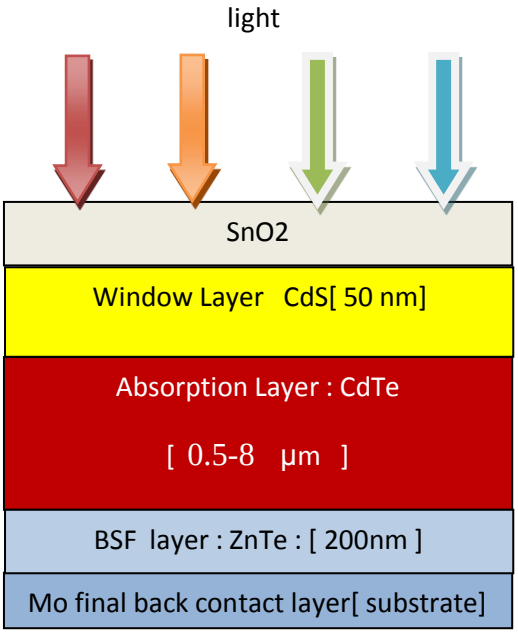

Fig. (2): Structure of the CdTe/CdS solar cell designed with back contact of ZnTe material.

The analysis of the solar cell is always used the computer programs to satisfy the higher methods of modeling and large number of parameters that varied in particular solar cell.

The numerical program which solves the basic semiconductor equations could be used for modeling thin film solar cell. These basic equations are poisson s equation, the continuity equation for free electrons, and holes. A various number of simulation programs have been developed and widely used recently , such as AMPS- 1D , SCAPS-1D,PC-1D , and AFORS-HET. In this work SCAPS-1D version 3.2.00 was used to simulate the proposed cell [9].

The basic layers that have been emphasized in this modeling are the SnO2 or Al as a front contact layer and Mo as the final back contact layer have been assumed which are very common contacts for typical cell, and n- CdS as a window layer, p- CdTe as an absorber layer and ZnTe as a back contact buffer layer. The material parameters for each layer are summarized in table (2).

Table (2): Material parameters used in simulation[5].

Properties	p- ZnTe	p- CdTe	n-CdS
Thickness [nm]	200	50	50
Bandgap(ev)	2.26	1.5	2.53
Electron affinity X(ev)	3.5	4.28	4.3
Dielectric permittivity $\varepsilon/\varepsilon_o$	9.67	10.3	9.35
CB effective density of state $N_C[cm^{-3}]$	$1*10^{15}$	$7.5*10^{17}$	$1.8*10^{19}$
VB effective density of state $N_v[cm^{-3}]$	$1*10^{16}$	$1.8*10^{18}$	$2.4*10^{18}$
Electron thermal velocity (cm/s)	$1*10^{7}$	$1*10^{7}$	$1*10^{7}$
Hole thermal velocity (cm/s)	$1*10^{7}$	$1*10^{7}$	$1*10^{7}$
Electron mobility μ_n (cm^2/V-s)	330	800-1100	10
Hole mobility μ_h (cm^2/V-s)	80	60-90	10
n , p $[cm^{-3}]$	$6.8*10^{19}$	$1*10^{15}$	$1*10^{18}$

Results and Discussion:

The solar cell analysis using simulation numerical program (SCAPS -1D)version 3200 (2012) has been done under AM 1.5 G illumination, and room temperature aiming to explore the performances of the proposed solar cell with ZnTe back contact buffer layer.

The comparison performances between the two solar cells are summarized in the table (3).

Table (3): The output parameters of two conventional solar cells

Cell structure	V_{oc} (volt)	J_{sc} (mA/cm^2)	FF	Eff %
SnO2/CdS/CdTe	0.79	23.89	0.76	11.0
SnO2/CdS/CdTe/ZnTe	0.799	24.8	0.79	13.55

It is clear from table 3-first column that the conventional cell structure without any buffer layer shown power conversion efficiency of 11.0%, which is approximately common value for this kind cell. However, with ZnTe insertion created improved results and higher conversion efficiency of 13.55% .The improvement in efficiency came from the improvement of V_{oc} and J_{sc}. Theoretically the minimum thickness necessary for CdTe films to absorb 99% of the incident photons with energy greater than Eg is about 3 µm. The comparison of cell output performance between two cell (CdS/ CdTe/ZnTe) and (CdS/CdTe) are explained in Fig. 4, which shows the several quantum efficiencies.

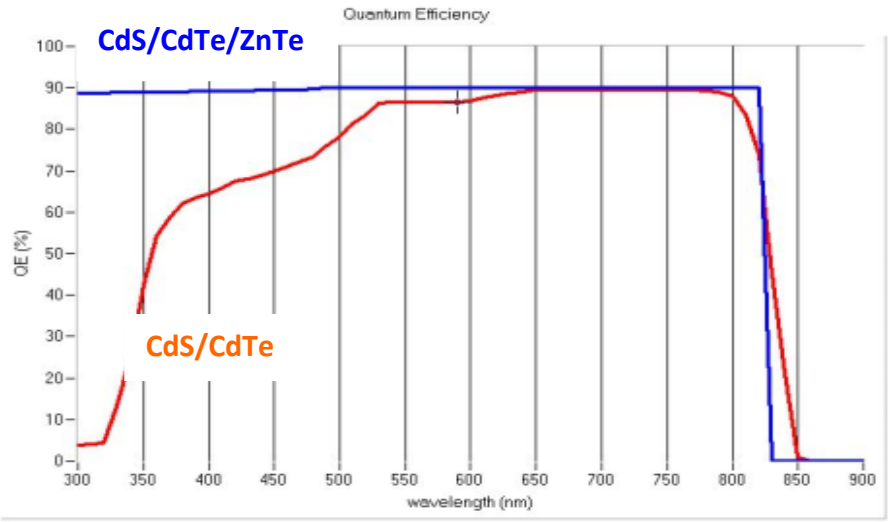

Fig . (4): Quantum efficiency of two different cells

From the theoretical calculations for the CdTe cell using the measurement results from the practical work, and applying the equations (5, 7, 8, and 9), are summarized in table (4).

Table (4): The output parameters of two conventional solar cells

Cell structure	V_m (volt)	I_m (mA)	P_m(mw)	P_{in}(mw)	Eff %
SnO2/CdS/CdTe	0.23	14.9	3.27	45.45	7.5
SnO2/CdS/CdTe/ZnTe	0.297	14.0	4.158	45.45	9.1

From table (4), the efficiency of the solar is increased after adding the ZnTe about 1.65%

This is differing on the efficiency from the simulation program, because of the effect of practical measurements, devices, materials and instruments.

The absorber layer thickness is effecting on the output performance of the cell. It is clear that the *Voc* and FF are approximately constant with the CdTe thickness increased for the two structures. But the Voc and FF values for the cell having aback contact buffer layer ZnTe is larger than that cell without ZnTe. This results are determined by a SCAPS-1D simulation program, and plotted using a MATLAB version 7.10.0.(R2010a). These explanations are shown in Figs.5 & 6.

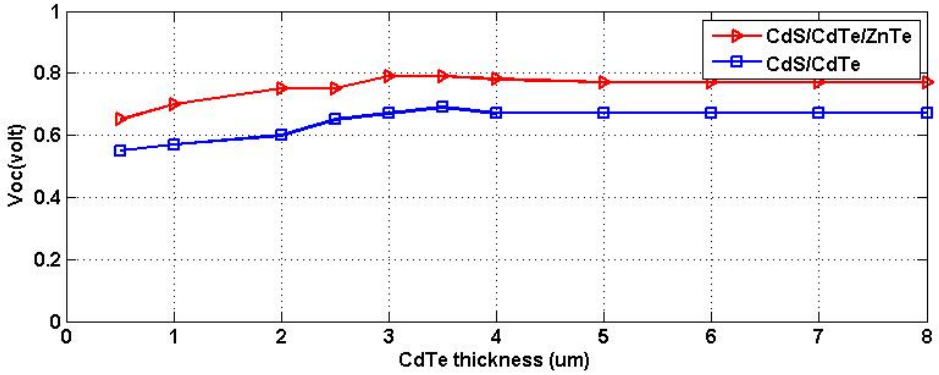

Fig. (5): Two different structure cells, the absorber thickness variations with the Voc.

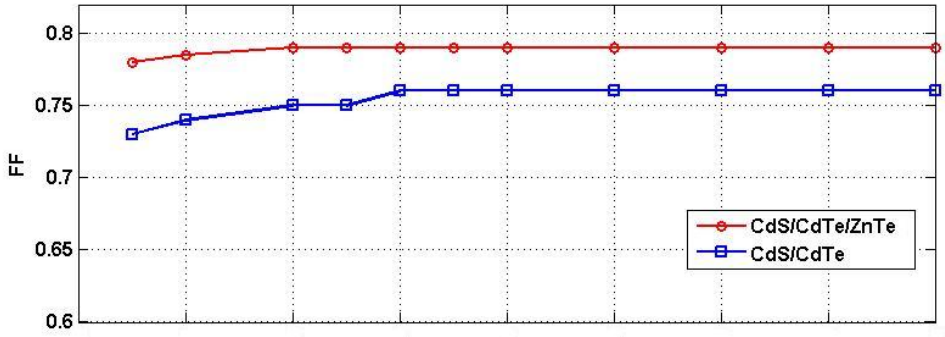

Fig. (6): Two different structure cells, the absorber thickness variations with the FF.

The short circuit current density *Jsc* and power conversion efficiency η were affected with the variations of the CdTe thickness. The cell without back contact buffer layer shows a lower much efficiency as the *Jsc* affected badly with the reduction of the CdTe layer thickness.

The cell structure with ZnTe as buffer layer shown better performance and almost unchanged output parameters till CdTe thickness of 3 µm. This implies that 3 µm thin or thinner CdS/CdTe cell is possible with ZnTe back contact buffer layer but not without buffer layer. These relations are shown in Fig.7 & 8.

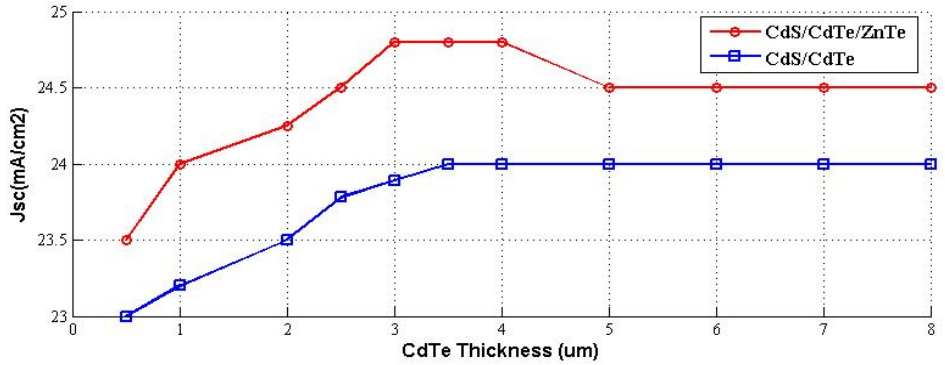

Fig. (7): Two different structure cells, the absorber thickness variations with the Jsc.

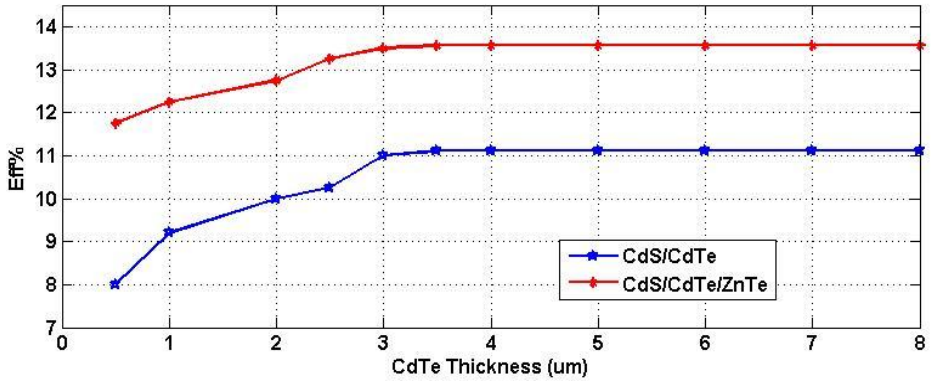

Fig. (8): Two different structure cells, the absorber thickness variations with the Eff.%.

Conclusions:

The high power conversion efficiency η = 13.5% for CdS/CdTe solar cell has been obtained from numerical analysis with 200 nm ZnTe as a back contact buffer layer and with CdTe thickness of 3.5µm. It seems that further reduction of CdTe layer is possible with the

least surrender of cell conversion efficiency. The best structure is the conventional structure with ZnTe as a back contact (CdS/CdTe/ZnTe) that has been achieved from this numerical analysis because of improvement in v_{oc} and j_{sc}. Hence the high efficiency of the CdTe solar cell can be realized with the optimum values of thickness , 50 nm of CdS layer, 3.5µm of CdTe layer and 200 nm ZnTe back contact buffer layer that contributes as the back surface effect to this configuration CdTe solar cells.

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Performance Evaluation Of Mpsk Modulation Using Vissim/Comm Simulator

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Abstract

It is a primary need today to achieve the higher data rates in limited spectrum bandwidth to improve System performance. Demand for mobile and personal communications is growing at a rapid pace, both in terms of the number of potential users and the introduction of new high-speed services. MPSK Modulation schemes, one of most bandwidth efficient techniques for achieving such higher data rates transmissions. In this paper the BER performance of the MPSK Modulation in the presence of additive white Gaussian noise (AWGN) channel has been simulated using VisSim/Comm Simulation software tool for communication systems models. VisSim/Comm is a Windows-based simulation environment for modeling end-to-end communication systems at the signal or physical level. Results shows a good agreement between theoretical and simulation results.

Keywords: AWGN, BER, MPSK, VisSim/Comm .

تقييم الإداء لتحوير Mpsk باستخدام محاكات Vissim/Comm

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الخلاصة

من الاحتياجات ذات الأولوية في الوقت الحاضر هو تحقيق مستوى عالي من سرعة نقل المعلومات ضمن حيز محدد من الطيف وبالتالي تحسين أداء المنظومة الرقمية. إن متطلبات منظومة الهاتف النقال والاتصالات الشخصية يتصاعد بشكل سريع متمثلا بالأعداد الهائلة من المستخدمين الذين يدخلون إلى الخدمة من ناحية ومن ناحية أخرى استحداث خدمات جديدة ذات سرع عالية. يعتبر تضمين الطور متعدد المستويات من التقنيات التي تمتلك كثافة طيفية عالية في تحقيق نقل هذه المعلمات التي تمتلك معدل سرعة عالية. تم في هذه المقالة إجراء محاكاة لمعيار معدل الخطأ للمعلومة لنظام تضمين الطور متعدد المستويات وباعتماد القناة ذات الضوضاء المضافة الغاوسية التوزيع. استند نظام المحاكاة المستخدم على الوسيلة البرمجية نوع (VISSIM/COMM) والذي يمثل الجزء الخاص بمجال الاتصالات. ترتكز هذه الوسيلة البرمجية على نظام النافذة في برنامج المحاكاة لتمثيل منظومة الاتصالات في الإرسال والاستلام وبالمستوى الفيزيائي. لقد أظهرت نتائج البحث تطابق واضح بين نتائج المحاكاة والنتائج النظرية.

1. Introduction

The demand for higher data rate and better bandwidth efficiency is increased day by day, but the total bandwidth allocation is limited. Cellular communication systems are the most widely used wireless communication systems. It is a primary need today to achieve the higher data rates in limited spectrum bandwidth to improve the performance of signals and flexibility. Hence, there has been great deal of search for a digital communication system that is bandwidth efficient and has low bit error rate (BER) at a relatively low signal to noise ratio. Various digital modulation schemes are incorporated but they are not feasible or cannot fulfill actual requirement varying in different kind of environment. Therefore it is very much necessary to study the modulation schemes which give us the better result. *M*-array modulation schemes achieve better bandwidth efficiency than other modulation techniques and give higher data rate [1][2].

The objective of this paper is to evaluate the *M*-array phase shift keying (MPSK) digital modulation schemes on the basis of the BER performance considering Additive White Gaussian Noise (AWGN) channel. To better evaluate the MPSK system, a VisSim/Comm simulation environment-based was used. System is designed for MPSK with M=4, 8 and 16. Results indicates that increasing of M results in increase of BER of MPSK system versus the signal-to-noise ratio (SNR) which is used to evaluate the performance of MPSK system. The BER curves for MPSK obtained after simulation are compared with theoretical curves. Constellation diagrams of the MPSK modulated signals was also considered in this paper. Modulations with large constellations have higher data rates for a given signal bandwidth, but will have higher error rates which require more transmission power to maintain a given Quality of service as determined by the communication service.

Intersymbol interference (ISI) due to multipath channel. is not taken into account here, since by decoupling the noise from the ISI we are able to simplify the system model and to constraint in this level of research on the exploiting of the VisSim/Comm facility to simulate an end to end communication system.

2. M-Array Modulation Techniques

Advancement in very large-scale integration (VLSI) and digital signal processing (DSP) technology have made digital modulation more cost effective than analog modulation. Digital modulation offers many advantages such as greater noise immunity and robustness to channel impairments, easier multiplexing of various forms of information and greater security. Moreover, digital transmissions accommodate digital error control codes, support complex signal conditioning and processing techniques such as source coding, encryption, equalization and diversity combining to improve the performance of the overall communication link. Digital baseband data may be sent by varying both the envelope and phase (or frequency) of an RF carrier as the envelope and phase offer two degrees of freedom and modulation techniques map baseband data into four or more possible RF Carrier signals. Such modulation techniques are called M-array modulation, since they can represent more signals than if just the amplitude or phase were varied alone [3].

In an M-array signaling scheme, we may send one of M possible signals s1(t), s2(t)……sM(t), during each signaling interval of duration Ts. For almost all applications, the number of possible signals $M=2^k$, where k is an integer. The symbol duration Ts=kTb, where Tb is the bit duration.

In pass-band data transmission these signals are generated by changing the amplitude, phase, frequency of a sinusoidal carrier in M discrete steps thus we have M-array ASK, M-array PSK and M-array FSK digital modulation schemes. Different bandwidth efficiency at the expense of power efficiency can be achieved using M-array modulation schemes [1].

2.1 M- Array Phase Shift Keying (MPSK) Modulation

In M-array PSK, the carrier phase takes on one of M possible values, namely, $\theta i = 2\,(i - 1)\,\pi/M$, where $i = 1,2, \ldots, M$. The modulated waveform can be expressed as [4].

$$S_i(t) = \sqrt{\frac{2Es}{T_s}} \cos\left(2\pi fct + \frac{2\pi}{M}(i-1)\right) \quad , 0 \le t \le T_S \quad i = 1,2,\ldots,M \qquad (1)$$

Where $E_s = (Log_2 M)\, E_b$ is the energy per symbol and $T_s = (Log_2 M)\, T_b$ is the symbol period.

T_b =Bit duration

E_b = The energy per bit= $TS/(Log_2 M)$

$M = 2^k$

k = Number of bit per symbol

f_c is the frequency of the carrier

2.2 Constellation Diagram Concept

Constellation diagram provides a graphical representation of the complex envelope of each possible Symbol state belong to a signal which is modulated by a digital modulation scheme . It displays the signal as a two-dimensional scatter diagram in the complex plane at symbol sampling instants and it can be obtained by deducing the orthogonal basis functions $\Phi_1(t)$ and $\Phi_2(t)$ of the modulated signal using Gram-Schmidt orthogonalization procedure [5].

Using the trigonometric identity $\cos(a + b) = \cos(a)\cos(b) - \sin(a)\sin(b)$ we can rewrite (1) as

$$S_i(t) = \sqrt{\frac{2Es}{T_s}} \cos\left(\frac{2\pi}{M}(i-1)\right)\cos(2\pi fct) \quad - \sqrt{\frac{2Es}{T_s}} \sin\left(\frac{2\pi}{M}(i-1)\right)\sin(2\pi fct) \quad i = 1,2, \ldots,M \qquad (2)$$

The MPSK signal set can be expressed as

$$S_i(t) = S_{i1}\,\Phi_1(t) + S_{i2}\,\Phi_2(t) \qquad (3)$$

Where

$$S_{i1} = \sqrt{Es}\cos\left(\frac{2\pi}{M}(i-1)\right) \quad , \quad S_{i2} = \sqrt{Es}\sin\left(\frac{2\pi}{M}(i-1)\right)$$

$$\phi_1(t) = \sqrt{\frac{2}{T_s}}\cos(2\pi f_c t)$$

$$\phi_2(t) = \sqrt{\frac{2}{T_s}}\sin(2\pi f_c t)$$

Here $\phi_1(t)$ and $\phi_2(t)$ are orthogonal basis functions of the MPSK modulation and $S_{i1}(t)$ and $S_{i2}(t)$ are the coefficients of each signaling point in the M-PSK constellation. The constellation points on the M-PSK constellation lie $2\pi/M$ radians apart and are placed on a circle of radius $\sqrt{Es}$. The coefficients s_{i1} and s_{i2} are termed as in phase (I) and quadrature-phase (Q) components respectively. The constellation diagram of an 8-array PSK signal set is illustrated in Figure 1. It is clear from Figure 1 that MPSK is constant envelop signal when no pulse shaping is used.

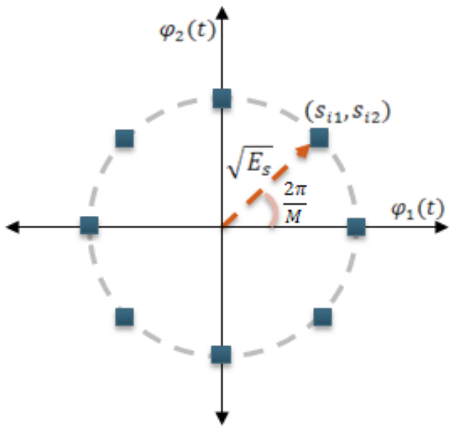


Fig. 1. Constellation diagram of MPSK with M=8

The measured constellation diagrams can be used to recognize the type of interference and distortion in a signal. The x- axis of the constellation diagram represents the in-phase component of the complex envelope and the y-axis represents the quadrature component of the complex envelope. The distance between the signals on the constellation diagram relates to how different the modulation waveform are, and how well a receiver can differentiate between all possible symbols when random noise is present.

In fact, because of the noise, the received samples will form a Gaussian cloud around the points in the constellation. Figure 2 shows in the case of 8-PSK, how constellations is formed:

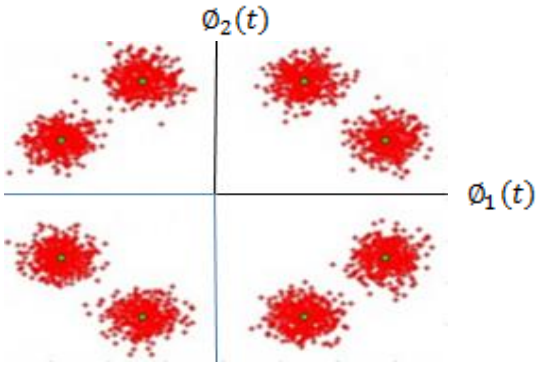


Fig. 2 . Clouded constellation for MPSK with M=8

Normally, the Bit Error Rate is measured by the distance between two nearest possible signal points in the signal space diagram (constellation diagram) as the distance between two points decreases the possibility of error increases. So, probability of BER increases as M increases.

3. Additive white Gaussian noise (AWGN)

In communication systems, the most common type of noise added over the channel is the Additive White Gaussian Noise (AWGN). It is additive because the received signal is equal to the transmitted signal plus the noise. It is white because it has a constant power spectral density. It is Gaussian because its probability density function can be accurately modeled to behave like a Gaussian distribution. It is noise because it distorts the received signal. The higher the variance of the noise, the more is the deviation of the received symbols with respect to the constellation set and, thus, the higher is the probability to demodulate a wrong symbol and make errors .Then the received signal is represented as :

$$r(t) = S_i(t) + n(t), \qquad i = 1,2,\ldots\ldots, M \tag{4}$$

where *r(t)*is the received signal, $S_i(t)$ is the transmitted signal, and *n (t)* is a zero-mean white Gaussian noise having a two-sided power spectral density of *No* /2 (W/Hz). The error performance, which is discussed in this paper, is mainly caused due to the channel additive noise [6].

4. BER Performance

In digital communication system design, the main objective is to receive data as similar as the data sent from the transmitter. It is important to analyze the system in term of probability of error to view the system's performance. Each modulation technique has different performance while dealing with signals, which normally are affected with noise. In Digital transmission the number of bit errors is the number of received bits of a data stream over a communication channel that has been altered due to noise, interference, distortion or bit synchronization errors. The bit error rate or bit error ratio (BER) is the number of bits in error divided by the total number of transferred bits during a studied time interval. BER is a unit less performance measure; often expressed as a percentage. The BER probability is defined as [7].

$$\text{Bit Error Rate } (P_B) = \frac{Number\ of\ bit\ in\ error}{Total\ number\ of\ transfered\ bits} \tag{5}$$

The BER probability of the coherent detection for an MPSK, assuming AWGN channel with two side noise probability of noise of *N0/2,*is given by [8].

$$P_B \approx \frac{2}{\log_2 M} Q\left(\sqrt{\frac{2\log_2 M\ E_b}{N_0}} \sin(\frac{\pi}{M})\right) \tag{6}$$

Where $Q(x) = \left(1/\sqrt{2\pi}\right)\int_x^{\infty} e^{-t^2/2} dt,$

5. VISSIM/COMM tool

VisSim is a trademark of Visual Solutions. VisSim is a visual environment for model-based development and dynamic simulation of complex systems. It combines an intuitive graphical interface with a powerful simulation engine to accurately represent linear and nonlinear systems, and simulate their behavior in continuous time, sampled time, or a combination of both. VisSim/Comm is a Windows-based simulation environment for modeling end-to-end communication systems at the signal or physical level. With its full complement of communication blocks and powerful, time-domain simulation engine, VisSim/Comm provides fast and accurate solutions for analog, digital, and mixed-mode communication systems. Using VisSim/Comm, you can seamlessly move among the stages of model construction, simulation, optimization, and validation. This means that you can simulate and view signal waveforms at any phase of the communication system chain. VisSim/Comm helps communication and electrical engineers decrease design cycle time, minimize hardware prototyping and build better products. The communication block set includes RF, UWB, Bluetooth, 802.x, Turbo Codes, Costas loop, PLL, VCO, BPSK, QPSK, DQPSK, QAM, BER, Eye Diagram, Viterbi, Reed-Solomon and much more [10][11].

6. Simulation and Results

The BER performance of the MPSK Modulation in the presence of additive white Gaussian noise (AWGN) channel has been simulated using VisSim/Comm Simulation software tool for communication systems models.

The simulation block diagram is shown in Figure 3. The implemented VisSim/Comm Simulator model for BER system evaluation is shown in Figure 4.

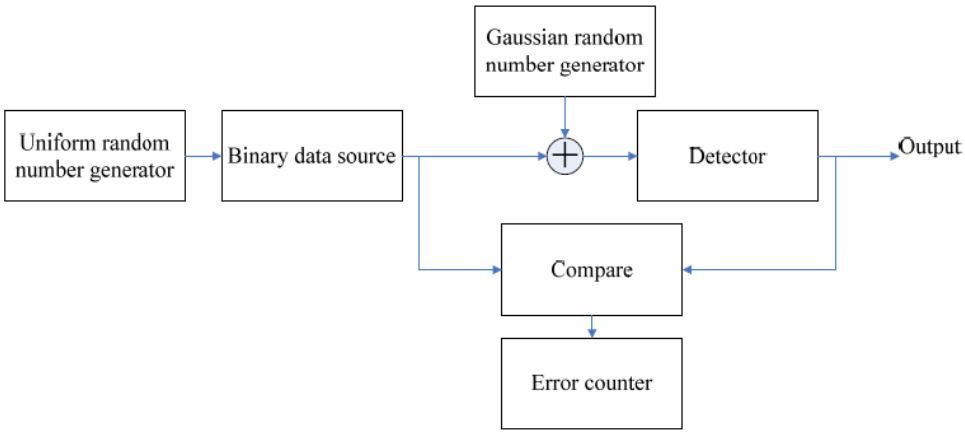


Fig. 3. Simulation block diagram of MPSK Modulation

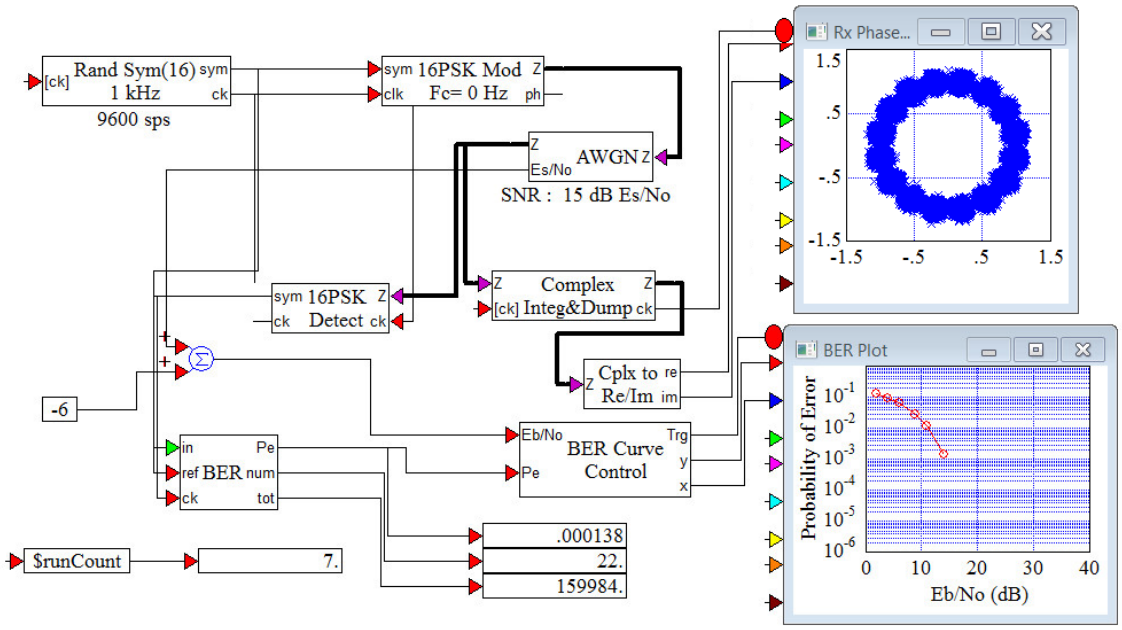
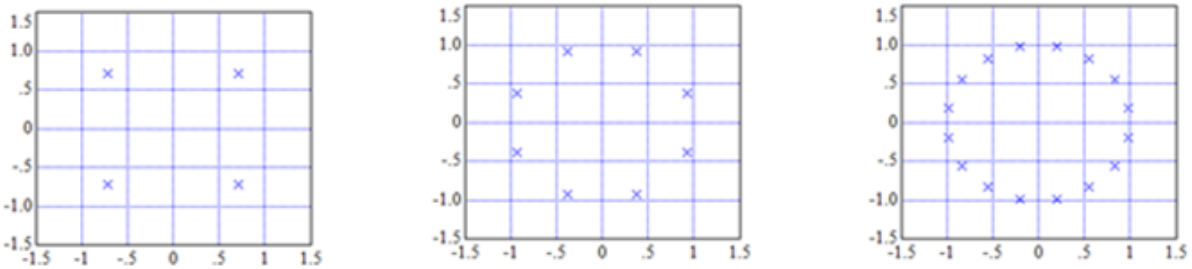


Fig. 4. Simulation model for MPSK Modulation

6.1. Constellation diagram

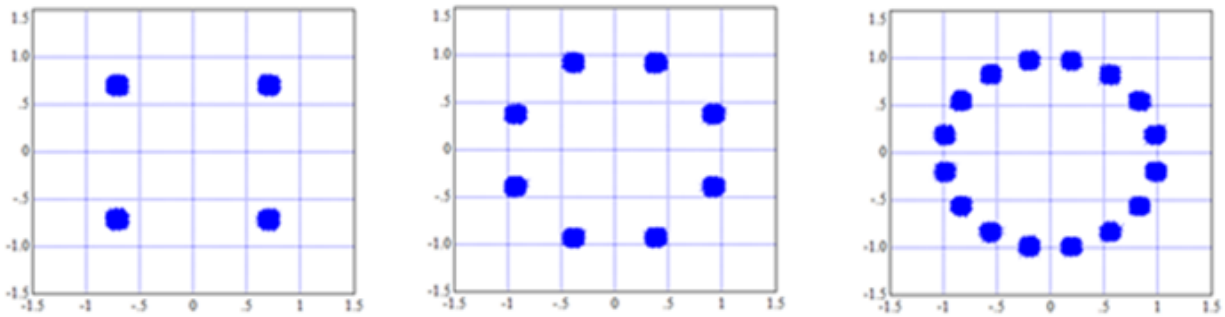
The ideal Constellation diagram for QPSK, 8-PSK and 16-PSK was simulated through the simulation model and is shown by Figure 5 (a), (b), and (c) respectively. Results shows a good agreement with theoretical ones.



(a) (b) (c)

Fig.5. Ideal constellation diagram for QPSK, 8-PSK and 16-PSK

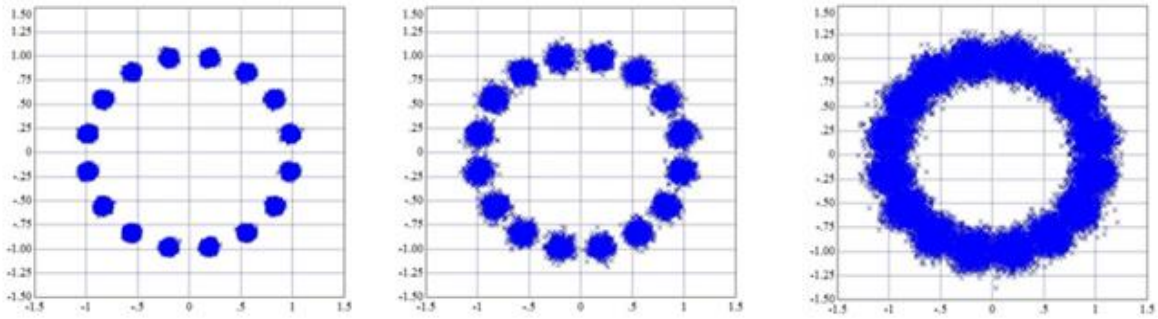
The noisy constellation diagram for QPSK, 8-PSK and 16-PSK was simulated through the simulation model for SNR= E_b/No =35dB and is shown by figure 6 (a), (b) and (c) respectively. The scattering phenomena due to AWGN is too clear.



(a) (b) (c)

Fig. 6. The noisy constellation diagram for QPSK, 8-PSK and 16-PSK

The noisy constellation diagram for 16-PSK was simulated for different signal to noise ratio (E_b/No = 32, 28, and 24 dB) as shown in figure 7 (a), (b), and (c) respectively. Results show more scattering occurring by decreasing the E_b/No value leading to decreasing the distance between adjacent constellation points and more degradation in system performance occurring due to increasing in the BER value.



(a) (b) (c)

Fig. 7. The noisy constellation diagram for 16-PSK for different SNR value

6.2. BER Performance

By considering perfect synchronization, zero ISI, and AWGN channel the simulated results of BER performance of QPSK, 8-PSK and 16-PSK was obtained using VisSim/Comm simulation environment and is shown in Figure 8 (a), (b) and (c) respectively. Results indicates that increasing of M leads to increasing BER for the same E_b/N_0 value.

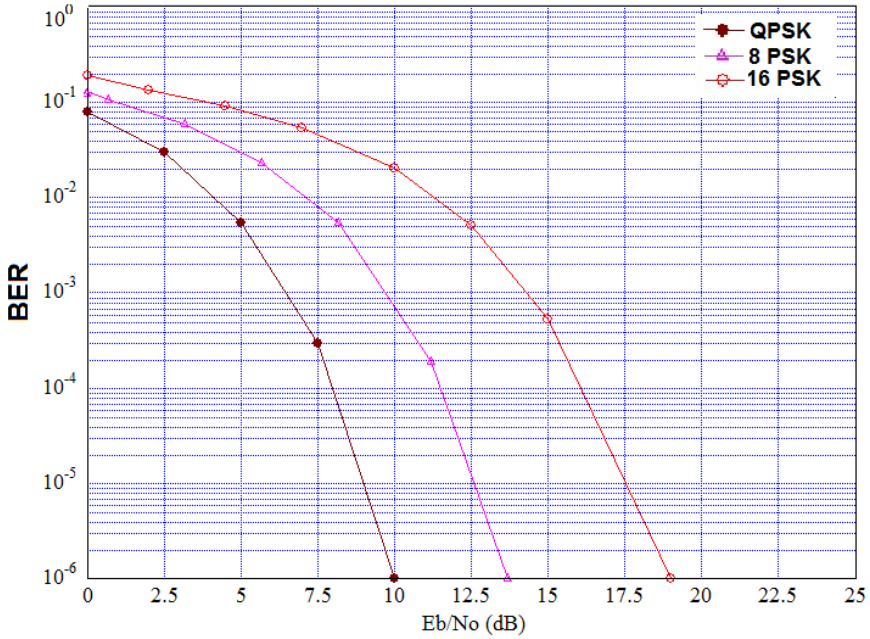


Fig.8. BER performance for MPSK Modulation

The comparative performance analysis of simulated and theoretical curves for BER verses E_b/No over AWGN channel for 16PSK is shown in Fig.9. Results shows a good agreement between theoretical and simulation results.

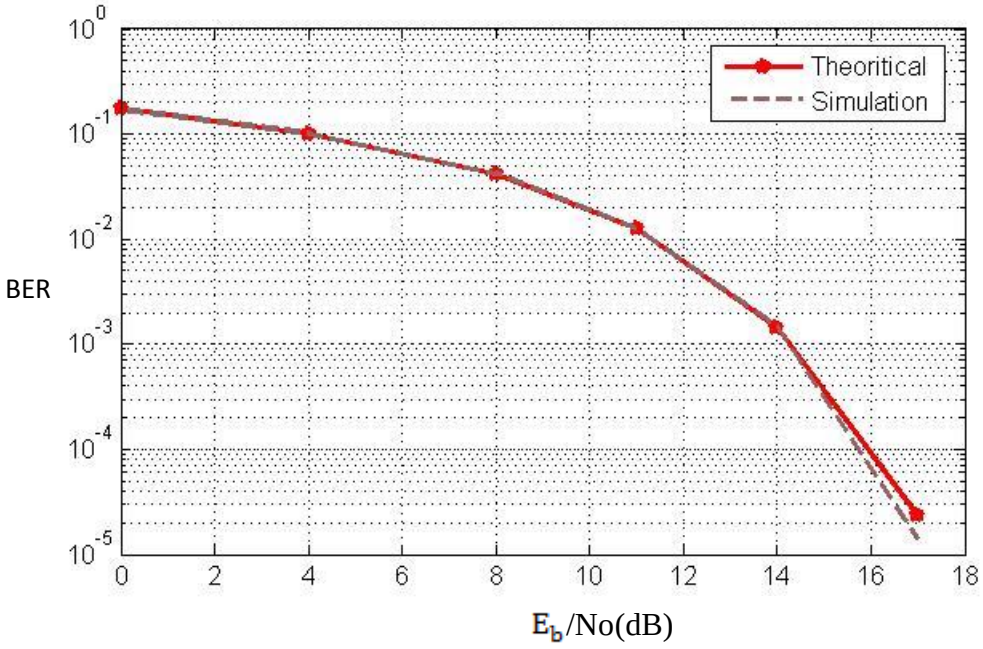


Fig. 9. Simulated and theoretical BER performance for 8PSK

7. Conclusion

VisSim/Comm Simulation software tool have been used efficiently to evaluate the BER performance of the MPSK modulation scheme in the presence of AWGN channel. Simulation results shows that the BER for all the MPSK based digital modulation schemes decrease monotonically with increase in E_b/No and having a good agreement with theoretical results. A QPSK system transmits information at twice the bit rate of a BPSK system for the same channel BW due to which QPSK is mostly used in practice. In case of 16PSK the probability of error is greater as constellation points come closer, but BW of 16PSK is one fourth of the BW of BPSK. So, a 16PSK system transmits information at four time the bit rate of a BPSK system. By increasing the modulation order M, more efficient bandwidth modulation scheme is obtained with sacrificing in the system performance degradation. To evade such degradation, more power need to by imposed at the transmitter level.

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