Real Time Systems1

ACHIEVING PREDICTABILITY/ DMA

lecture 4-1

ACHIEVING PREDICTABILITY

- **First** component that affects the predictability of the scheduling is the processor itself.
- The internal characteristics of the processor, such as:
- instruction pre-fetch,
- pipelining,
- cache memory, and
- direct memory access (DMA) mechanisms, are the first cause of non-determinism.

ACHIEVING PREDICTABILITY

- In fact,
- although these features improve the average performance of the processor, they introduce non-deterministic factors that prevent a precise estimation of the worst-case execution times (WCETs).

ACHIEVING PREDICTABILITY

- **Other important components** that influence the execution of the task set are the internal characteristics of the real-time kernel, such as the scheduling algorithm, the synchronization mechanism, the types of semaphores, the memory management policy, the communication semantics, and the interrupt handling mechanism

ACHIEVING PREDICTABILITY/ DMA

- *Direct memory access* (DMA) is a technique used by many peripheral devices to transfer data between the device and the main memory. The purpose of DMA is to relieve the central processing unit (CPU) of the task of controlling the input/output (I/O) transfer.

- Since both the CPU and the I/O device share the same bus, the CPU has to be blocked when the DMA device is performing a data transfer

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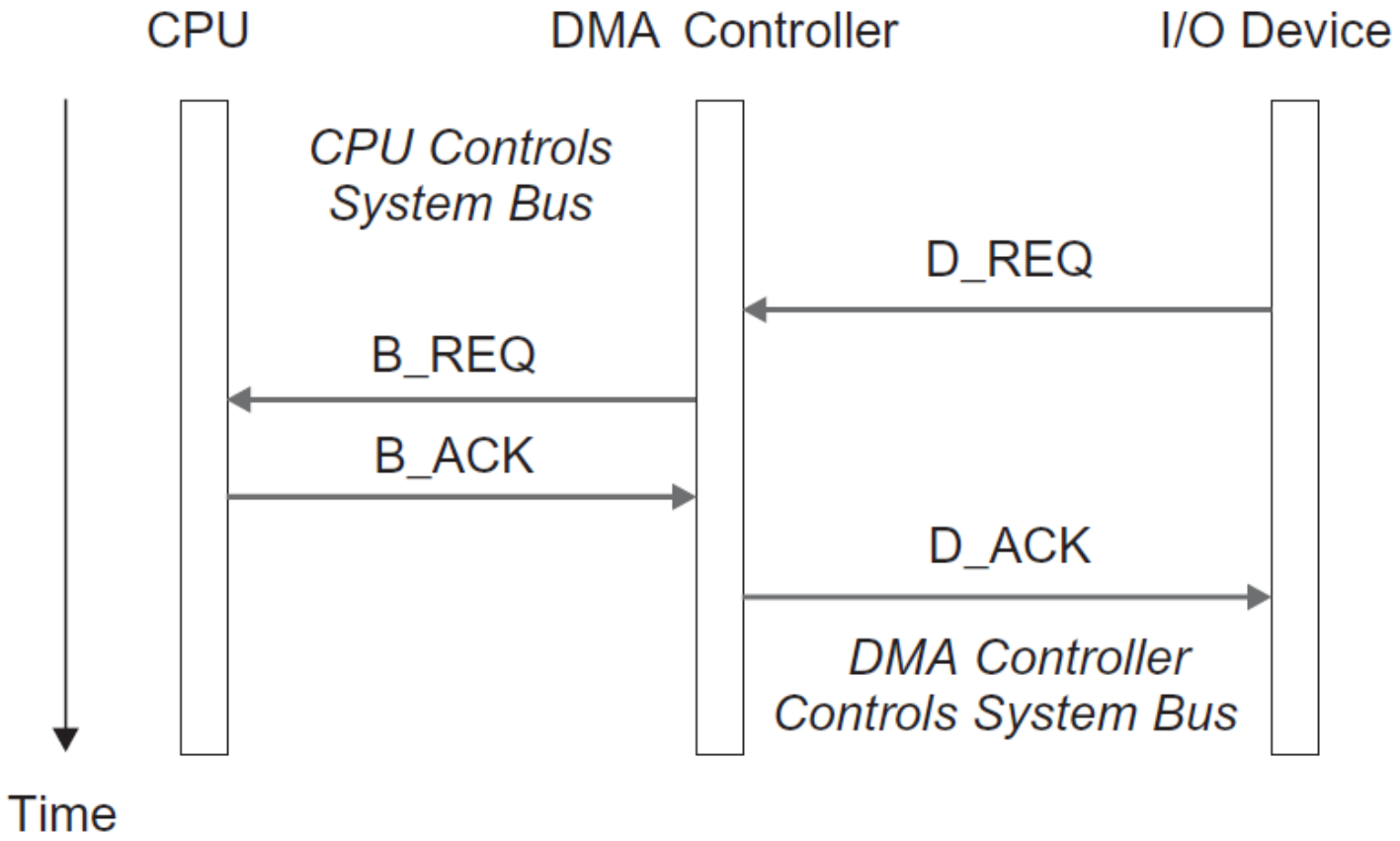

ACHIEVING PREDICTABILITY/DMA

- Several different transfer methods exist:

- Cycle stealing
- Time slice

ACHIEVING PREDICTABILITY/DMA

- *Cycle stealing method.* according to which the DMA device steals a CPU memory cycle in order to execute a data transfer. During the DMA operation, the I/O transfer and the CPU program execution run in parallel.

- However, if the CPU and the DMA device require a memory cycle at the same time, the bus is assigned to the DMA device and the CPU waits until the DMA cycle is completed.

ACHIEVING PREDICTABILITY/DMA/*cycle stealing*

- Using the cycle stealing method, there is no way of predicting how many times the CPU will have to wait for DMA during the execution of a task; hence the response time of a task cannot be precisely determined.

ACHIEVING PREDICTABILITY/DMA

- A possible solution to this problem is to adopt a different technique, which requires the DMA device to use the memory *time-slice method*.

- According to this method, each memory cycle is split into two adjacent time slots: one reserved for the CPU and the other for the DMA device.

ACHIEVING PREDICTABILITY/DMA

- Memory Time slice method is more expensive than cycle stealing but more predictable.

- In fact, since the CPU and DMA device do not conflict, the response time of the tasks do not increase due to DMA operations and hence can be predicted with higher accuracy.