Computer Science Dept. / 2nd year 2nd Course (2024-2025)
Computer Architecture
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Interleaving Memory

Memory Interleaving: It is a technique that divides memory into a number of modules (**banks**) such that successive words in the address space are placed in the different modules. It is used to improve the performance of memory systems.

Memory Banks: Independent sections of memory that can be accessed simultaneously.

In order to carry out **m** independent access simultaneously, main memory must be portioned into **m** separate memory **modules** or **banks M_0, M_1, M_2, … M_{m-1}** as shown in the figure:

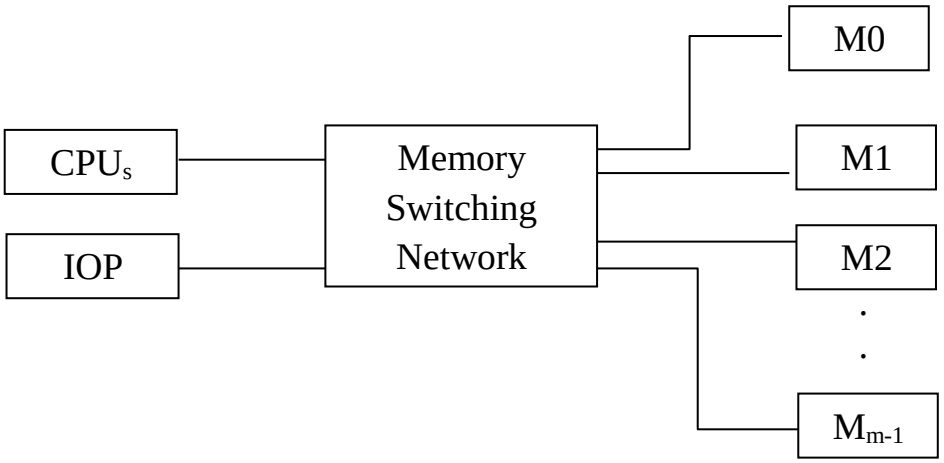

Figure: Modular Memory Organization.

Each module must be provided with its own independent addressing circuitry. A modular memory organization is ***particularly useful*** in multiprocessor system where several processors require access to a common memory. The processor memory bandwidth is then ***m words*** per memory cycle. There are ***two methods*** to organize data in the interleaved memory: ***Consecutive Word in a Module*** and ***Consecutive Word in Consecutive Module***.

➢ Consecutive Word in a Module:

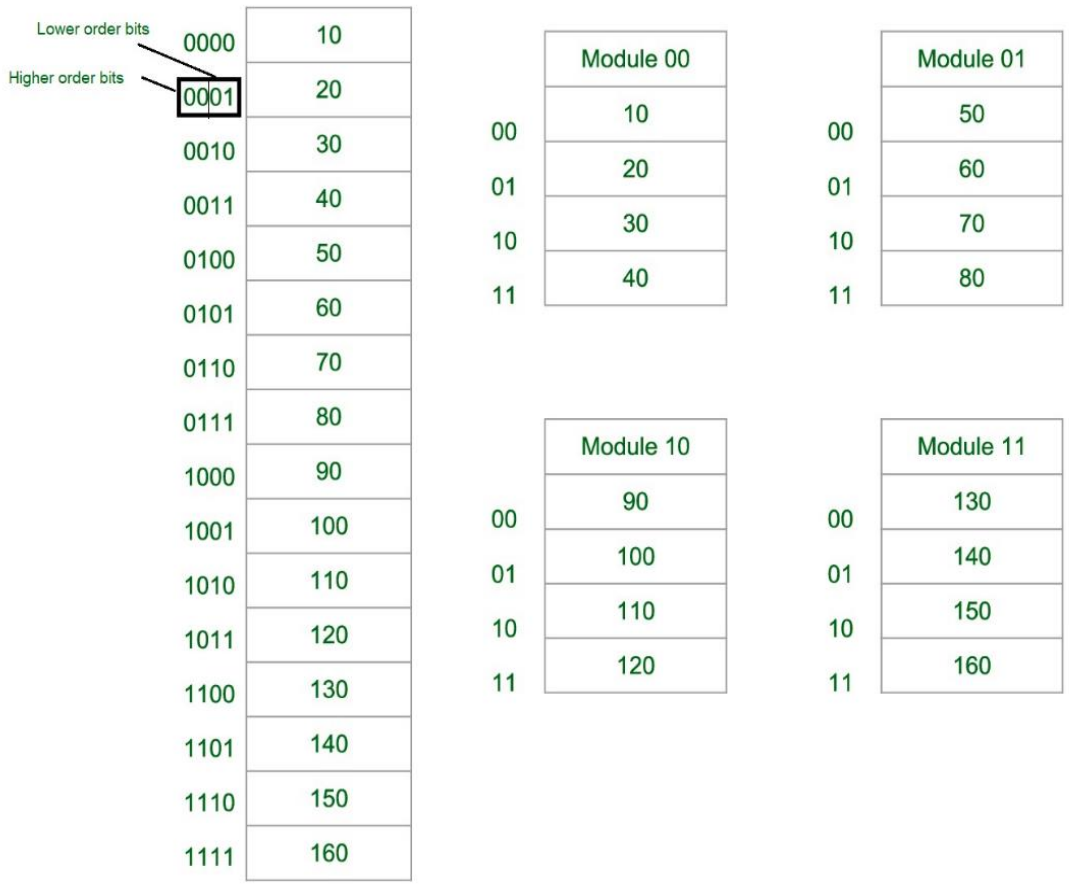

Figure: Consecutive Word in a Module

Most significant bit (***MSB***) provides the ***Address of the Module*** & the least significant bit (***LSB***) provides the ***Address of the Data*** in the module.

Example: to get 90 (Data) 1000 will be provided by the processor. This 10 will indicate that the data is in module 10 (module 3) & 00 is the address of 90 in Module 10 (module 3).

```
Module 1 Contains Data : 10, 20, 30, 40
Module 2 Contains Data : 50, 60, 70, 80
Module 3 Contains Data : 90, 100, 110, 120
Module 4 Contains Data : 130, 140, 150, 160
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➢ Consecutive Word in Consecutive Module:

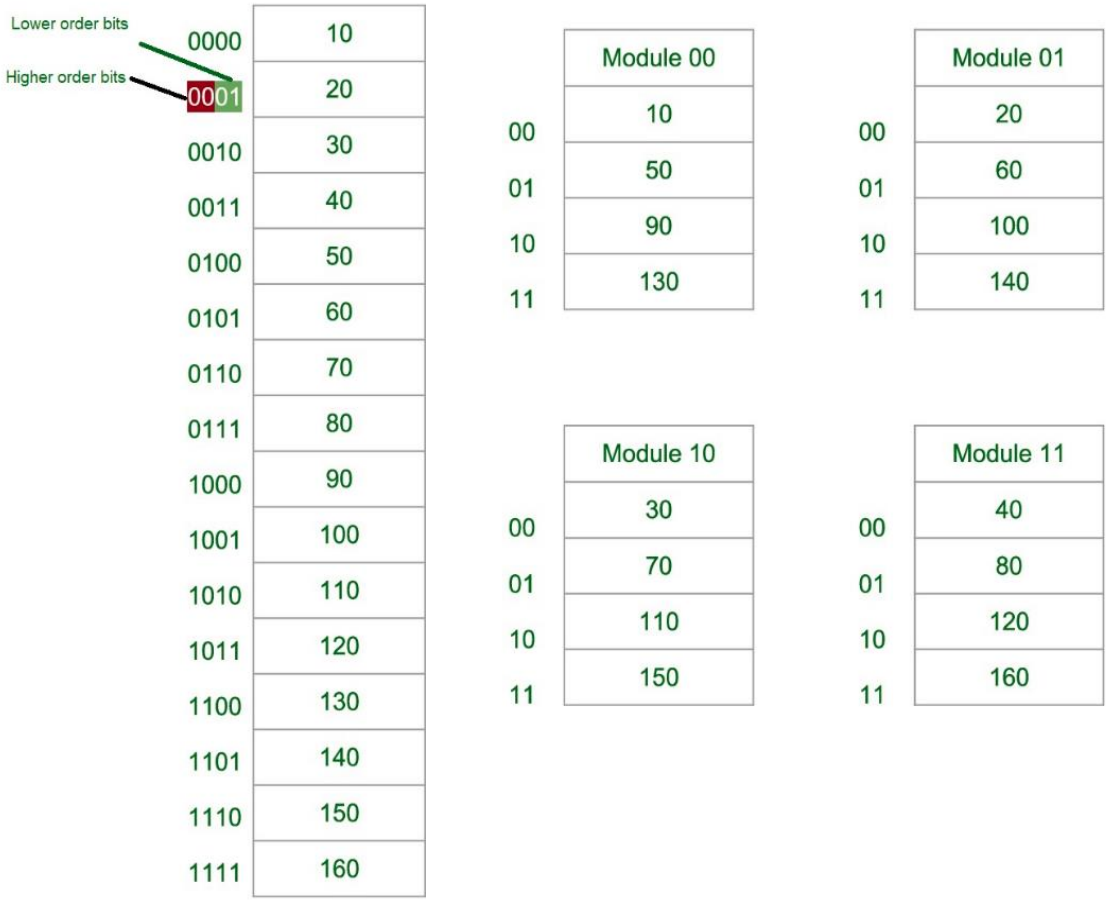

Figure: Consecutive Word in Consecutive Module

Least Significant Bit (***LSB***) provides the ***Address of the Module*** & Most Significant Bit (***MSB***) provides the ***Address of the Data*** in the module.

Example: to get 90 (Data) 1000 will be provided by the processor. This 00 will indicate that the data is in module 00 (module 1) & 10 is the address of 90 in Module 00 (module 1).

```
Module 1 Contains Data : 10, 50, 90, 130
Module 2 Contains Data : 20, 60, 100, 140
Module 3 Contains Data : 30, 70, 110, 150
Module 4 Contains Data : 40, 80, 120, 160
```

➢ How Does the Interleaved Memory Works ?

- When the CPU requests data, the ***Memory Controller*** determines which bank contains the requested address.
  Memory Controller: The component that manages memory accesses and determines which bank to access.
- Because consecutive addresses are in different banks, the controller can initiate multiple memory accesses in ***parallel***.
- This significantly increases the memory bandwidth, allowing the CPU to retrieve data more quickly.
- Essentially, it allows for overlapping memory access operations, rather than having to wait for each one to fully complete before starting the next.

➢ Advantages of Memory Interleaving

1- Reduced Memory Latency: By overlapping memory accesses, interleaving helps to reduce the effective latency of memory operations.

2- We can access all Modules at the same time thus achieving Parallelism. This method uses memory effectively.

3- Increased Memory Bandwidth: The primary benefit is a significant improvement in memory bandwidth, which translates to faster overall system performance.