Logical Design

Lecture 8: Combinational Circuits

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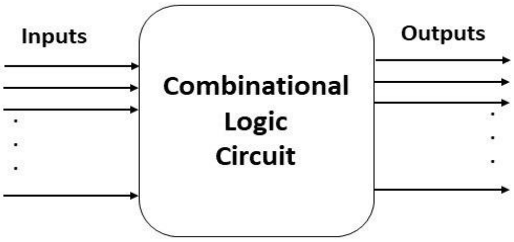
Digital circuits

Digital circuits can be categorized into two types: Combinational circuits and sequential circuits.

Combinational circuit

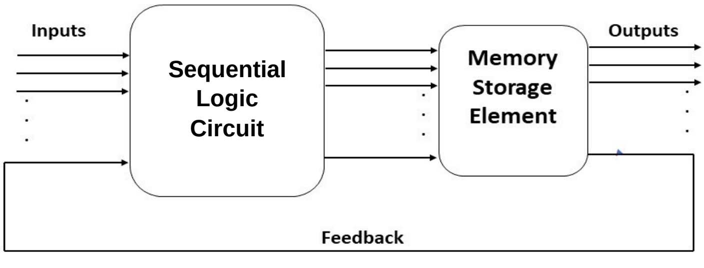
• Output of combinational circuit based on the combination of present input only.



• No feedback
• No memory
• Ex: encoder, decoder, multiplexer, demultiplexer, adder, and subtractor.

Sequential circuit

- The output of a sequential circuit depends on the current input and a previous output.



- Feedback is present
- Memory is present
- Ex: Flipflop, Registers and Counters

Combinational Circuits

Connecting logical gates together to produce a specified output with no storage involved. Combinational circuits are divided into three main parts:

1. ***Arithmetic and logical function***

Adder, Subtractor, and Comparator.

2. ***Code convertors***

Binary, Gray, and BCD

3. ***Data transmission***

Encoder, Decoder, Multiplexer, and Demultiplexer.

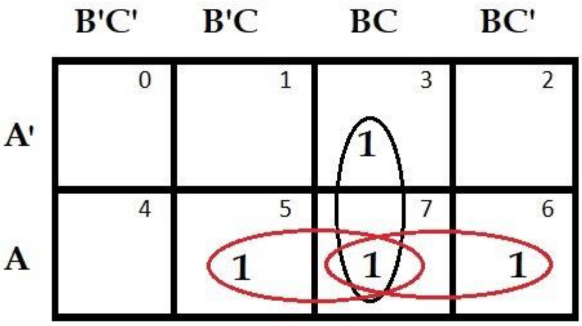
Design a combinational circuit

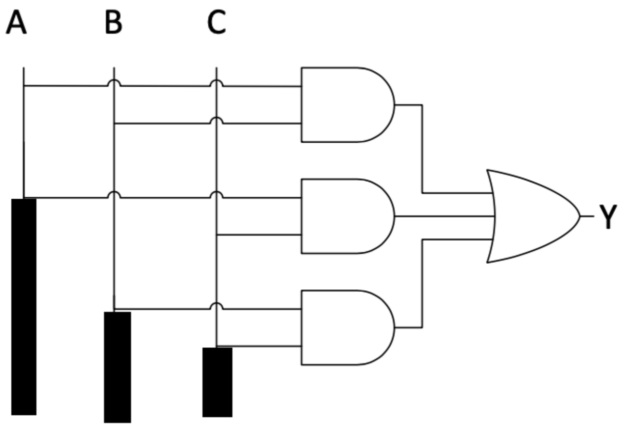
Example: Design a combinational circuit with three variables that will produce a logic 1 output when more than one input variable is at logic 1.

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

$$Y = \overline{A}BC + A\overline{B}C + AB\overline{C} + ABC$$

After simplification as follows:





Y=AC+AB+BC

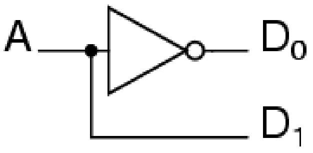
Decoder

A **decoder** is a combinational logic circuit that is used to change the code into a set of signals. It is called a decoder because it does the reverse of encoding. decoder which takes an n-digit binary number and decodes it into 2^n data lines. The simplest is the 1-to-2 line decoder. The truth table is:

A	D_1	D_0
0	0	1
1	1	0

⇨

A is the address and ***D*** is the data-line. ***D_0*** is NOT A and ***D_1*** is A. The circuit looks like



2-to-4 Line Decoder

The truth table is:

A_1	A_0	D_3	D_2	D_1	D_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

The equations are:

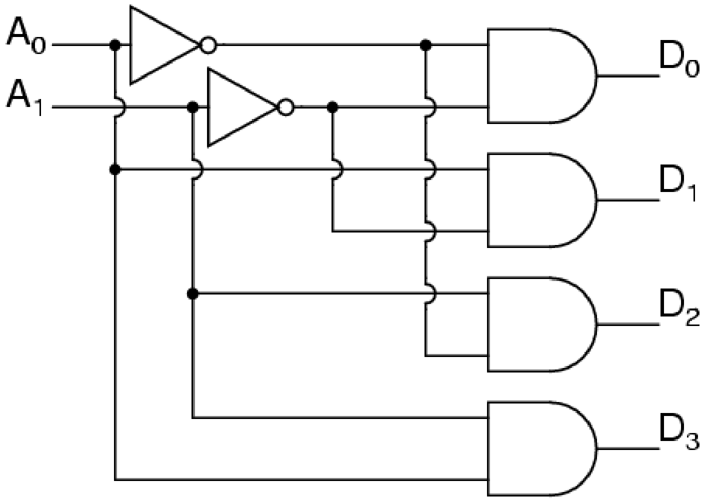
$$D_0 = \overline{A_1} \cdot \overline{A_0}$$

$$D_1 = \overline{A_1} \cdot A_0$$

$$D_2 = A_1 \cdot \overline{A_0}$$

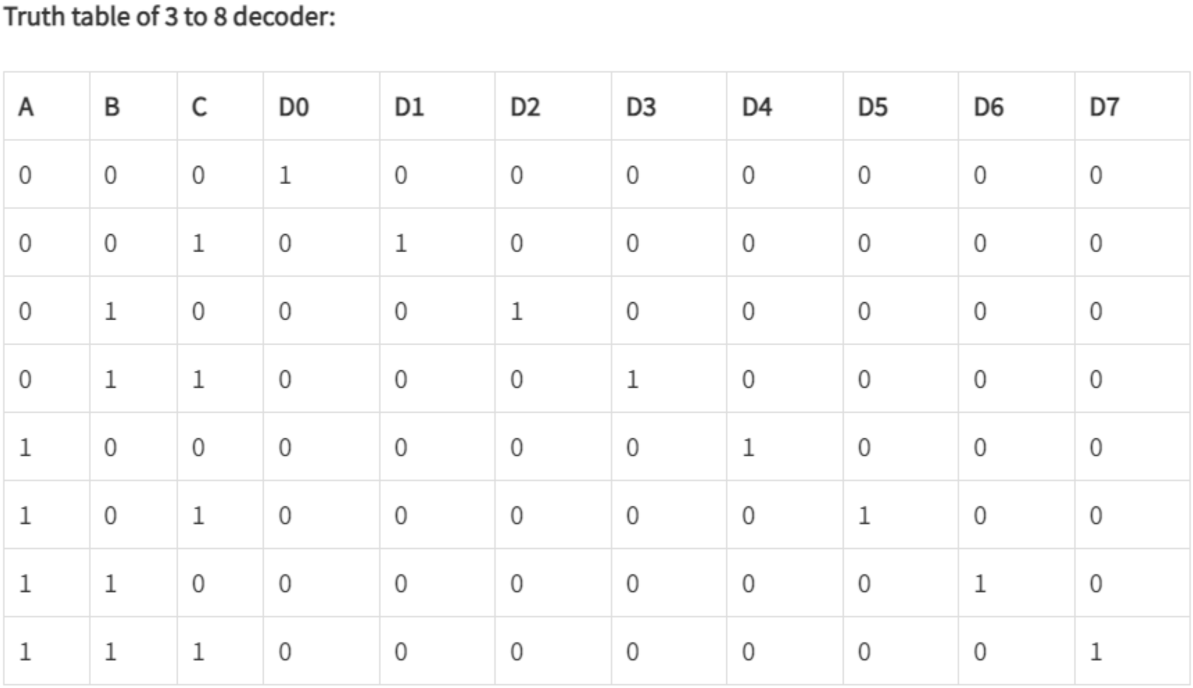
$$D_3 = A_1 \cdot A_0$$

The 2-to-4 decoder logic circuit is



3 to 8 Decoder

- A 3 to 8 decoder has three inputs (A, B, C) and eight outputs (D0 to D7).
- Based on the 3 inputs ***one*** of the eight outputs is selected.
- The truth table for 3 to 8 decoder is shown in the below table.



Truth table of 3 to 8 decoder:

A	B	C	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

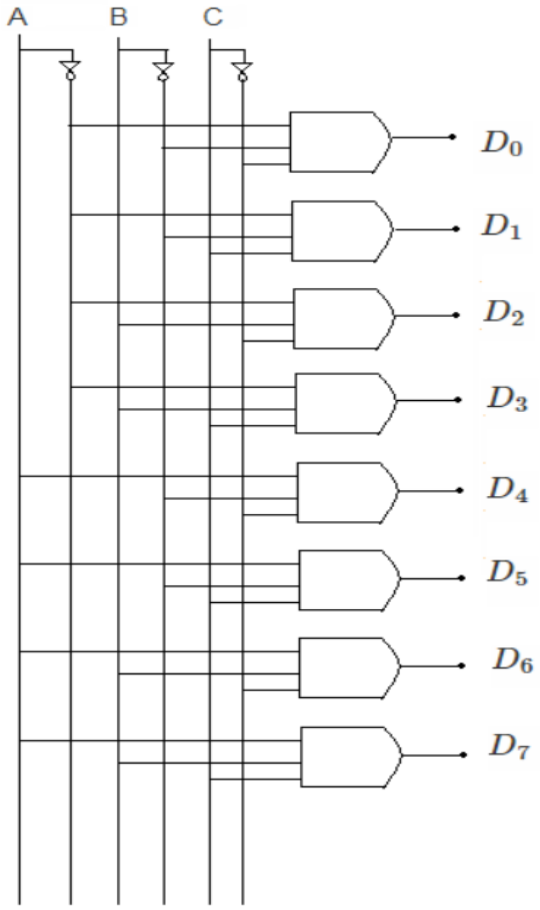
- From the truth table, it is seen that only one of eight outputs (D0 to D7) is selected based on three select inputs.
- From the truth table, the logic expressions for outputs can be written as follows:

$$D_0 = \bar{A}\bar{B}\bar{C}, \quad D_1 = \bar{A}\bar{B}C, \quad D_2 = \bar{A}B\bar{C},$$

$$D_3 = \bar{A}BC, \quad D_4 = A\bar{B}\bar{C}, \quad D_5 = A\bar{B}C,$$

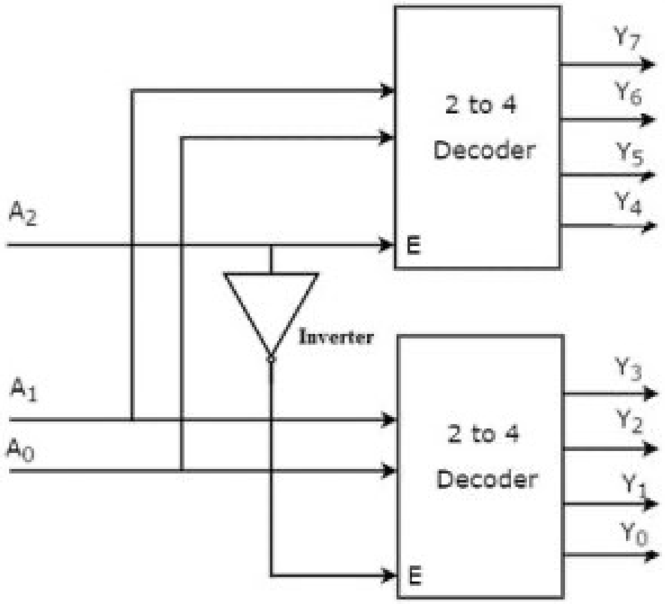
$$D_6 = AB\bar{C}, \quad D_7 = ABC$$

- Using the above expressions, the circuit of a 3 to 8 decoder can be implemented using three NOT gates and eight 3-input AND gates as shown in the following figure.



Building a 3-to-8 decoders using 2-to-4 decoders

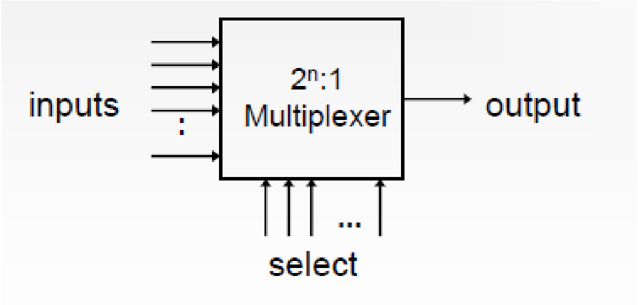
The implementation of this 3 line to 8 line decoder can be done using two 2 lines to 4 line decoders. We have discussed above that 2 to 4 line decoder includes two inputs and four outputs. So, in 3 lines to 8 line decoder, it includes three inputs like A2, A1 & A0 and 8 outputs from Y7 – Y0. In addition to input pins, the decoder has a ***Enable Pin***.



Multiplexers (MUX)

The multiplexer is a combinational logic circuit designed to switch one of several input lines to a single common output line.

It steers one of 2^n inputs to a single output line, using n selection lines. Also known as a ***data selector***.



Routes one of its N data inputs to its one output, based on the binary value of select inputs:

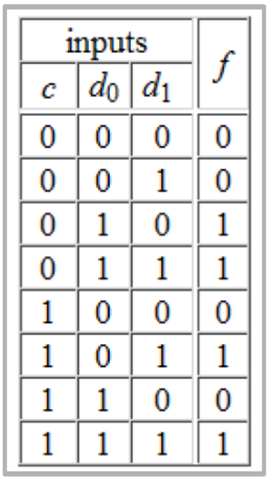
- ✓ 4 input mux needs 2 select inputs to indicate which input to route through.
- ✓ 8 input mux needs 3 select inputs.
- ✓ N inputs →$\log_2(N)$ selects.

MUX Advantages:

1. Reduce the number of wires.
2. Reduce circuit complexity and cost.
3. The multiplexer is a very useful electronic circuit that has uses in many different applications such as signal routing, data communications, and data bus control applications.
4. Helps share a single communication line among a number of devices.
5. At any time, only one source and one destination can use the communication line.

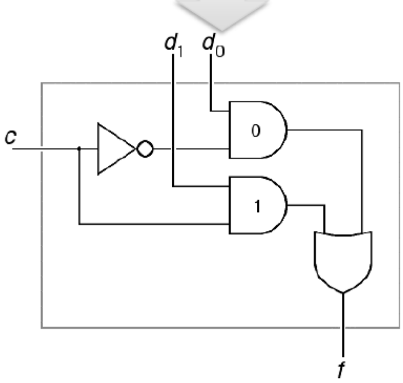
2-input multiplexor

The truth table for a multiplexor with **2** data inputs ***d*₀** and ***d*₁** and one control input ***c*** is as follows:

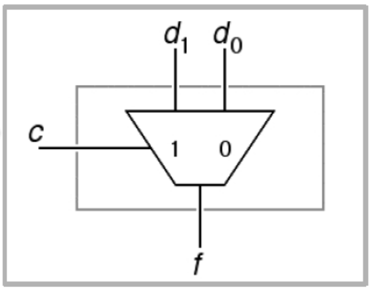


inputs			f
c	d_0	d_1	
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

$$f = (d_0\,\bar{c}) + (d_1\,c)$$

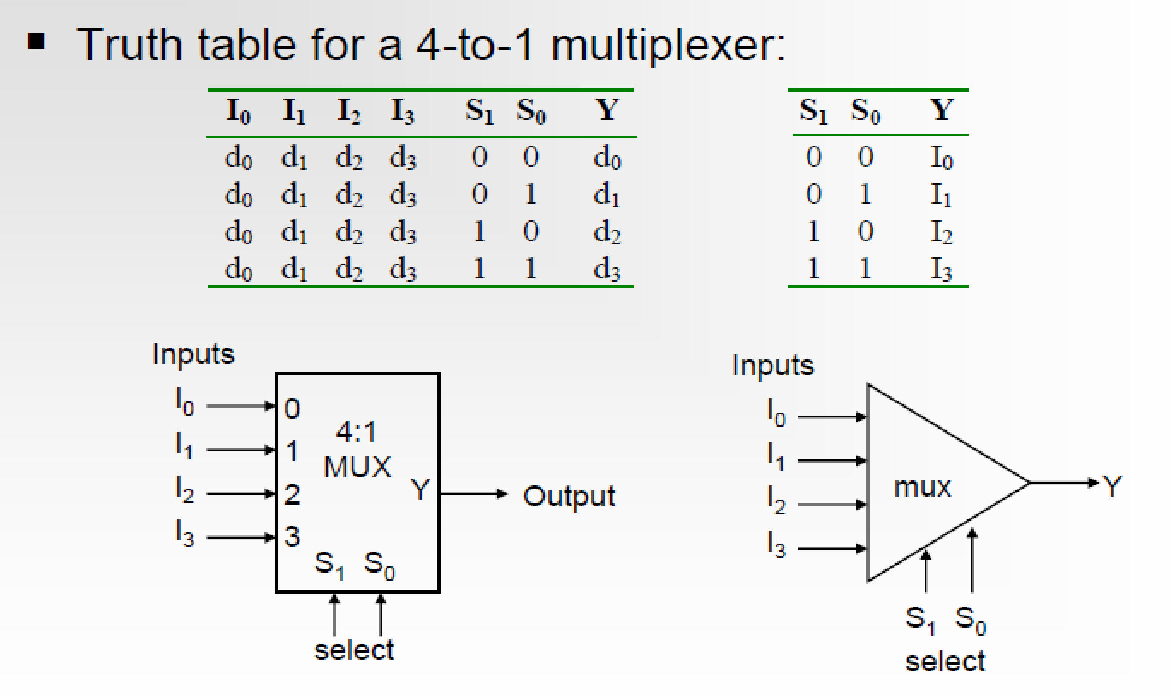


logic circuit involving only 4 gates



schematic symbol

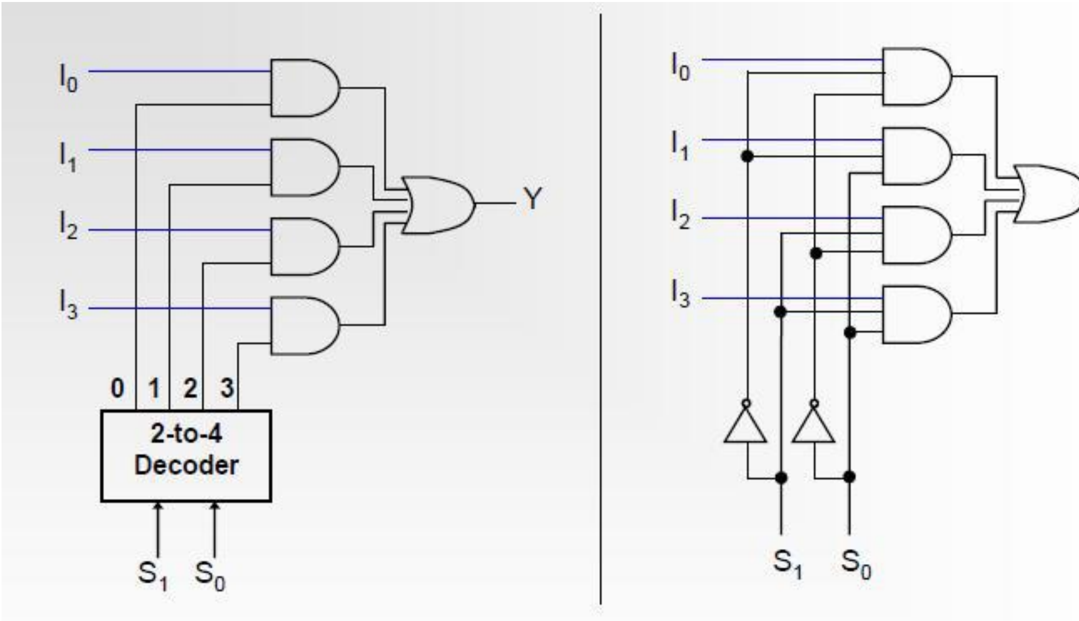
4-input multiplexor



- Truth table for a 4-to-1 multiplexer:

I_0	I_1	I_2	I_3	S_1	S_0	Y
d_0	d_1	d_2	d_3	0	0	d_0
d_0	d_1	d_2	d_3	0	1	d_1
d_0	d_1	d_2	d_3	1	0	d_2
d_0	d_1	d_2	d_3	1	1	d_3

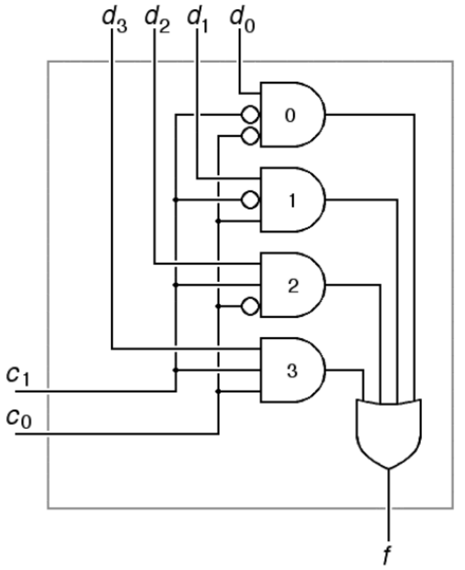
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

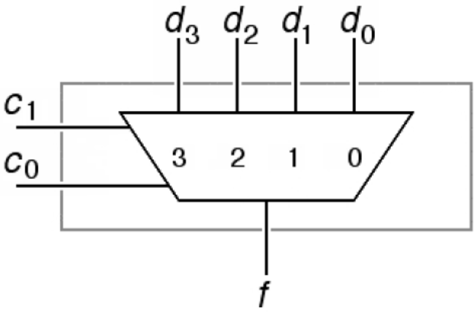


Four-to-one multiplexer design.

Gate-level design for a 4-input multiplexor

$$f = (d_0\, c'_1\, c'_0) + (d_1\, c'_1\, c_0) + (d_2\, c_1\, c'_0) + (d_3\, c_1\, c_0)$$



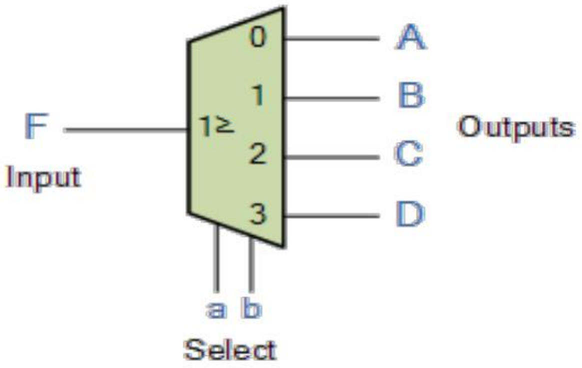


schematic symbol

Demultiplexers (Demux)

The ***demultiplexer*** is a combinational logic circuit designed to switch one common input line to one of several separate output lines.

The ***demultiplexer*** takes one single input data line and then switches it to any one of a number of individual output lines one at a time. The ***demultiplexer*** converts a serial data signal at the input to parallel data at its output lines as shown in the figure.


0
1
2
3
A
B
C
D
Outputs
F
Input
1≥
a
b
Select