Pins and signals of 8086

Overview

First 16- bit processor released by INTEL in the year 1978

Originally HMOS, now manufactured using HMOS III technique
(HMOS: High Performance Metal Oxide Semiconductor).

Approximately 29, 000 transistors, 40 pin DIP, 5V supply

Does not have internal clock; external asymmetric clock source with 33% duty cycle

20-bit address to access memory $\Rightarrow$ can address up to $2^{20} = 1$ megabytes of memory space.

Addressable memory space is organized in to two banks of 512 kb each; Even (or lower) bank and Odd (or higher) bank. Address line A_0 is used to select even bank and control signal $\overline{BHE}$ is used to access odd bank

Uses a separate 16 bit address for I/O mapped devices $\Rightarrow$ can generate $2^{16} = 64$ k addresses.

Operates in two modes: minimum mode and maximum mode, decided by the signal at MN and $\overline{MX}$ pins.

Pins and Signals
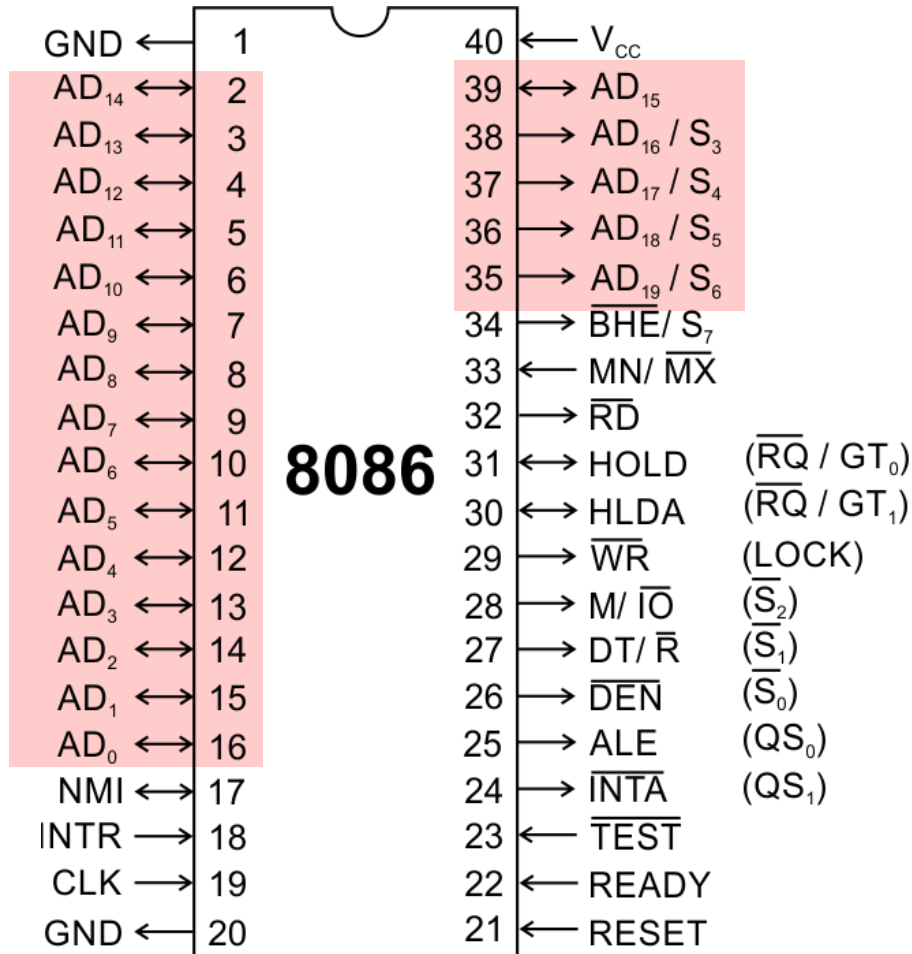
AD_0-AD_{15} (Bidirectional)

Address/Data bus

Low order address bus; these are multiplexed with data.
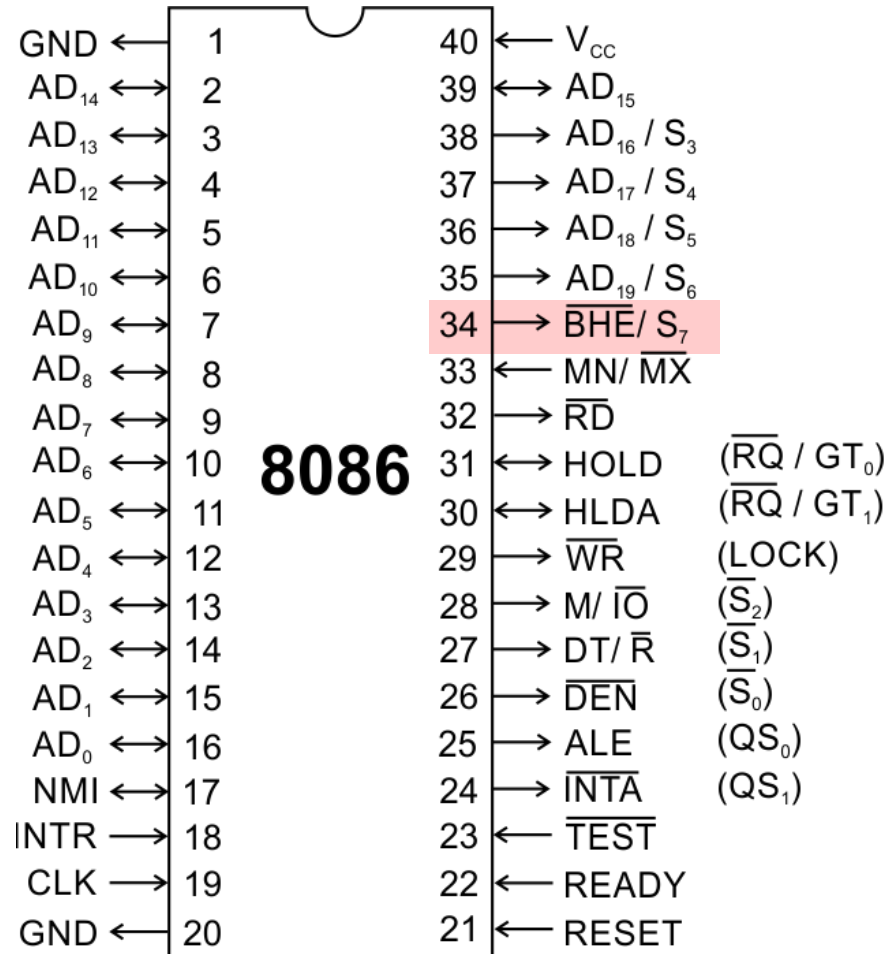
When AD lines are used to transmit memory address the symbol A is used instead of AD, for example A_0-A_{15}.

When data are transmitted over AD lines the symbol D is used in place of AD, for example D_0-D_7, D_8-D_{15} or D_0-D_{15}.

A_{16}/S_3, A_{17}/S_4, A_{18}/S_5, A_{19}/S_6

High order address bus. These are multiplexed with status signals

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Pins and Signals

```
GND  ←──  1        40  ←──  V_CC
AD14 ←──→ 2        39  ←──→ AD15
AD13 ←──→ 3        38  ──→  AD16 / S3
AD12 ←──→ 4        37  ──→  AD17 / S4
AD11 ←──→ 5        36  ──→  AD18 / S5
AD10 ←──→ 6        35  ──→  AD19 / S6
AD9  ←──→ 7        34  ──→  BHE/ S7
AD8  ←──→ 8        33  ←──  MN/ MX
AD7  ←──→ 9        32  ──→  RD
AD6  ←──→ 10  8086 31  ←──→ HOLD    (RQ / GT0)
AD5  ←──→ 11       30  ←──→ HLDA    (RQ / GT1)
AD4  ←──→ 12       29  ──→  WR      (LOCK)
AD3  ←──→ 13       28  ──→  M/ IO   (S2)
AD2  ←──→ 14       27  ──→  DT/ R   (S1)
AD1  ←──→ 15       26  ──→  DEN     (S0)
AD0  ←──→ 16       25  ──→  ALE     (QS0)
NMI  ←──→ 17       24  ──→  INTA    (QS1)
INTR ──→  18       23  ←──  TEST
CLK  ──→  19       22  ←──  READY
GND  ←──  20       21  ←──  RESET
```

BHE (Active Low)/S_7 (Output)

Bus High Enable/Status

It is used to enable data onto the most significant half of data bus, D_8-D_{15}. 8-bit device connected to upper half of the data bus use BHE (Active Low) signal. It is multiplexed with status signal S_7.
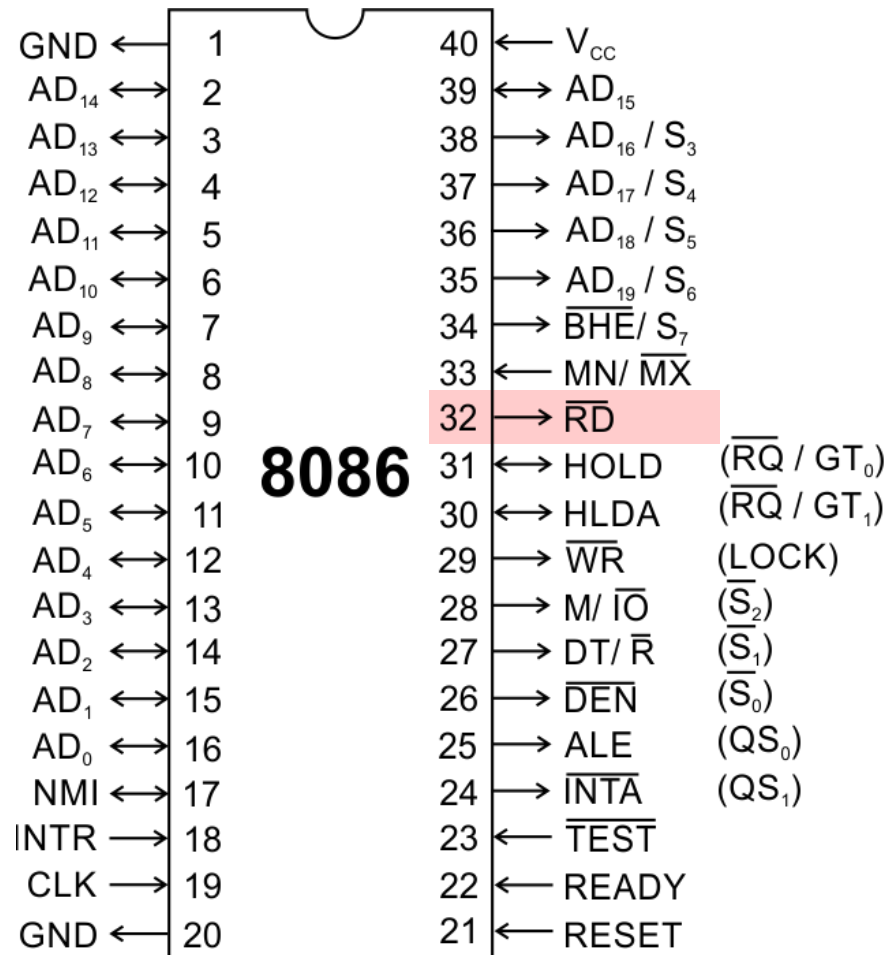
MN/ MX

MINIMUM / MAXIMUM

This pin signal indicates what mode the processor is to operate in.

RD (Read) (Active Low)

The signal is used for read operation.
It is an output signal.
It is active when low.

8086 Microprocessor

Pins and Signals


```
GND    ← 1        40 ← Vcc
AD14   ↔ 2        39 ↔ AD15
AD13   ↔ 3        38 → AD16 / S3
AD12   ↔ 4        37 → AD17 / S4
AD11   ↔ 5        36 → AD18 / S5
AD10   ↔ 6        35 → AD19 / S6
AD9    ↔ 7        34 → BHE/ S7
AD8    ↔ 8        33 ← MN/ MX
AD7    ↔ 9        32 → RD
AD6    ↔ 10       31 ↔ HOLD     (RQ / GT0)
AD5    ↔ 11       30 ↔ HLDA     (RQ / GT1)
AD4    ↔ 12       29 → WR       (LOCK)
AD3    ↔ 13       28 → M/ IO    (S2)
AD2    ↔ 14       27 → DT/ R    (S1)
AD1    ↔ 15       26 → DEN      (S0)
AD0    ↔ 16       25 → ALE      (QS0)
NMI    ↔ 17       24 → INTA     (QS1)
INTR   → 18       23 ← TEST
CLK    → 19       22 ← READY
GND    ← 20       21 ← RESET
```

8086

TEST

$\overline{\text{TEST}}$ input is tested by the 'WAIT' instruction.

8086 will enter a wait state after execution of the WAIT instruction and will resume execution only when the $\overline{\text{TEST}}$ is made low by an active hardware.

This is used to synchronize an external activity to the processor internal operation.
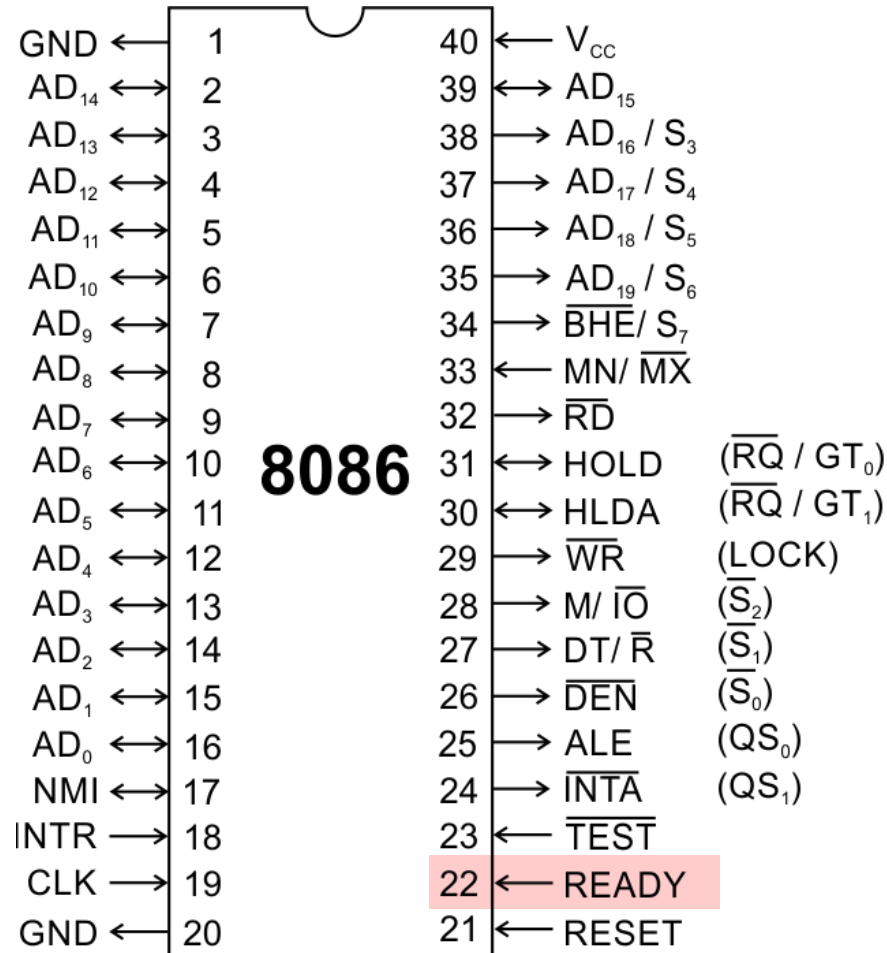
READY

This is the acknowledgement from the slow device or memory that they have completed the data transfer.

The signal made available by the devices is synchronized by the 8284A clock generator to provide ready input to the 8086.

The signal is active high. [5]

8086 Microprocessor

Common signals

Pins and Signals

Pin	Signal
1	GND
2	AD₁₄
3	AD₁₃
4	AD₁₂
5	AD₁₁
6	AD₁₀
7	AD₉
8	AD₈
9	AD₇
10	AD₆
11	AD₅
12	AD₄
13	AD₃
14	AD₂
15	AD₁
16	AD₀
17	NMI
18	INTR
19	CLK
20	GND

Pin	Signal
40	V_cc
39	AD₁₅
38	AD₁₆ / S₃
37	AD₁₇ / S₄
36	AD₁₈ / S₅
35	AD₁₉ / S₆
34	$\overline{BHE}$/ S₇
33	MN/ $\overline{MX}$
32	$\overline{RD}$
31	HOLD ($\overline{RQ}$ / GT₀)
30	HLDA ($\overline{RQ}$ / GT₁)
29	$\overline{WR}$ (LOCK)
28	M/ $\overline{IO}$ ($\overline{S_2}$)
27	DT/ $\overline{R}$ ($\overline{S_1}$)
26	$\overline{DEN}$ ($\overline{S_0}$)
25	ALE (QS₀)
24	$\overline{INTA}$ (QS₁)
23	$\overline{TEST}$
22	READY
21	RESET

8086

RESET (Input)

Causes the processor to immediately terminate its present activity.

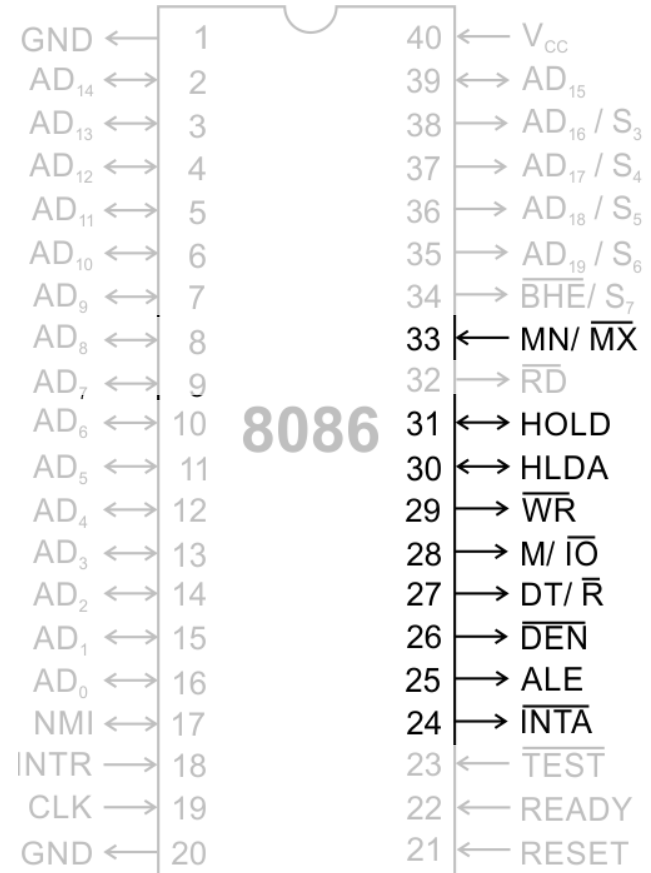The signal must be active HIGH for at least four clock cycles.

CLK

The clock input provides the basic timing for processor operation and bus control activity. Its an asymmetric square wave with 33% duty cycle.

INTR Interrupt Request

This is a triggered input. This is sampled during the last clock cycles of each instruction to determine the availability of the request. If any interrupt request is pending, the processor enters the interrupt acknowledge cycle.

This signal is active high and internally synchronized.

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Pins and Signals

Min/ Max Pins

The 8086 microprocessor pin diagram:

Pin	Signal		Pin	Signal
1	GND		40	V_{CC}
2	AD_{14}		39	AD_{15}
3	AD_{13}		38	AD_{16} / S_3
4	AD_{12}		37	AD_{17} / S_4
5	AD_{11}		36	AD_{18} / S_5
6	AD_{10}		35	AD_{19} / S_6
7	AD_9		34	$\overline{BHE}/ S_7$
8	AD_8		33	MN/ $\overline{MX}$
9	AD_7		32	$\overline{RD}$
10	AD_6		31	HOLD
11	AD_5		30	HLDA
12	AD_4		29	$\overline{WR}$
13	AD_3		28	M/ $\overline{IO}$
14	AD_2		27	DT/ $\overline{R}$
15	AD_1		26	$\overline{DEN}$
16	AD_0		25	ALE
17	NMI		24	$\overline{INTA}$
18	INTR		23	$\overline{TEST}$
19	CLK		22	READY
20	GND		21	RESET

8086

The 8086 microprocessor can work in two modes of operations : Minimum mode and Maximum mode.
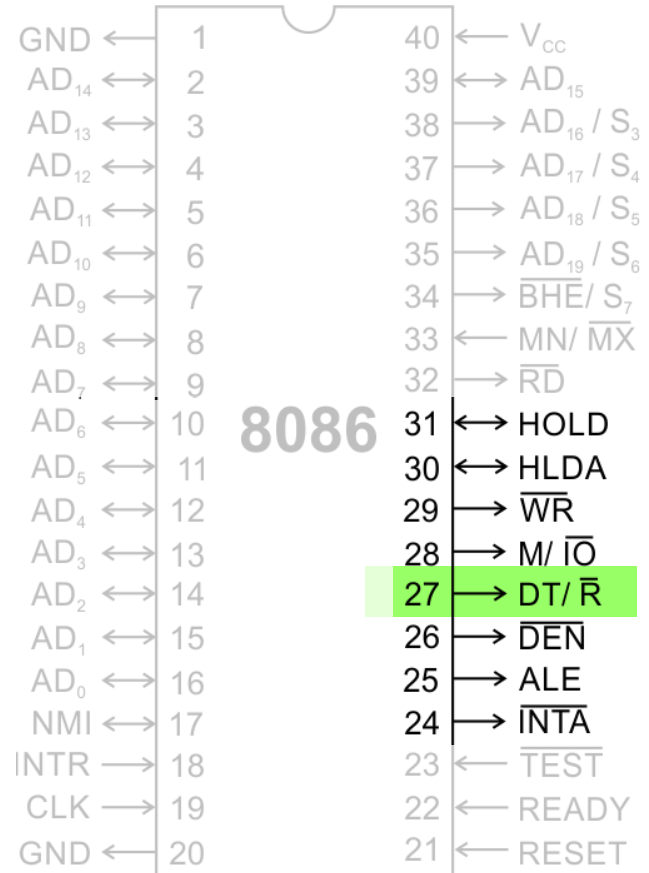
In the **minimum mode** of operation the microprocessor **do not** associate with any co-processors and can not be used for multiprocessor systems.

In the **maximum mode** the 8086 **can work** in multi-processor or co-processor configuration.

Minimum or maximum mode operations are decided by the pin MN/ MX(Active low).

When this pin is high 8086 operates in minimum mode otherwise it operates in Maximum mode.
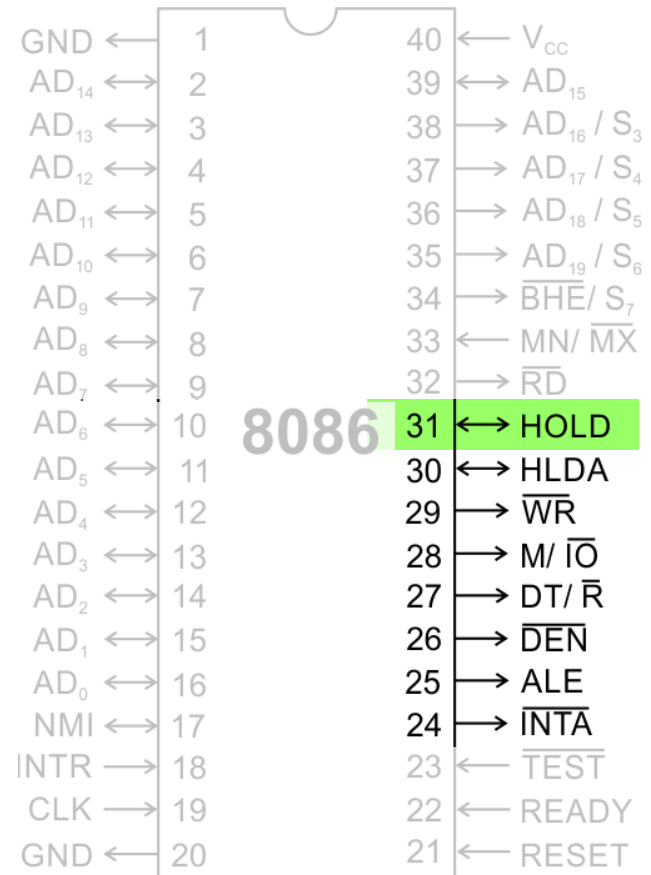
Pins and Signals

Pins 24 -31

For minimum mode operation, the MN/ $\overline{MX}$ is tied to VCC (logic high)

8086 itself generates all the bus control signals

Signal	Description
DT/$\overline{R}$	(**Data Transmit/ Receive**) Output signal from the processor to control the direction of data flow through the data transceivers
$\overline{DEN}$	(**Data Enable**) Output signal from the processor used as out put enable for the transceivers
ALE	(**Address Latch Enable**) Used to demultiplex the address and data lines using external latches
M/$\overline{IO}$	Used to differentiate memory access and I/O access. For memory reference instructions, it is **high**. For IN and OUT instructions, it is **low**.
$\overline{WR}$	Write control signal; asserted **low** Whenever processor writes data to memory or I/O port
$\overline{INTA}$	(**Interrupt Acknowledge**) When the interrupt request is accepted by the processor, the output is **low** on this line.

8086 pin diagram:

GND — 1 ... 40 ← V_{CC}
AD_{14} — 2 ... 39 ↔ AD_{15}
AD_{13} — 3 ... 38 → AD_{16}/S_3
AD_{12} — 4 ... 37 → AD_{17}/S_4
AD_{11} — 5 ... 36 → AD_{18}/S_5
AD_{10} — 6 ... 35 → AD_{19}/S_6
AD_9 — 7 ... 34 → $\overline{BHE}/S_7$
AD_8 — 8 ... 33 ← MN/$\overline{MX}$
AD_7 — 9 ... 32 → $\overline{RD}$
AD_6 — 10 ... 8086 ... 31 ↔ HOLD
AD_5 — 11 ... 30 ↔ HLDA
AD_4 — 12 ... 29 → $\overline{WR}$
AD_3 — 13 ... 28 → M/$\overline{IO}$
AD_2 — 14 ... 27 → DT/$\overline{R}$
AD_1 — 15 ... 26 → $\overline{DEN}$
AD_0 — 16 ... 25 → ALE
NMI — 17 ... 24 → $\overline{INTA}$
INTR — 18 ... 23 ← $\overline{TEST}$
CLK — 19 ... 22 ← READY
GND — 20 ... 21 ← RESET

Pins and Signals

Pins 24 -31

For minimum mode operation, the MN/ $\overline{\text{MX}}$ is tied to VCC (logic high)

**8086 itself generates all the bus control signals**

```
GND  ←  1        40  ←  V_CC
AD_14 ←→ 2        39  ←→ AD_15
AD_13 ←→ 3        38  →  AD_16 / S_3
AD_12 ←→ 4        37  →  AD_17 / S_4
AD_11 ←→ 5        36  →  AD_18 / S_5
AD_10 ←→ 6        35  →  AD_19 / S_6
AD_9  ←→ 7        34  →  BHE / S_7
AD_8  ←→ 8        33  ←  MN/ MX
AD_7  ←→ 9        32  →  RD
AD_6  ←→ 10  8086 31  ←→ HOLD
AD_5  ←→ 11       30  ←→ HLDA
AD_4  ←→ 12       29  →  WR
AD_3  ←→ 13       28  →  M/ IO
AD_2  ←→ 14       27  →  DT/ R
AD_1  ←→ 15       26  →  DEN
AD_0  ←→ 16       25  →  ALE
NMI   ←→ 17       24  →  INTA
INTR  →  18       23  ←  TEST
CLK   →  19       22  ←  READY
GND   ←  20       21  ←  RESET
```

HOLD   Input signal to the processor form the bus masters as a request to grant the control of the bus.

Usually used by the DMA controller to get the control of the bus.

HLDA   (**Hold Acknowledge**) Acknowledge signal by the processor to the bus master requesting the control of the bus through HOLD.

The acknowledge is asserted high, when the processor accepts HOLD.

Pins and Signals
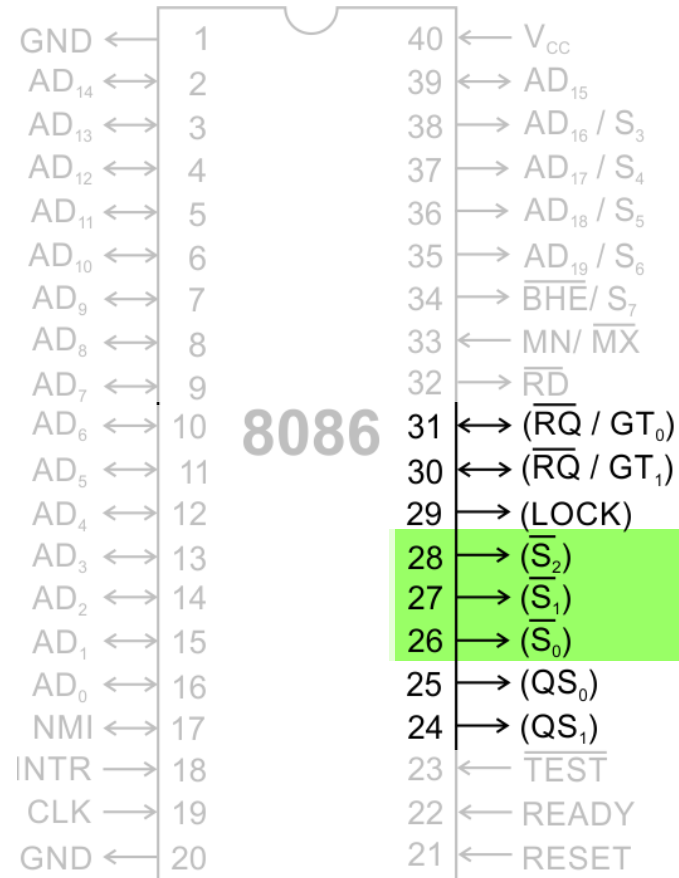
During maximum mode operation, the MN/ $\overline{\text{MX}}$ is grounded (logic low)
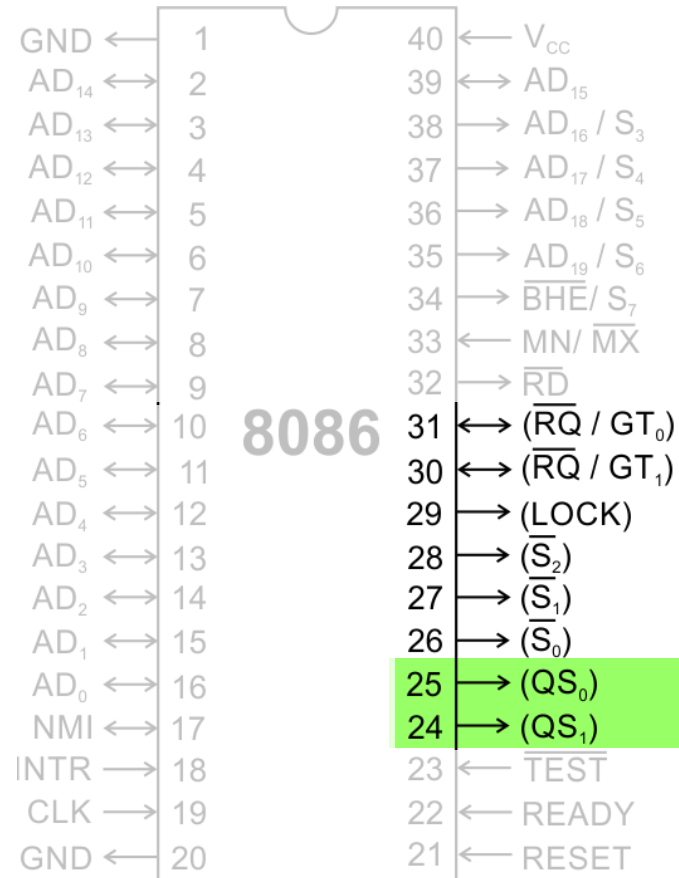
Pins 24 -31 are reassigned

$\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$ **Status signals; used by the 8086 bus controller to generate bus timing and control signals. These are decoded as shown.**

Status Signal			Machine Cycle
$\overline{S}_2$	$\overline{S}_1$	$\overline{S}_0$	
0	0	0	Interrupt acknowledge
0	0	1	Read I/O port
0	1	0	Write I/O port
0	1	1	Halt
1	0	0	Code access
1	0	1	Read memory
1	1	0	Write memory
1	1	1	Passive/Inactive

Pins and Signals

During maximum mode operation, the MN/ $\overline{MX}$ is grounded (logic low)

Pins 24 -31 are reassigned

$\overline{QS_0}$, $\overline{QS_1}$ (**Queue Status**) The processor provides the status of queue in these lines.

The queue status can be used by external device to track the internal status of the queue in 8086.

The output on QS_0 and QS_1 can be interpreted as shown in the table.

Queue status		Queue operation
QS_1	QS_0	
0	0	No operation
0	1	First byte of an opcode from queue
1	0	Empty the queue
1	1	Subsequent byte from queue

8086 Microprocessor

Pins and Signals
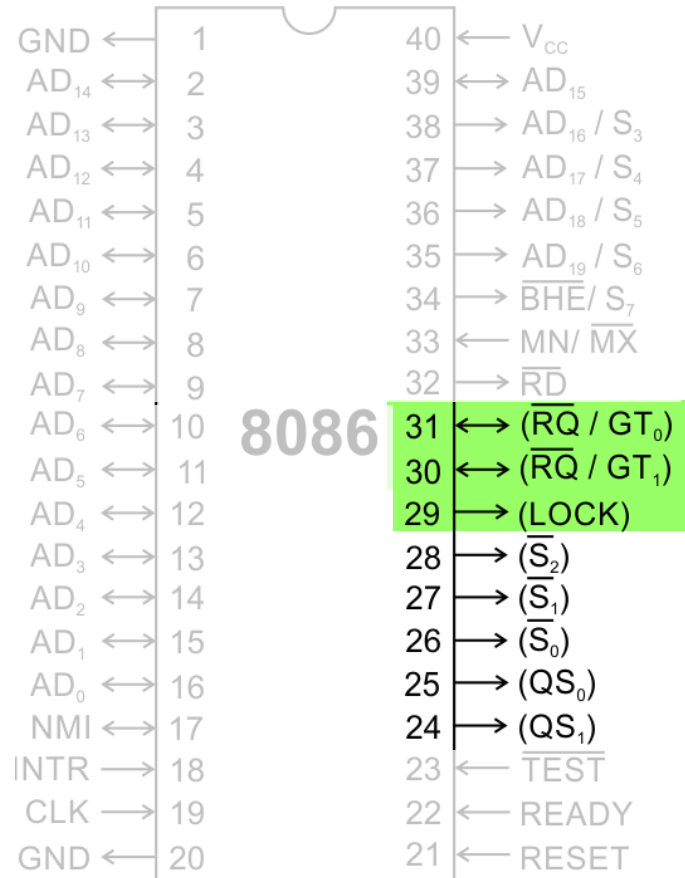
During maximum mode operation, the MN/ $\overline{MX}$ is grounded (logic low)

Pins 24 -31 are reassigned

$\overline{RQ}/\overline{GT_0}$, $\overline{RQ}/\overline{GT_1}$

(**Bus Request/ Bus Grant**) These requests are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle.

These pins are bidirectional.

The request on $\overline{GT_0}$ will have higher priority than $\overline{GT_1}$

$\overline{LOCK}$

An output signal activated by the LOCK prefix instruction.

Remains active until the completion of the instruction prefixed by LOCK.

The 8086 output low on the $\overline{LOCK}$ pin while executing an instruction prefixed by LOCK to <u>prevent other bus masters from gaining control of the system bus.</u>