The 8086 Microprocessor Hardware Specifications

Pin Diagram and Pin Description of 8086 Microprocessor

The 8086 can be configured to work in one of the following two modes:

♦The **Minimum Mode** is selected by applying logic 1 to the MN/$\overline{MX}$ input. It is typically used for smaller single microprocessor systems.

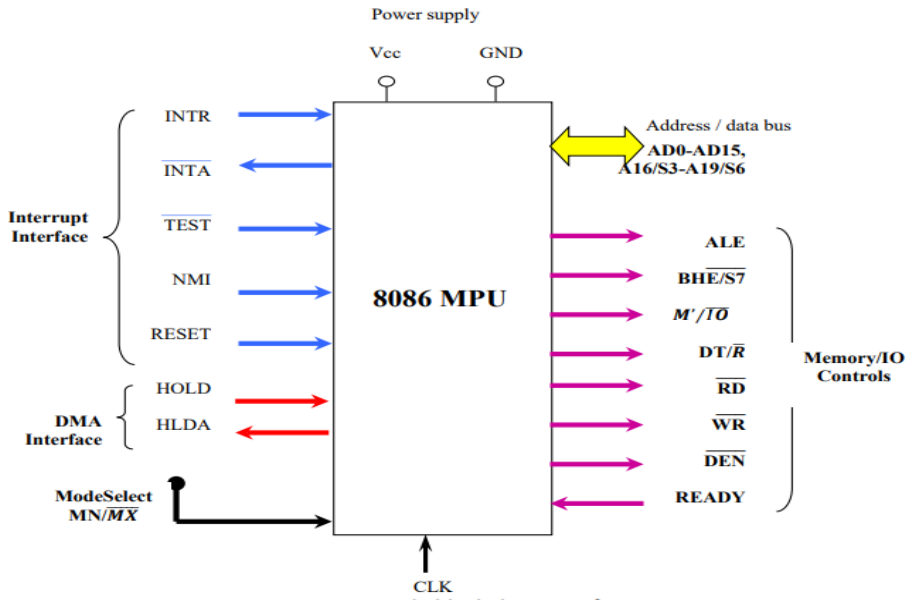
♦The **Maximum Mode** is selected by applying logic 0 to the MN/$\overline{MX}$ input. It is typically used for larger multiple microprocessor systems.

Depending on the mode of operation selected, the 8086 signals can be categorized in three groups.

- The first are the signal having common functions in minimum as well as maximum mode.
- The second are the signals, which have special functions for minimum mode.
- The third are the signals having special functions for maximum mode.

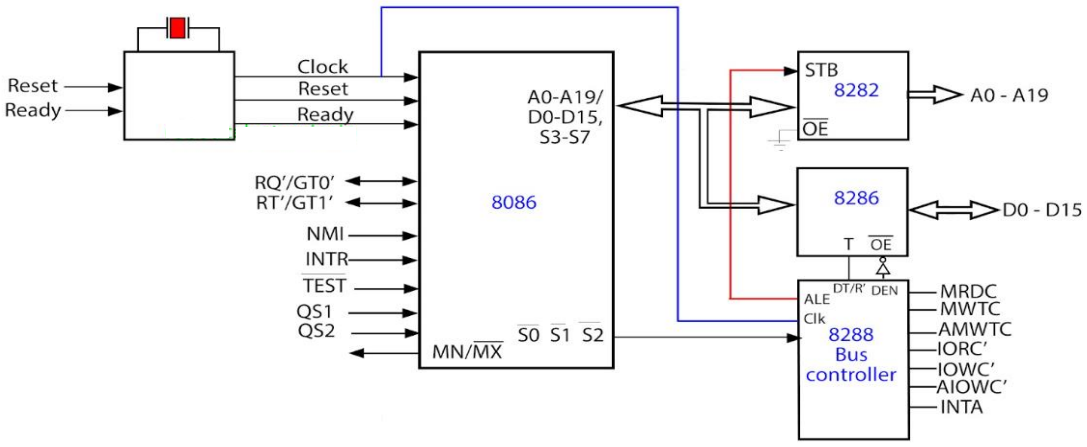
Minimum mode Operation

- Figure below show block diagram of minimum mode.
- Minimum mode operation is the least expensive way to operate the 8086.
- In minimum mode, the 8086 itself provides all the control signals needed to implement the memory and I/O interfaces.
- These control signals are identical to those of the Intel 8085 an earlier 8-bit microprocessor.
- This mode allows the 8085 peripherals to be used with the 8086 without any special consideration.



Maximum mode Operation

- Figure below show block diagram of maximum mode**.**
- This mode supports existence of more than one processor in a system i.e. multiprocessor system**.**
- In a multiprocessor system environment, more than one processor exists in the system, and each processor is executing its own program**.**
- In maximum mode, the 8086 provides facilities by generating some of the control signals externally**.**
- In maximum-mode, a separate chip (the 8288 Bus Controller) is used to help in sending control signals over the shared bus.



❖ The signals common for both minimum & maximum modes:

Common Signals	
Name	**Function**
AD15-AD0	Address/Data Bus
A19/S6 - A16/S3	Address/Status
MN / $\overline{MX}$	Minimum/Maximum mode control
$\overline{RD}$	Read Control
$\overline{TEST}$	Wait on test control
$\overline{READY}$	Wait state control
RESET	System reset
CLK	System clock
Vcc	+5V
GND	Ground
$\overline{BHE}$ /S7	Bus High Enable/Status
INTR	Interrupt Request
NMI	non maskable interrupt Request

- ***Address/Data Bus (AD15-AD0):*** These are 16 address/data bus. AD0-AD7 carries low order byte data and AD8-AD15 carries higher order byte data. During the first clock cycle, it carries 16-bit address and after that it carries 16-bit data.
- ***Address/Status signals (A19/S6, A18/S5, A17/S4, A16/S3):*** These are the multiplexed pins to provide address signals (A19-A16) and status lines (S6-S3). *Bit S6 always remains logic 0*, bit *S5* indicates the condition of *interrupt flag* (IF) bits. *S4 and S3* together form a 2-bit binary code that identifies which of the *internal segment registers* was used to generate the physical address that was output on the address bus during the current bus cycle.

S4	S3	Indication
0	0	Extra Data Segment
0	1	Stack Segment
1	0	Code or No Segment
1	1	Data Segment

- ***MN/$\overline{MX}$:*** Is an input pin used to select one of this mode .when MN/$\overline{MX}$ is high the 8086 operates in minimum mode .In this mode the 8086 is configured to support small single processor system using a few devices that the system bus .when MN/$\overline{MX}$ is low 8086 is configured to support multiprocessor system**.**
- ***Read ($\overline{RD}$):*** Is logic 0 (low) when the data is read from memory or I/O location**.**
- ***$\overline{TEST}$:*** Is an input pin and is only used by the ***wait*** instruction. If the TEST pin goes LOW (logic 0), execution will continue (WAIT instruction functions as a NOP), else if TEST pin goes HIGH (logic 1) the processor remains in an idle state**.**
- ***$\overline{READY}$:*** It indicates that the device is ready to transfer data. If the READY pin goes LOW (logic 0) the processor enters into wait state and remains in an

idle state. If the READY pin goes HIGH (logic 1) it has no effect on the operation of the processor**.**

- ✓ ***RESET:*** It is used to restart the execution. It causes the processor to immediately terminate its present activity. This signal used to reset the microprocessor, registers, seg. regs, flags**.**
- ✓ ***Clock Input (CLK):*** The clock input provides the basic timing for processor operation and bus control activity. Its frequency is different for different versions, i.e. 5MHz, 8MHz and 10MHz.
- ✓ ***Vcc:*** +5V power supply for the operation of the internal circuit**.**
- ✓ ***GND:*** Ground for the internal circuit. The 8086 microprocessor have two pins labeled GND both must be connected to ground for proper operation.
- ✓ ***Bus High Enable/Status ($\overline{BHE}$ /S7):*** The bus high enable signal goes low to indicate the transfer of data over the higher order (D15-D8). The state S7 is always logic 1**.**
- ✓ ***Interrupt Request (INTR)***: INTR is an input to the 8086 that can be used by an external device to signal that it needs to be serviced. Logic 1 at INTR represents an active interrupt request. When the MPU recognizes an interrupt request, it indicates this fact to external circuits with pulses to logic 0 at the $\overline{INTA}$ output. INTR is a maskable interrupt.
- ✓ ***NMI:*** Is the non-maskable interrupt input. The NMI is not maskable internally by software. The NMI is a hardware interrupt that cannot be ignored by the instructions of CPU. NMI used for emergency purposes like power failure.

❖ Minimum mode interface signals

Name	Function
(M/$\overline{IO}$)	Memory/IO Control
$\overline{WR}$	WRITE Control
ALE	Address Latch Enable
DT/$\overline{R}$	Data Transmit/Receive
DEN	Data Enable
HOLD	Hold request
HLDA	Hold Acknowledgment
$\overline{INTA}$	Interrupt Acknowledgment

- ✓ ***Memory/IO (M/$\overline{IO}$):*** This signal is used to distinguish between memory and I/O operation. When it is LOW, it indicates the CPU is having an I/O operation, and when it is HIGH, it indicates that the CPU is having a memory operation **.**
- ✓ ***WRITE ($\overline{WR}$):*** Indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the M/$\overline{IO}$ signal**.**
- ✓ ***Address Latch Enable (ALE) :*** A positive pulse is generated each time the processor begins any operation. This signal indicates the availability of a valid address on the address/data lines. ALE: Contains address bits A15-A0 when ALE is 1 & data bits D15 – D0 when ALE is 0.
- ✓ ***Data Transmit/Receive (DT/$\overline{R}$):*** This output is used to decide the direction of data flow through the 8286 transceiver (*is a device with bidirectional buffers, used to separate data from the address/data bus*). When (DT/$\overline{R}$ = 1) the processor sends data out (transmitting), when (DT/$\overline{R}$ = 0) the processor receiving data**.**
- ✓ ***Data Enable (DEN):*** Activate external data bus buffers (transceiver).
- ✓ ***HOLD:*** When an external device wants to take control of the system bus (Data, Address, Control), it signals to the 8086 by switching HOLD to logic 1. The hold input requests a Direct Memory Access (DMA).
- ✓ ***Hold Acknowledge (HLDA)***: The processor, after receiving the HOLD request, issues the hold acknowledge signal on HLDA pin, indicates that the 8086 has entered the hold.
- ✓ ***Interrupt Acknowledge ($\overline{INTA}$):*** This signal is used as a read strobe for interrupt acknowledge cycles. i.e. when it goes low, the processor has accepted the interrupt**.**

❖ Maximum mode interface signals

Name	Function
$\overline{RQ}$ / $\overline{GT0}$,($\overline{RQ}$ / $\overline{GT1}$)	Request/Grant bus access control
($\overline{S2}$, $\overline{S1}$, $\overline{S0}$)	Status Lines
$\overline{LOCK}$	Bus priority lock control
QS1 , QS0	Queue Status

- ✓ ***Request/Grant ($\overline{RQ}$ /$\overline{GT0}$) ,($\overline{RQ}$ /$\overline{GT1}$):*** These lines are bidirectional, and are used to both request and grant a DMA operation in maximum mode. RQ/GT0 has a *higher priority* than RQ/GT1.
- ✓ ***Status Lines ($\overline{S2}$, $\overline{S1}$, $\overline{S0}$):*** These three bit are input to the ***external bus controller device 8288***, which decodes them to identify the type of next bus cycle. The following table shows the function of these status bits in the maximum mode.

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	CPU Cycle	8288 Command
0	0	0	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O port	$\overline{IORC}$
0	1	0	Write I/O port	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Code Access	$\overline{MRDC}$
1	0	1	Read Memory	$\overline{MRDC}$
1	1	0	Write Memory	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	None

- ✓ ***$\overline{LOCK}$:*** This output pin indicates to the other processors not to ask the CPU to leave the system bus, while the $\overline{LOCK}$ signal is low. The LOCK signal is activated by *using the LOCK prefix on any instruction* and remains active until the completion of the instruction.
- ✓ ***Queue Status (QS1, QS2):*** Provide status to allow external tracking of the internal 8086 instruction queue. These pins are provided for access by the numeric coprocessor (8087 Mathco.). The following table shows the operation of the queue status bits.

QS1	QS0	Indication
0	0	No Operation (Queue is idle)
0	1	First Byte of the opcode from the queue
1	0	Empty Queue
1	1	Subsequent Byte from the Queue