

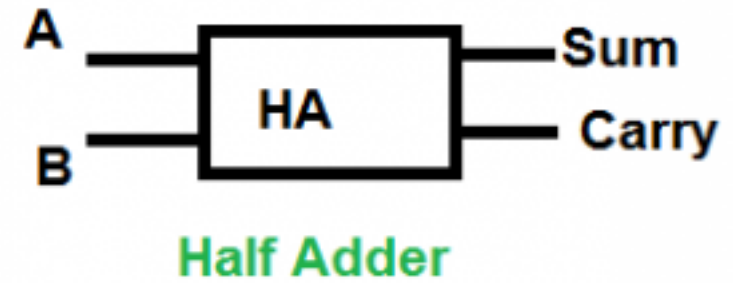
Logical Design

Lecture 14

Dr Zaid Al-Bayati

Half Adder (HA)

The addition of 2 bits is done using a combination circuit called a Half adder. The output variables are sum & carry bits. A and B are the two input bits.



A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

K-maps for the output

Here we perform two operations Sum and Carry, thus we need two K-maps one for each to derive the expression.

1) for Sum:

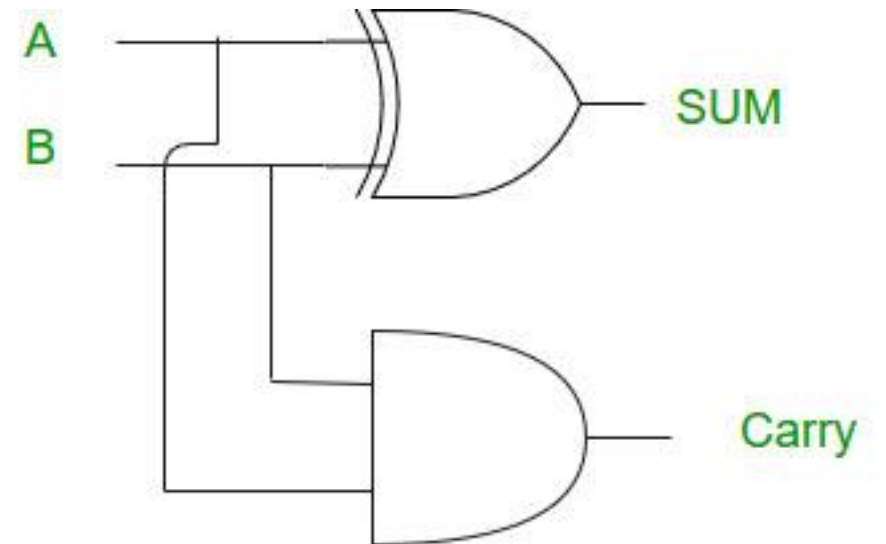
A \ B	0	1
0	0	1
1	1	0

$$\text{Sum} = A \text{ XOR } B$$

2) for Carry:

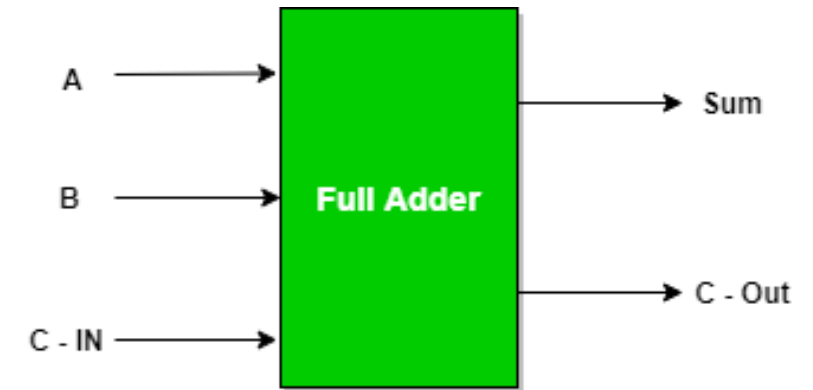
A \ B	0	1
0	0	0
1	0	1

$$\text{Carry} = A \text{ AND } B$$



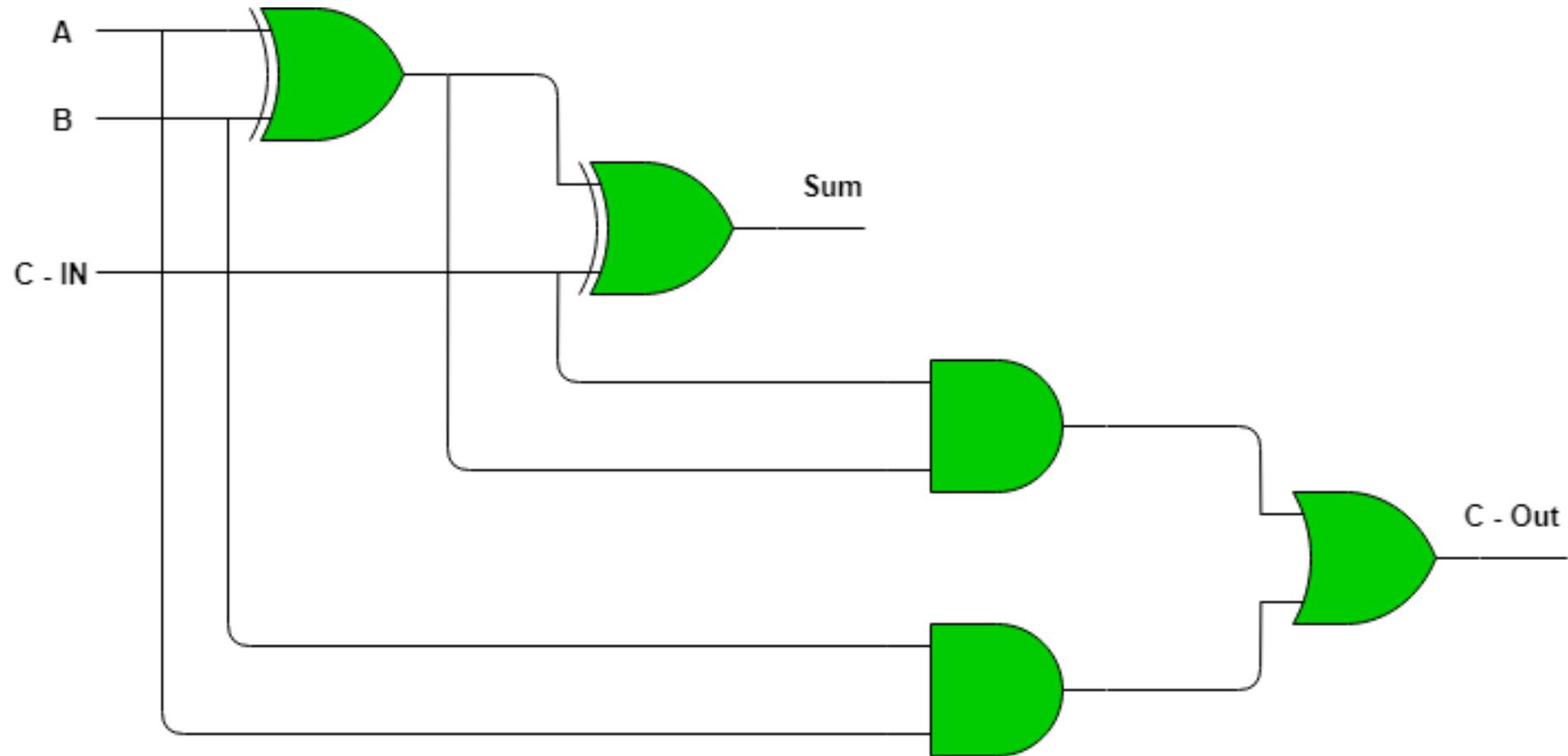
Full Adder

Full Adder is the adder which adds three inputs and produces two outputs. The first two inputs are A and B, and the third input is an input carry as C-IN. The output carry is designated as C-OUT and the normal output is designated as S which is SUM.



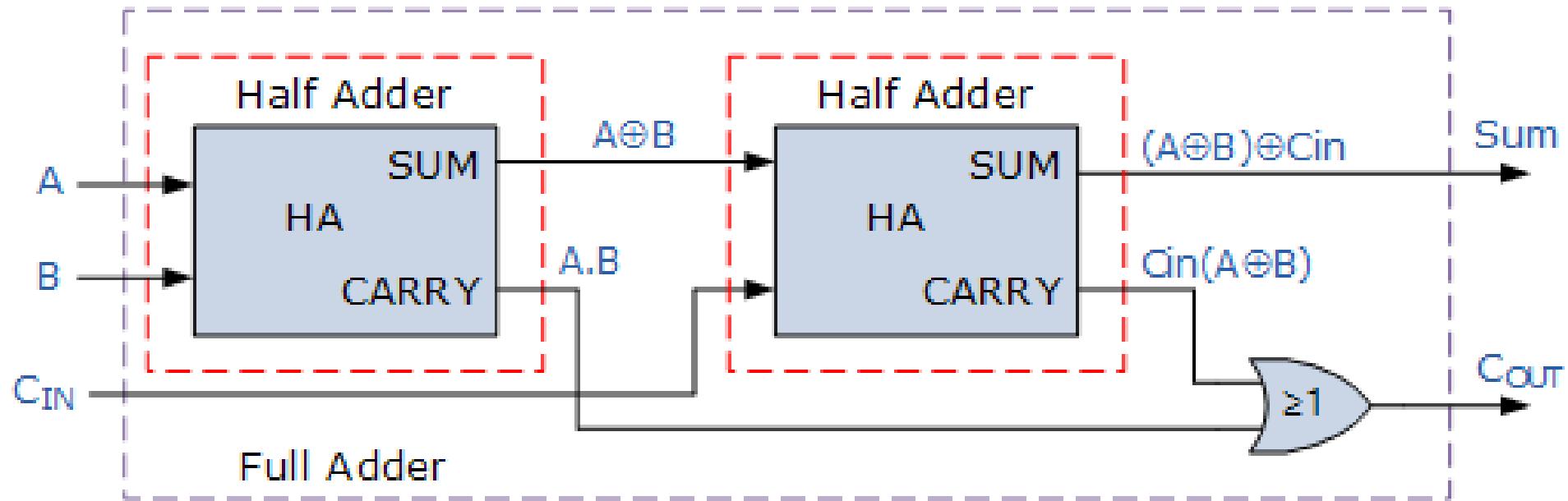
Inputs			Outputs	
A	B	C – IN	Sum	C – Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Full Adder logic circuit



Implementation of Full Adder using Half Adders

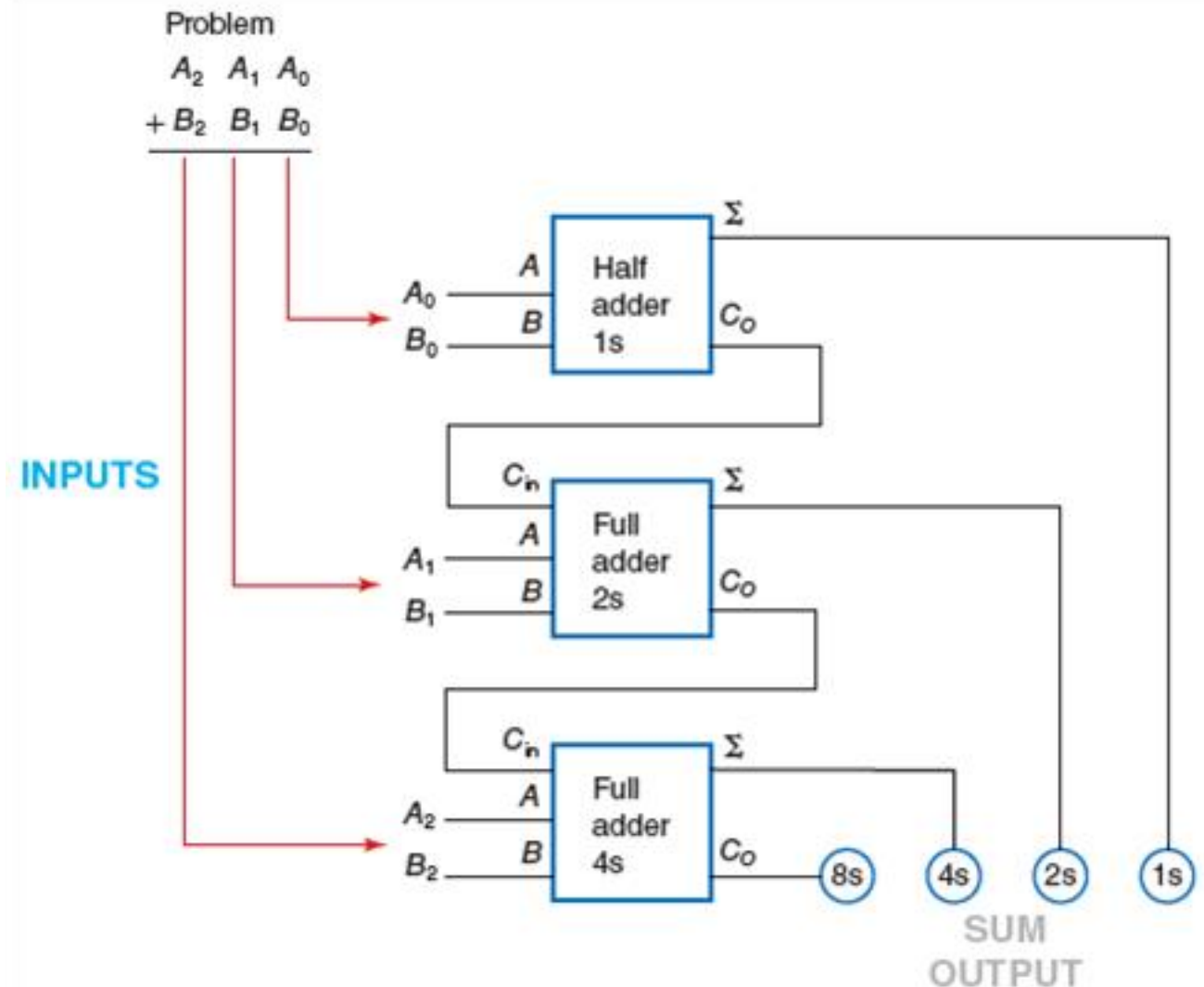
2 Half Adders and a OR gate is required to implement a Full Adder.



3 bit adder, two numbers.

A 3 bit adder is a combinational circuit that is designed to give the addition of **two** 3 bit numbers.

It can be designed using one half adder and two full adders.



Example:

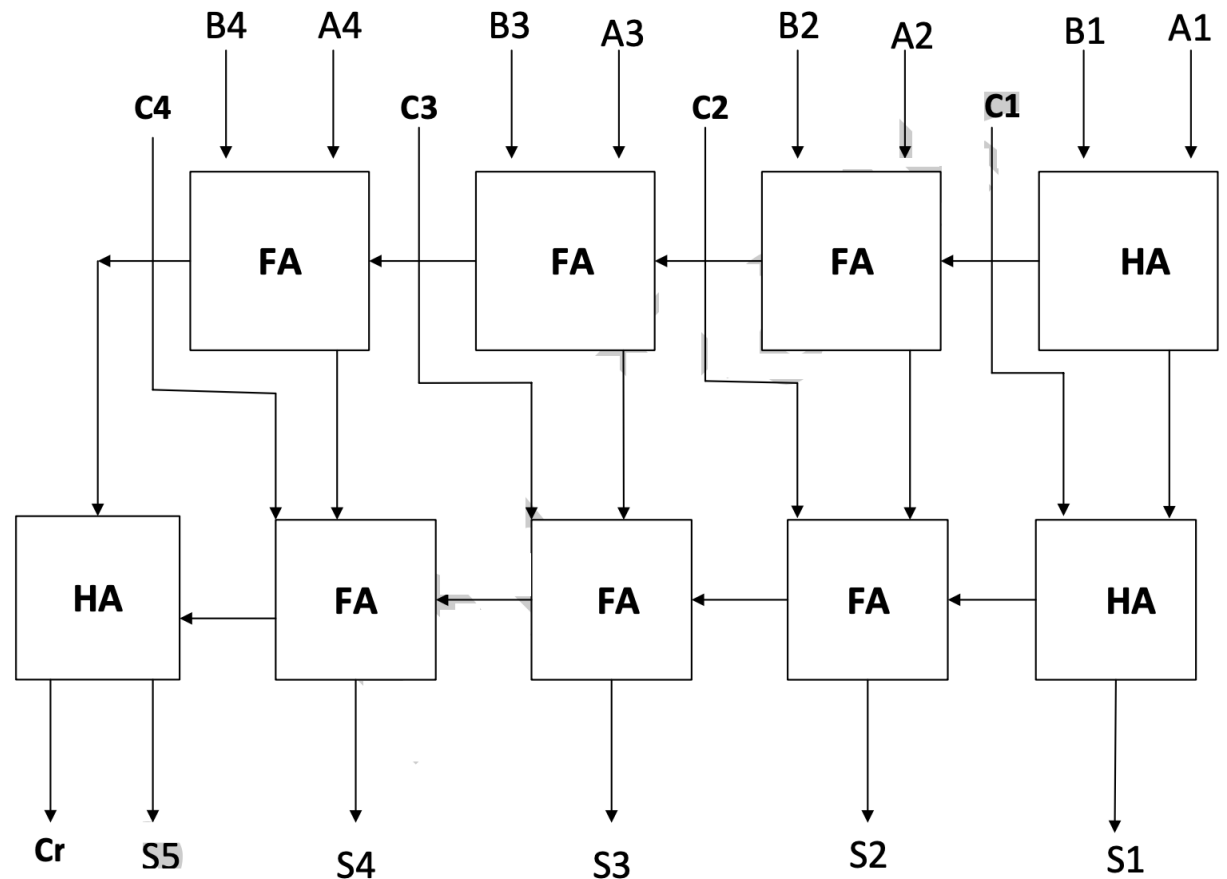
Design a logic circuit to add 4 bits 3-binary numbers.

$A \rightarrow A_4A_3A_2A_1$

$B \rightarrow B_4B_3B_2B_1$

$C \rightarrow C_4C_3C_2C_1$

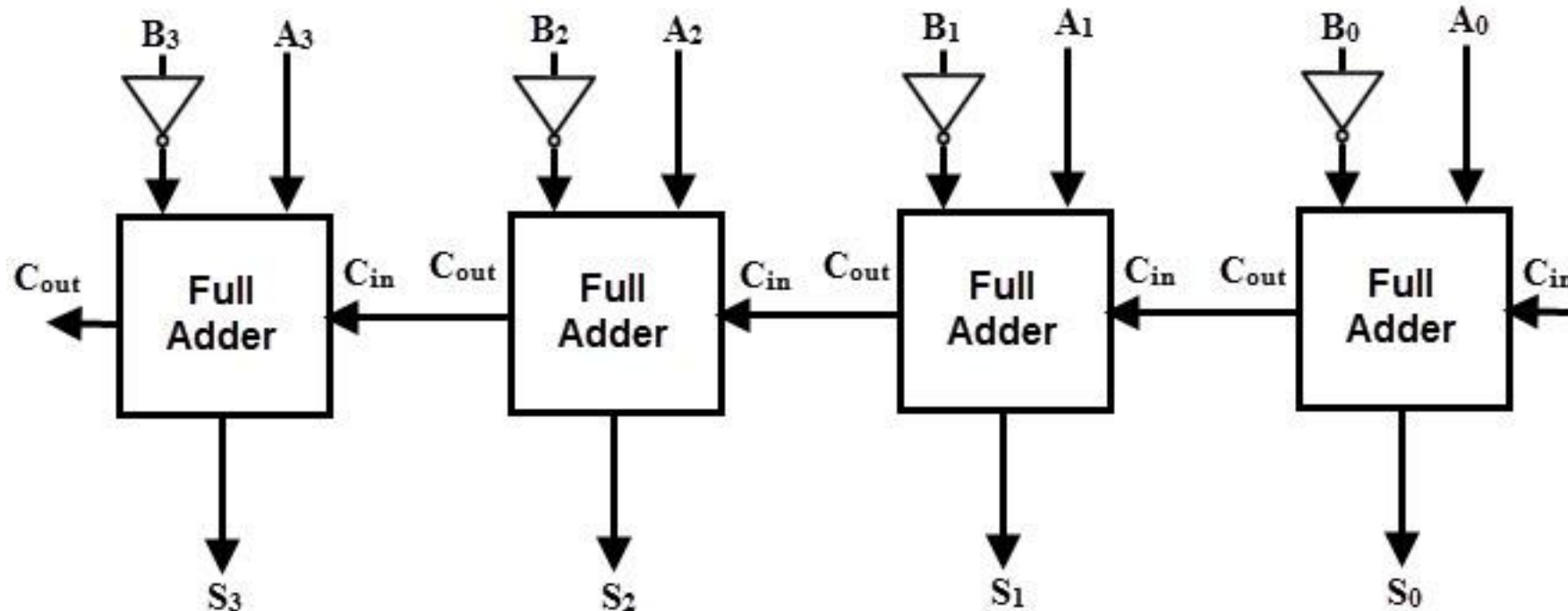
!



Design a 4-bit parallel subtractor using 4 full adders

It is also possible to design a 4 bit parallel subtractor using 4 full adders as illustrated in the diagram. The subtraction of A by B is obtained by taking 2's complement of B and adding it to A. The 2's complement of B is obtained by taking 1's complement and adding 1 to the least significant pair of bits.

Hence, in this circuit 1's complement of B is obtained with the inverters (NOT gate) and a 1 can be added to the sum through the input carry.



Half Subtractor (HS)

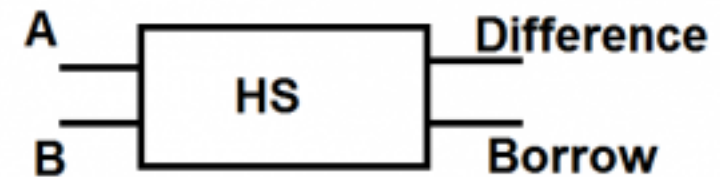
The half subtractor is a [combinational circuit](#) which is used to perform subtraction of two bits. It has two inputs A and B. And two outputs the difference and borrow_{out}.

A	B	Diff	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

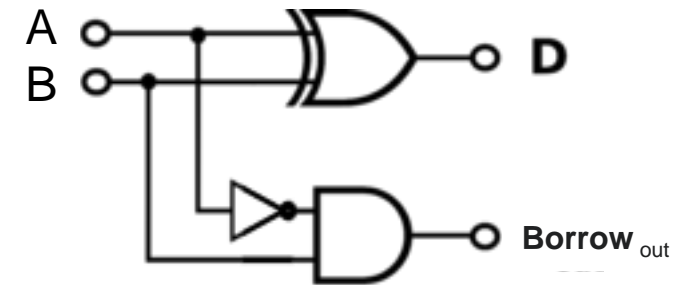
Logical Expression

Difference = $A \oplus B$

Borrow = $\bar{A}B$

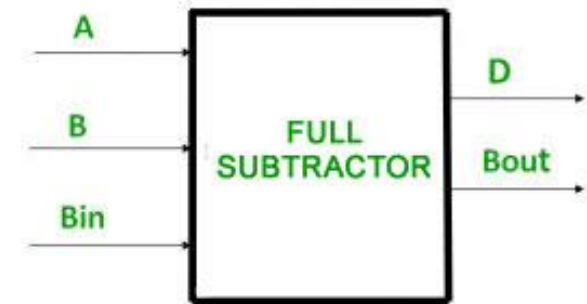


Half Subtractor



Full Subtractor (FS)

A full subtractor is a **combinational circuit** that performs subtraction of two bits, considering a borrow of the previous subtraction operation. This circuit **has three inputs and two outputs**. The three inputs A, B and Bin(previous borrow). The two outputs, D and Bout represent the difference and output borrow, respectively.



INPUT			OUTPUT	
A	B	Bin	D	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

K-Map for “difference” and “borrow”

From above table the K-Maps for “difference” and “borrow” are:

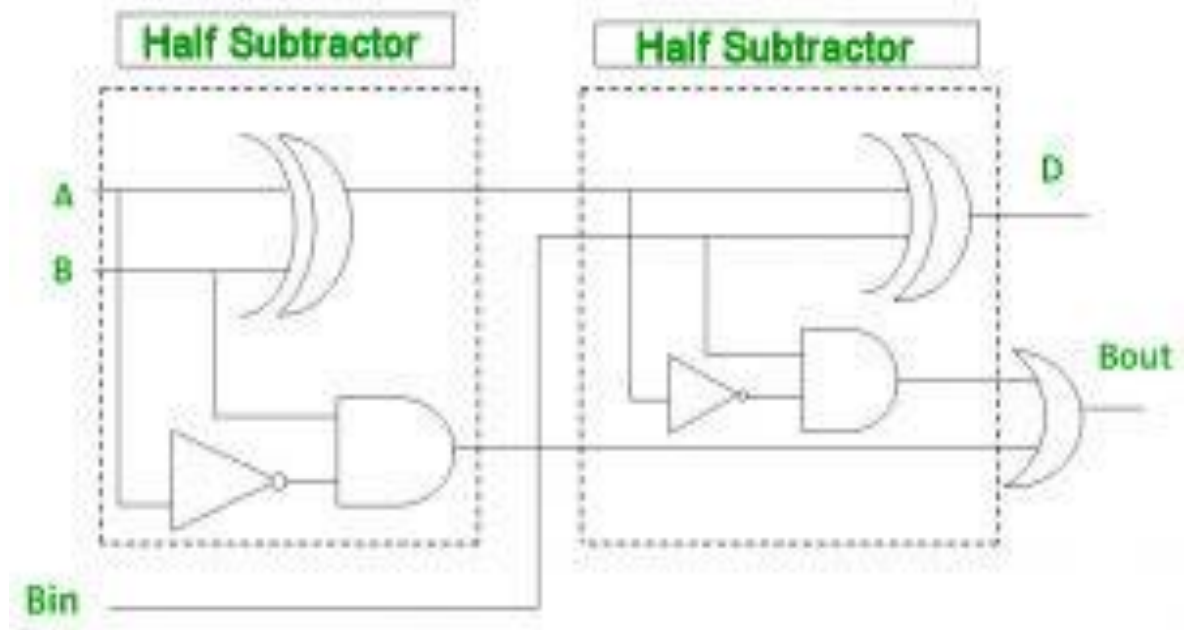
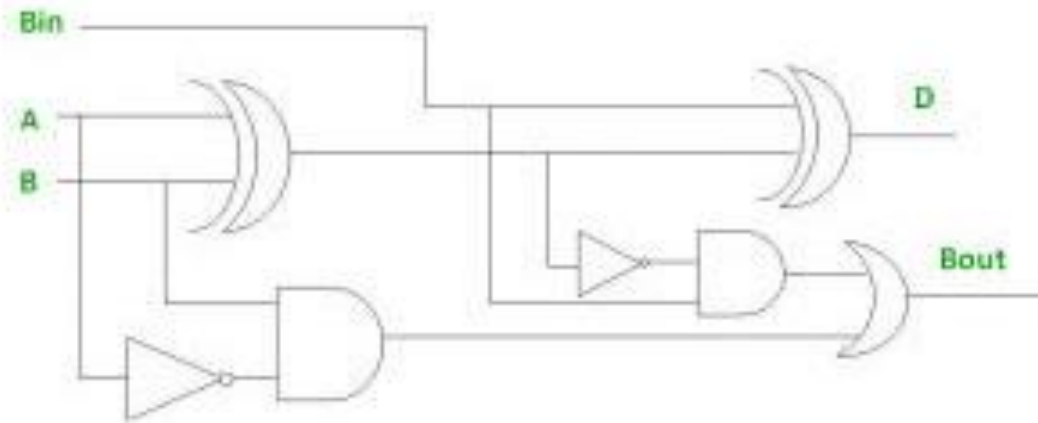
		B Bin			
		00	01	11	10
A	0	0	1	0	1
	1	1	0	1	0

$$D = A'B'Bin + AB'Bin' + A'BBin' + ABBin$$

		B Bin			
		00	01	11	10
A	0	0	1	1	1
	1	0	0	1	0

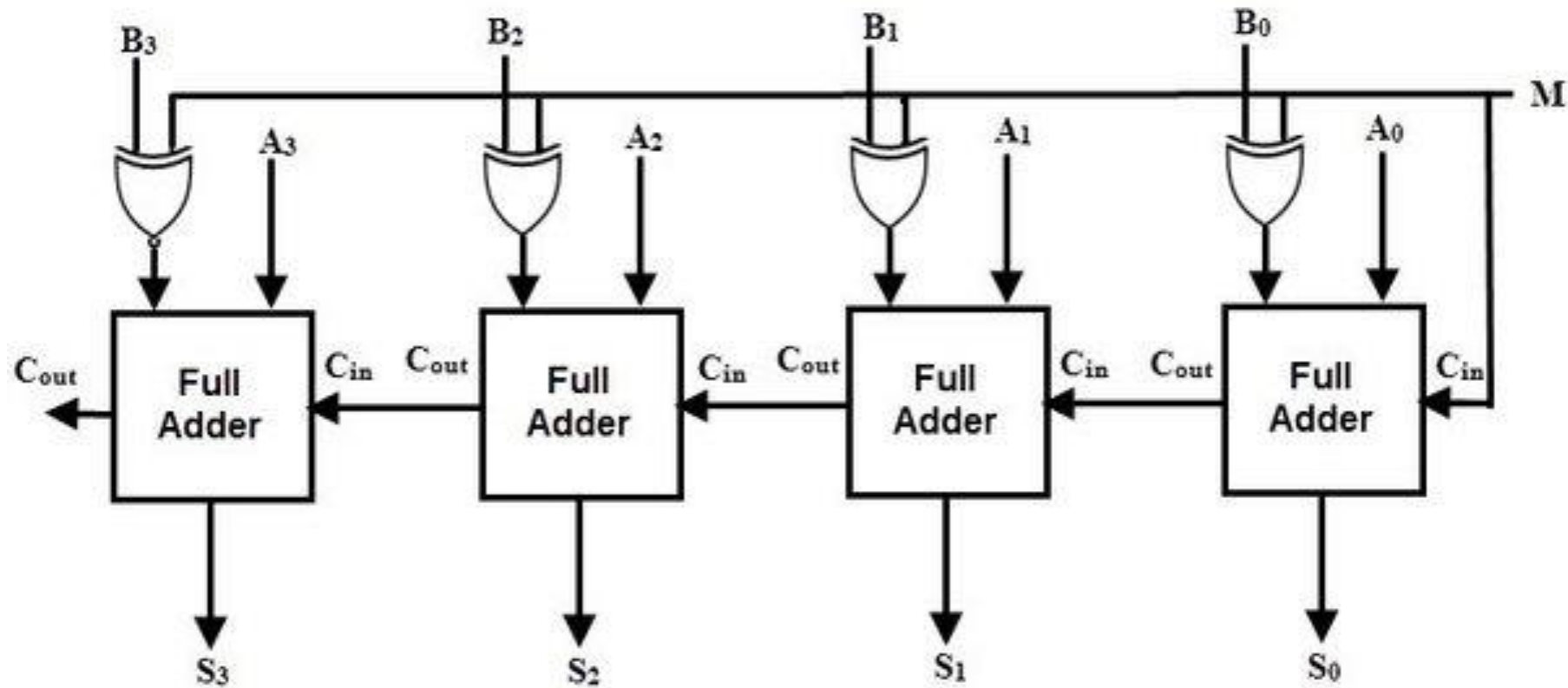
$$Bout = A'Bin + A'B + BBin$$

Full Subtractor logic circuit



Parallel Adder / Subtractor

The operations of both addition and subtraction can be performed by a one common binary adder. Such binary circuit can be designed by adding an Ex-OR gate with each full adder as shown in below figure. The figure below shows the 4 bit parallel binary adder/subtractor which has two 4 bit inputs as ' $A_3 A_2 A_1 A_0$ ' and ' $B_3 B_2 B_1 B_0$ '.



Parallel Adder / Subtractor

The **mode input control** line M is connected with carry input of the least significant bit of the full adder. This control line decides the type of operation, whether **addition** or **subtraction**.

When **M= 1**, the circuit is a **subtractor** and when **M=0**, the circuit becomes **adder**. The Ex-OR gate consists of two inputs to which one is connected to the B and other to input M. When $M = 0$, B Ex-OR of 0 produce B. Then, full adders add the B with A with carry input zero and hence an addition operation is performed.

When $M = 1$, B Ex-OR of 1 produce B complement and carry input is 1. Hence the complemented B inputs are added to A and 1 is added through the input carry, nothing but a 2's complement operation. Therefore, the subtraction operation is performed.

Design a logic circuit to add two numbers in BCD system

1. If four-bit sum is equal to or less than 9, no correction is needed.
2. If the four-bit sum is greater than 9 or if a carry is generated from the four-bit sum, the sum is invalid.
3. To correct the invalid sum, add 0110_2 to the four-bit sum. If a carry results from this addition, add it to the next higher-order BCD digit.

Inputs				Output
S_3	S_2	S_1	S_0	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Design a logic circuit to add two numbers in BCD system

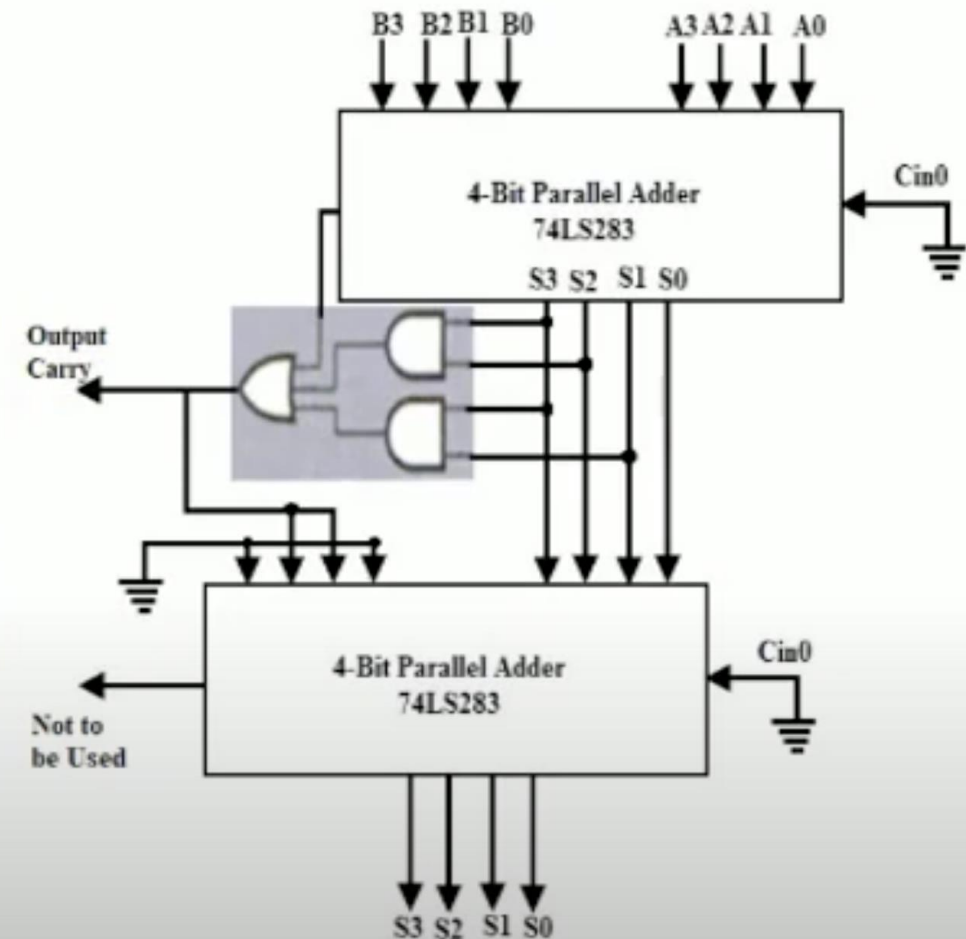
BCD Adder

K-Map for

Y

S_1S_0	$\overline{S_1}\overline{S_0}$	$\overline{S_1}S_0$	S_1S_0	$S_1\overline{S_0}$
$\overline{S_3}\overline{S_2}$	0	0	0	0
$\overline{S_3}S_2$	0	0	0	0
S_3S_2	1	1	1	1
$S_3\overline{S_2}$	0	0	1	1

$$Y = S_3S_2 + S_3S_1$$



Design a 2-Bit Binary Multiplier

A Binary Multiplier is a digital circuit used in digital electronics to multiply two binary numbers and provide the result as output.

$$\begin{array}{r} \begin{array}{cc} A1 & A0 \\ B1 & B0 \end{array} \\ \hline \begin{array}{ccc} & A1B0 & A0B0 \\ A1B1 & A0B1 & X \end{array} \\ \hline \begin{array}{ccc} A1B1+C & A0B1+A1B0 & A0B0 \end{array} \end{array}$$

Design a 2-Bit Binary Multiplier

