Logical Design Lectures

Dr. Faris Llwaah and Eman Abdulaziz

January 25, 2020

Lecture 8 – D & J-K & T Flip Flop & Counters Circuits

- **D - Flip Flop**

  The D-type flip-flop is a modification of the **Set/Reset** flip-flop by adding an inverter to prevent the S and R inputs from being at the same logic level. In fact the $D-$ Flip Flop is to a large extent of the clocked flip-flops as it ensures that inputs S and R are never equal to one logic (0 or 1) at the same time. The D-type flip flop is constructed from a gated SR flip-flop with an inverter added between the S and the R inputs to allow for a single D (Data) input as shown in the figure 1.

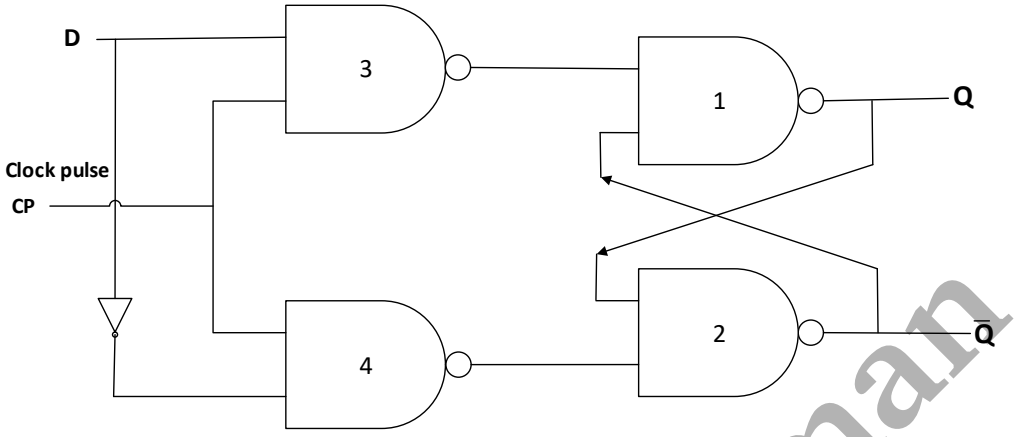

Figure 1: $D - FF$ using NAND gates

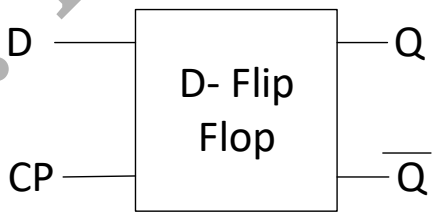

Figure 2: Block Diagram of D FF

CP	D	Q	State
0	**0**	**0**	**No change**
0	**1**	**1**	**No change**
1	**0**	**0**	**Reset**
1	**1**	**1**	**Set**

- When $CP = 0$, the output of NAND gates in First-line are logic 1, and the circuit can not change state, regardless of the value of D.
- When $CP = 1$ the state takes value as follows:

1− if $D = 1 \rightarrow$ output of gate 3 is 0 and gate 4 is 1, so the output of gate 1 is at logic 1 and $Q = 1$

2− if $D = 0 \rightarrow$ output of gate 3 is 1 and output of gate 4 is 0, with this output of gate 1 is at logic 0 and output of gate 2 is at logic 1 then $Q = 0$

- **J-K - Flip Flop**

  The JK flip flop is an improvement on the SR flip flop where $S = R = 1$ is not a problem.

- The JK is an improvement of the RS Flip flop.
- The problem of indeterminate state in RS flip flop solved in JK flip flop.
- The JK inputs behave like RS flip flop to Set or Reset.
- When both inputs of JK are equal to 1, the FF switches to complement state, that is, if $Q = 0$, it switches to $Q = 1$ and vice-versa.
- This condition can be written as $Q_{n+1} = \overline{Q_n}$, where $Q_{n+1} = next\ \ state$, $Q_n = present$ state.

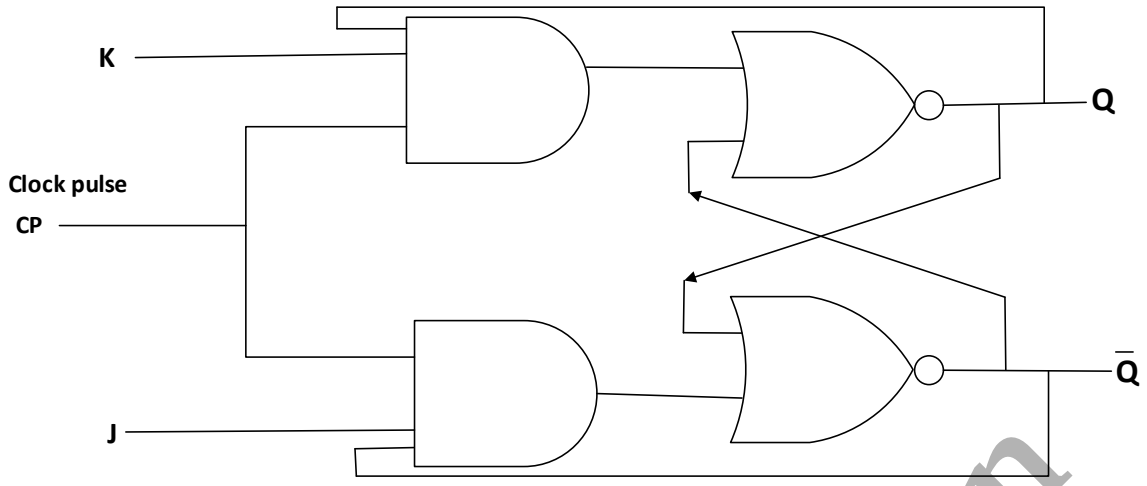

Figure 3: Clocked JK Flip Flop

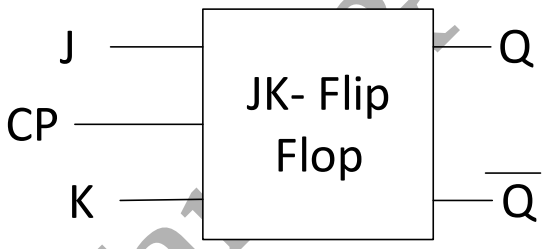

Figure 4: Block Diagram of JK Flip Flop

Qn	J	K	Qn+1	State
0	0	0	0	No change
0	0	1	0	Reset
0	1	0	1	Set
0	1	1	1	Complement Qn+1
1	0	0	1	No change
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	0	Complemen Qn+1

- When $J = K = 0$, the flip flop remains in No change state, however $Q_{n+1} = Q_n$.
- When $K = 1$, $J = 0$, the flip flop in Reset state i.e. $Q = 0$.
- When $K = 0$, $J = 1$, the flip flop in Set state i.e. $Q = 1$.
- when $J = K = 1$, the flip flop will be in Toggling state, i.e. $Q_{n+1} = \overline{Q_n}$. However for repeated CP, the output will turn ON, OFF, ON, OF and so on.
- **T - Flip Flop**

  T flip flop is obtained from the JK flip flop where J and K inputs are connected together and given to the T input. As shown in the following circuit.

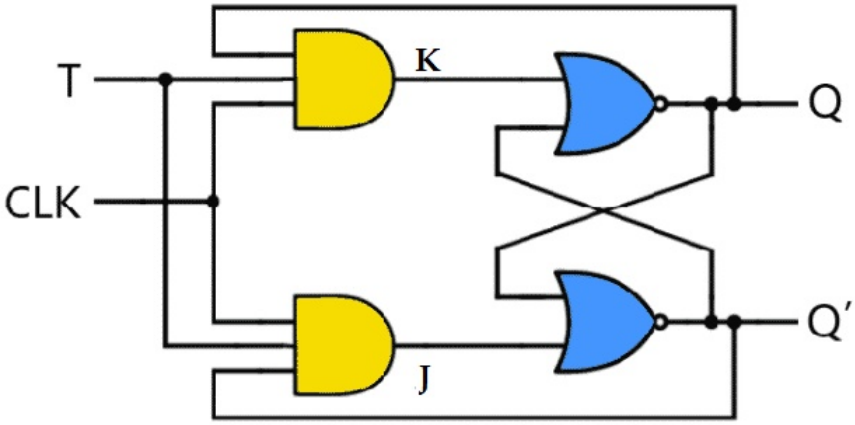

Figure 5: Logic circuit of T Flip Flop

Input	Outputs	
	Present State	Next State
T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Figure 6: Truth table of T Flip Flop

- **The applications of Flip Flop**

1− Parallel data storage. A common requirement in digital system is to take several bits of data on parallel lines and store them simultaneously in a group of flip flops.

- Each of the four parallel data lines are connected to the D input/output of a flip flop.
- The clock input/output of all flip flops are connected to a common clock i/ps, so that each FF is triggered at the same time.
- In this example a +ve edge triggered FF is used.
- Also the asynchronous i/ps are connected to a common $\overline{CLR}$ line which Reset all FFs.
- A group of FFs used for data storage are called registers.

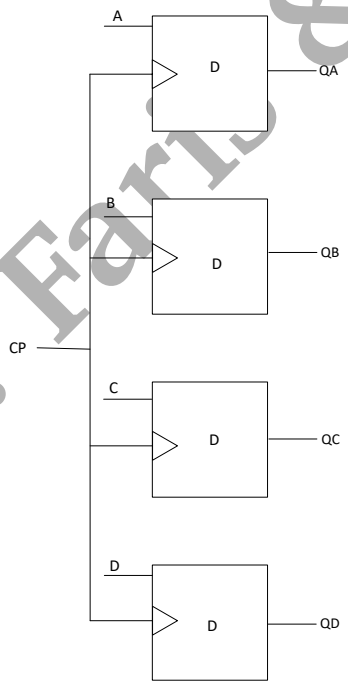

Figure 7: Parallel in Parallel out register