Microprocessor 8086/8088

8086 CPU organized as two separate processors called the Bus Interface Unit (BIU) and the Execution Unit (EU). The BIU provides hardware functions, including generation of the memory and I/O addresses for the transfer of the data between the outside of the CPU and the EU.

The EU receives program instruction code and data from the BIU, execute these instructions and store the result in the general registers. By passing the data back to the BIU, data can also be stored in a memory location or written to an output device. Note that the EU has no connection to the system buses. It receives and output all its data through the BIU.

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The only difference between an 8088 μP and 8086 μP is the BIU. In the 8088, the BIU data bus path is 8 bits wide versus the 8086's 16 bits data bus. Another difference is that the 8088 instruction queue is four bytes long instead of six.

From the previous figure we see that the main parts of the BIU are:

- *The instruction queue.*
- *A register arrays.*
- *An adder.*
- *A control unit.*

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The register array serves addressing purposes. It includes four segment registers and an instruction pointer (IP). All of which are 16 bit long. This particular adder is used only for address calculations. It does not passes the full arithmetic /logic capabilities of the main ALU of the EU. Three temporary registers shown with the adder hold either address components (prior to an address calculation) or the result. Notice that each unit of the 8088/8086 has its own independent control section. The control section of the BIU is responsible for all data transfers over the external CPU bus. Incoming data flow via the internal bus of the BIU to the instruction queue or its register address. Addresses flow from the temporary register, at the output of the adder to the external CPU bus via a 20 bit address bus.

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The main parts of the EU are:

- *The array of general registers.*
- *The main ALU.*
- *A flag register.*
- *A control section.*

There are again three temporary registers holding operands during data manipulation by the ALU. Employed in most CPUs, such registers are generally inaccessible and transparent to programmer. Note that all registers of the EU connect to a common 16 bit wide bus for data exchanges, results from the ALU flow to registers through this bus as well. The control section of the EU is more complex than that of the BIU. Some of the control lines of the external bus as, for example, bus control and interrupt lines, are handled by the control section of the EU. However, all data transfer are via the BIU. Opcode flows from the instruction queue into the instruction register (IR) for decoding

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Operands flow to appropriate registers via the ALU data bus. Notice also a 16 bit bi-directional data path between the BIU register array and the ALU data bus. Address components for final address calculation at the BIU as well as data destined for the external bus flow from the EU via this path.

Memory Segmentation:

When the EU of the 8088/8086 decodes an instruction, it determines (among the other things) the applicable addressing modes. Then it manipulates each operand field according to derive a 16 bit address. Since internal paths are 16 bit wide, the EU is generally limited to handling quantities up to 16 bits long. A 16 bit address allows unique identification of 64 Kilo byte (2^{16}) byte location. But since the 8088/8086 has a 1 Mega byte address space, the 16 bits address must be argumented somehow to 20 bits to make possible unique identification of 1 million byte locations (1,024,576).

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Here is exactly where the role of the BIU comes into play (in address calculation). The BIU takes the 16 bit address derived by the EU and adds it to the contents of a register. This register can be any one of the four so-called "segment registers". Before the addition, the contents of the segment register are shifted four positions in the direction of the MSB. That is, to the left. Thus, the adder procedures a 20 bit quantity as in the figure. This quantity is used for identification of physical memory locations and is therefore called "physical address". Addresses presented over the external bus are always physical addresses. However, the address component it contributes is named a "segment address" rather than a base address. On the other hand, the address provided by the EU is treated as a displacement (or offset) what is the lowest physical address within the segment. Clearly, this corresponds to an all-zero offset and this coincides with the segment address (SA) itself.

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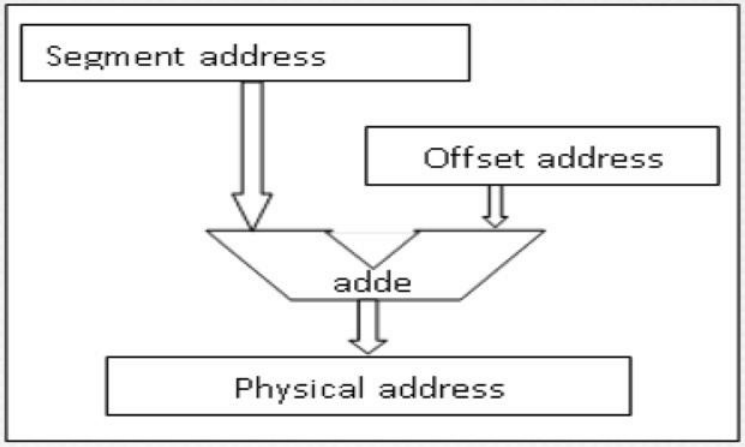

Note that due to the 4 bit shift, segment addresses are always multiplies by 16. The highest possible physical address within the segment correspond to the maximum possible value of the offset that is SA + 64K. Since the 8088/8086 has four segment register it can address up to a total of 4 * 64K = 256KB at any given time. By loading different segment addresses in the segment registers, any location in the 1MB address space may be accessed.