Computer Organization

SYSTEM BUS

The CPU , memory and I/O are normally connected by three groups of connections, each called a **bus**: ***data bus, address bus and control bus.***

1. **Data Bus**: These are lines used by the information that is being moved.

When communicating with memory this information may either instruction or data.

In I/O devices this information may be data, device status or commands or interrupt information.

- ❑ Data can be transferred in both directions on the data bus (bidirectional).
- ❑ Internal data bus: within the CPU itself.
- ❑ External data bus: Between CPU and other components (as RAM, I/O devices,etc.).
- ❑ The number of data lines in a bus determines the number of bits that can be transferred simultaneously.
- ❑ A microcomputer with n data lines is normally called an n-bit microcomputer.

ex: 8-bits microcomputer can transfer one byte in each bus cycle.

16-bits microcomputer can transfer 2 byte (word) in each bus cycle. (8086 mp).

SYSTEM BUS

EX1: How many bus cycle need to transfer data of size 64bits , if data bus size 16 line?

sol:

$$no\ of\ cycle = \frac{no.\ of\ bits\ (data)}{\text{no. of lines in dada bus}} = \frac{64}{16} = 4 \text{ bus cycle}$$

EX2: How many bus cycle need to transfer 128 byte of data in 32-bits microcomputer ?

$$\because \text{data bus size} = 32\,\text{bits} = 4\,\text{byte can be transfer in each cycle}$$

$$no\ of\ cycle = \frac{size\ \text{of data}}{\text{size of data bus}} = \frac{128\,byte}{4\,\text{byte}} = 32\,\text{bus cycle}$$

2. Address Bus:

❑ unidirectional group of wires which carries address information bits form processor to peripherals

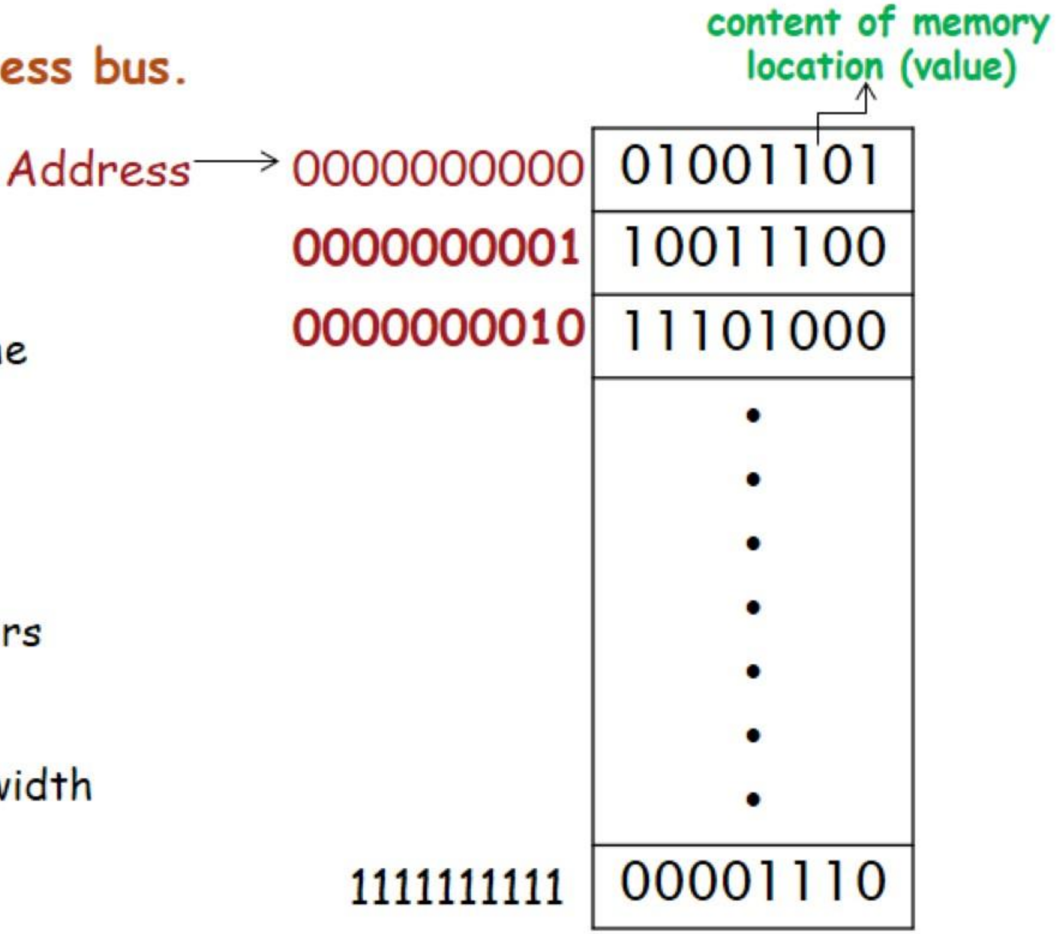
❑ Each memory locations or interface register has associated with it a unique bit combination called an address.

❑ The number of bits used to specify an address clearly determines the set of all possible addresses.

❑ Memory address is put on address bus.

Memory

- Ordered sequence of bytes
  - □ The sequence number is called the **memory address**
- Byte addressable memory
  - □ Each byte has a unique address
  - □ Supported by almost all processors
- Physical address space
  - □ Determined by the address bus width



content of memory location (value)

Address →

0000000000	01001101
0000000001	10011100
0000000010	11101000
	• • • • • • •
1111111111	00001110

The size of address bus determine :

Let n = the number of lines in address bus

1. The size of memory connected with processor (capcity).

$$\text{size of memory} = 2^n$$

2. Size of memory address (physical address).

$$\text{size of memory address} = n$$

3. The address space of main memory (set of all possible addresses).

$$\text{address space} = 0 \rightarrow \lfloor 2^n - 1 \rfloor \qquad \text{(in decimal)}$$

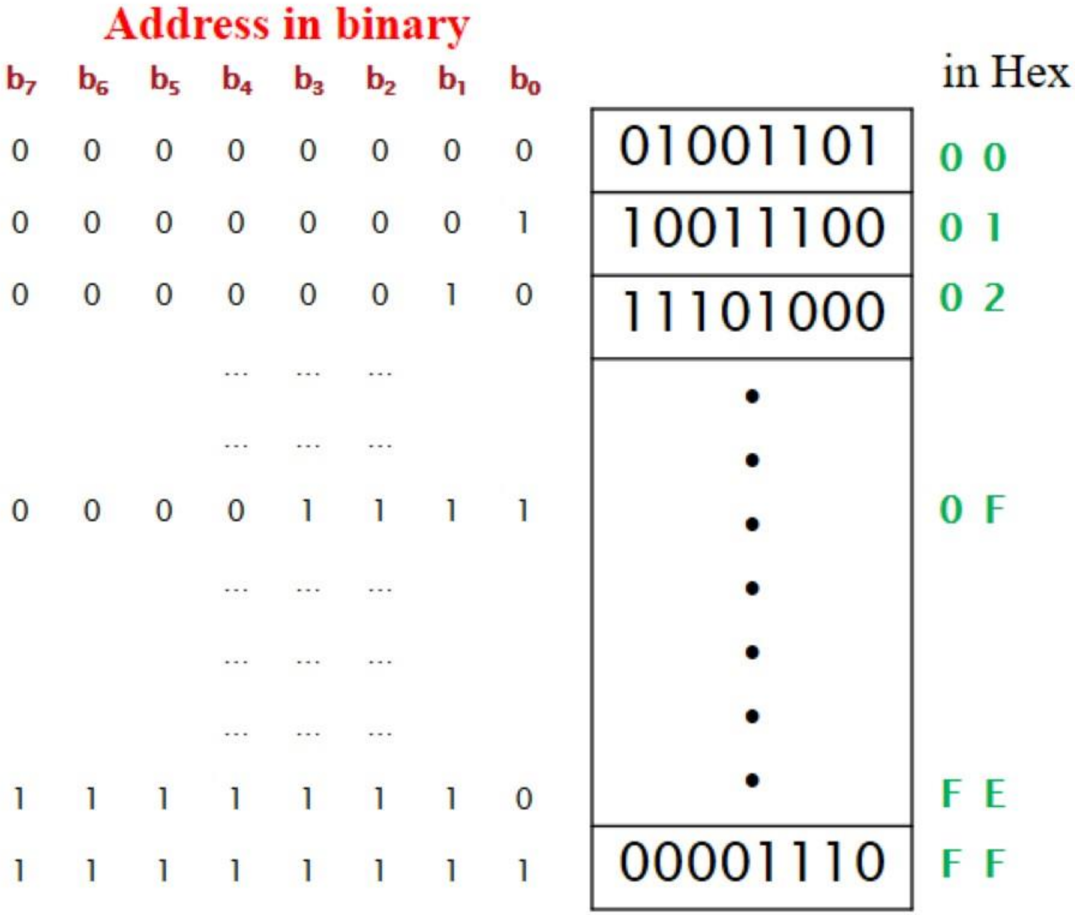
EX: Processor has a 8 lines address bus

Size of memory = 2^n = 2^8 = 256 byte

Size of address for each memory location = 8 bits

Address space (decimal) = 0 ⟶ 2^8-1 = 0 ⟶ 255 different memory location

Address space in hexadecimal



Address in binary									in Hex
b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0		
0	0	0	0	0	0	0	0	01001101	0 0
0	0	0	0	0	0	0	1	10011100	0 1
0	0	0	0	0	0	1	0	11101000	0 2
			...	...	...			•	
			...	...	...			•	
0	0	0	0	1	1	1	1	•	0 F
			...	...	...			•	
			...	...	...			•	
			...	...	...			•	
1	1	1	1	1	1	1	0	•	F E
1	1	1	1	1	1	1	1	00001110	F F

Address Space is the set of memory locations (bytes) that can be addressed 00 -- FF

EX: Processor has a 16 lines address bus

Size of memory = $2^n = 2^{16}$ = 64 K.Byte

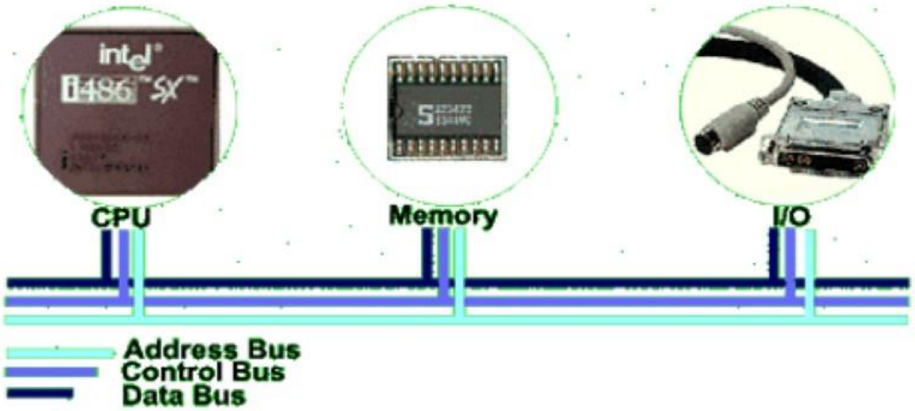
Size of address for each memory location = 16 bits

Address space (decimal) = $0 \longrightarrow 2^{16}-1 = 0 \longrightarrow 65536$ different memory location

Address space in hexadecimal 0000 -- FFFF

b15	b14	B13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0		in Hex
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	01001101	0000
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	10011100	0001
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	11101000	0002
	...	...	...	...		...	...	...			...	...	...			• • •	
	...	...	...			...	...	...			...	...	...				
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	00001110	000F
				...	...	...	...	...	...		...	...	...			• • •	
				...	...	...	...	...	...		...	...	...				
0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0		00FF
	...	...	...	...		...	...	...			...	...	...				
	...	...	...			...	...	...			...	...	...				
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		FFFF

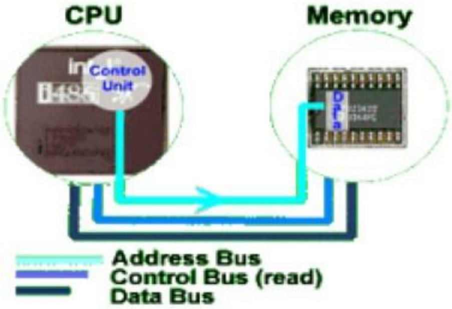
Control Bus: Regardless of the bus arrangement being used, a certain amount of control information must be passed back and forth among the CPU, the memory modules, and the device interfaces.



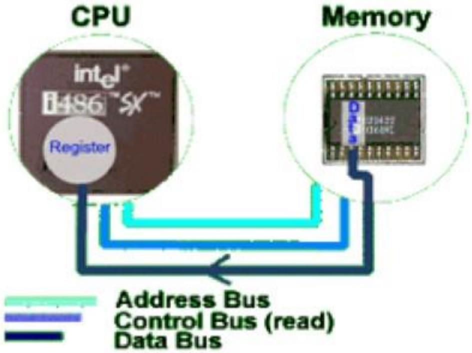
Fetch and Execute

The following pages illustrate the operations performed within a computer during a fetch and execute cycle.

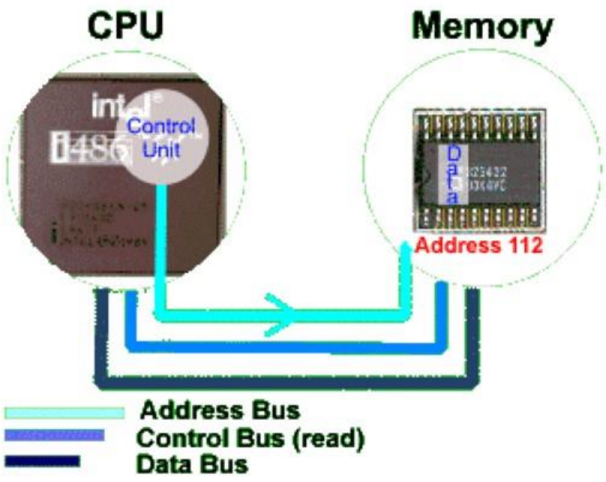
The control bus performs a read operation:

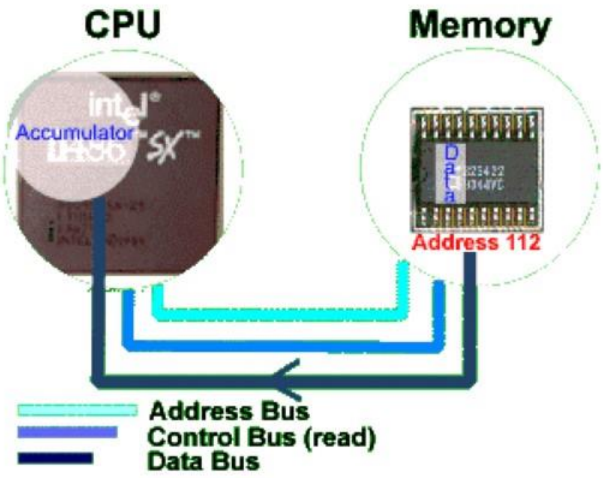


The control unit in the CPU prompts memory to put the instruction onto the data bus enabling the CPU to read the instruction onto its instruction decoder which is part of the control unit:



The next step involves the CPU decoding the instruction. This instruction is then executed. For example, if the instruction is for the Control Unit to load the contents of the memory location 112 into the accumulator:

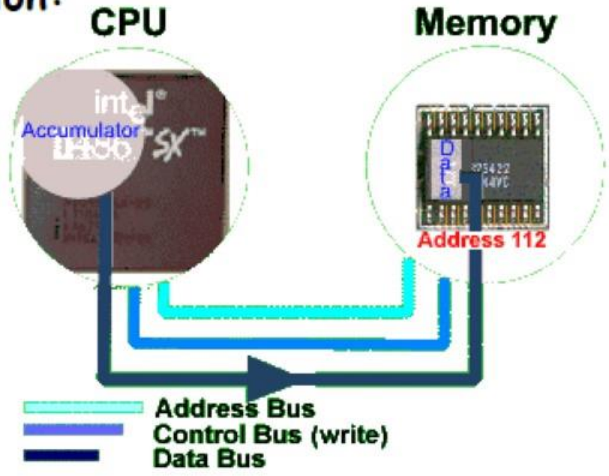




Performing a write operation

The control unit sets the address bus to location 112 and puts the value of the accumulator onto the data bus.

Finally the control bus performs a memory write operation:


CPU
Memory
intel
Accumulator
SX
Data
Address 112
Address Bus
Control Bus (write)
Data Bus