Example 5–4 (continued)

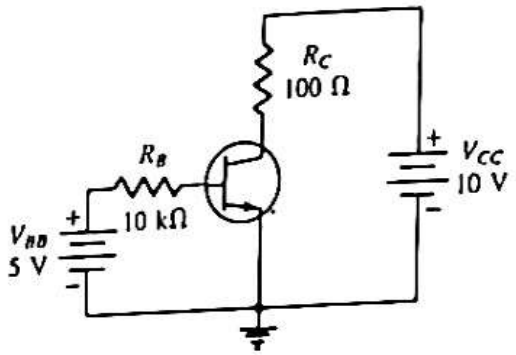


FIGURE 5–12

Solution:

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{5\text{ V} - 0.7\text{ V}}{10\text{ k}\Omega} = 430\ \mu\text{A}$$

$$I_C = \beta_{dc} I_B = (150)(430\ \mu\text{A}) = 64.5\text{ mA}$$

$$\alpha_{dc} = \frac{\beta_{dc}}{\beta_{dc} + 1} = \frac{150}{151} = 0.993$$

$$I_E = \frac{I_C}{\alpha_{dc}} = \frac{64.5\text{ mA}}{0.993} = 64.95\text{ mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 10\text{ V} - (64.5\text{ mA})(100\ \Omega)$$
$$= 10\text{ V} - 6.45\text{ V} = 3.55\text{ V}$$

$$V_{CB} = V_{CE} - V_{BE} = 3.55\text{ V} - 0.7\text{ V} = 2.85\text{ V}$$

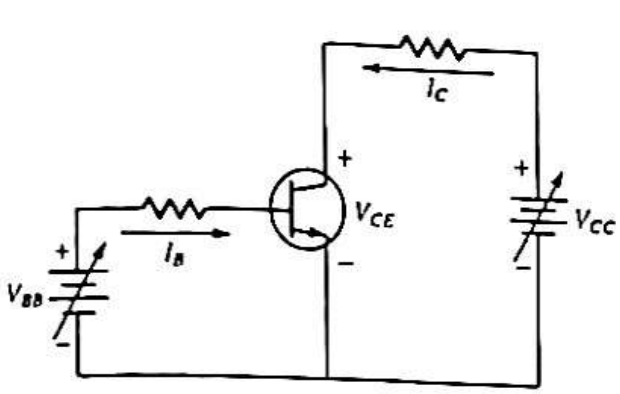
Since the collector is at a higher voltage than the base, the collector-base junction is reverse-biased.

Collector Curves

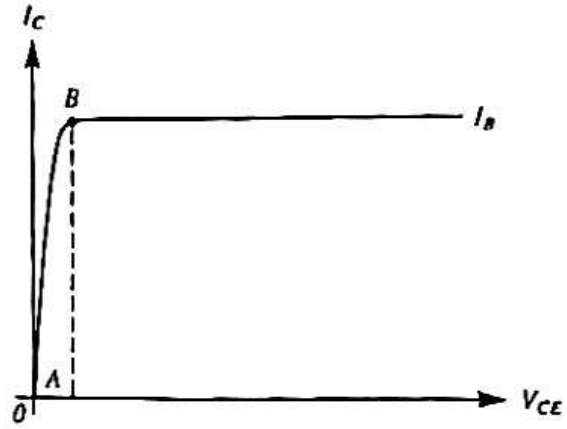
With a circuit like Figure 5–13A, a set of curves can be generated showing how I_C varies with V_{CE} for various values of I_B. These are the *collector characteristic* curves.

Notice that both V_{BB} and V_{CC} are adjustable. If V_{BB} is set to produce a specific value of I_B and V_{CC} is zero, then $I_C = 0$ and $V_{CE} = 0$. Now, as V_{CC} is gradually increased, V_{CE} will increase and so will I_C. This is indicated on the portion of the curve between points A and B in Figure 5–13B.

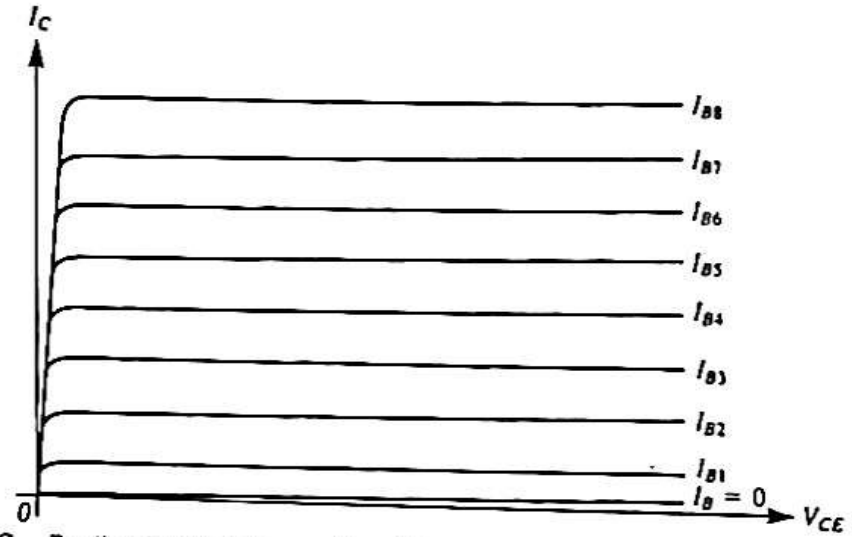
When V_{CE} reaches approximately 0.7 V, the base-collector junction becomes reverse-biased and I_C reaches its full value determined by the relationship $I_C =$



A. Circuit



B. I_C curve for one value of I_B with V_{CE} changing



C. Family of collector curves ($I_{B1} < I_{B2} < I_{B3}$, etc.)

FIGURE 5–13 *Collector characteristic curves.*

$\beta_{dc}I_B$. At this point the I_C levels off to an almost constant value as V_{CE} continues to increase. This action appears to the right of point B on the curve. Actually, I_C increases slightly as V_{CE} increases due to widening of the base-collector depletion layer which results in fewer holes for recombination in the base region.

By using other values of I_B, additional I_C–versus-V_{CE} curves can be produced, as shown in Figure 5–13C. These curves constitute a *family* of collector curves for a given transistor.

Example 5–5

Sketch the family of collector curves for the circuit in Figure 5–14 for I_B = 5 μA to 25 μA in 5 μA increments. Assume β_{dc} = 100.

Example 5–5 (continued)

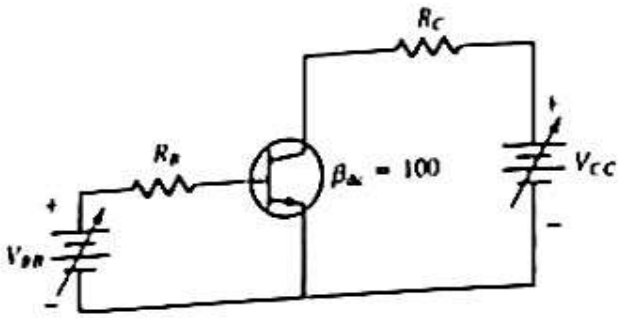


FIGURE 5–14

Solution:

Using the relationship $I_C = \beta_{dc} I_B$, values of I_C are calculated and tabulated in Table 5–1. The resulting curves are plotted in Figure 5–15.

TABLE 5–1

I_B	I_C
5 μA	0 5 mA
10 μA	1.0 mA
15 μA	1.5 mA
20 μA	2.0 mA
25 μA	2.5 mA

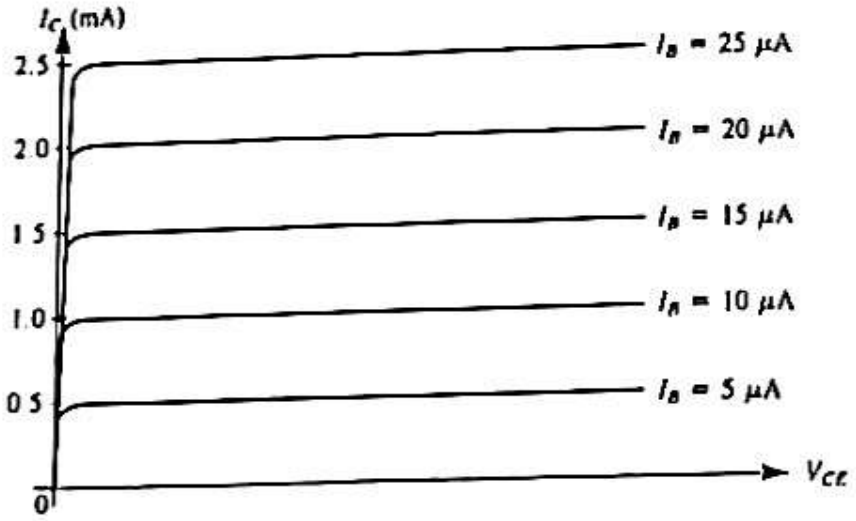


FIGURE 5–15

Cutoff and Saturation

When $I_B = 0$, the transistor is *cutoff*. This is shown in Figure 5–16 with the base lead open to produce a base current of 0. Under this condition, there is a very

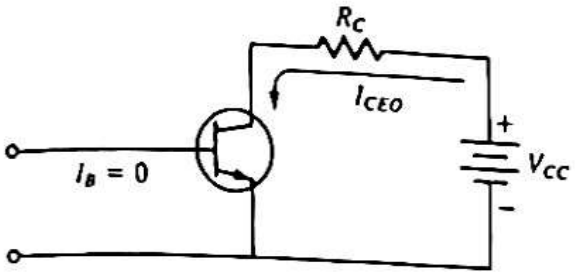


FIGURE 5–16 *Collector leakage current in cutoff.*

small amount of collector leakage current, I_{CEO}, due mainly to thermally produced carriers. In cutoff, both the base-emitter and the base-collector junctions are *reverse*-biased.

Now let's consider the condition known as *saturation*. When the base current in Figure 5–17A is increased, the collector current also increases and V_{CE} decreases as a result of more drop across R_C.

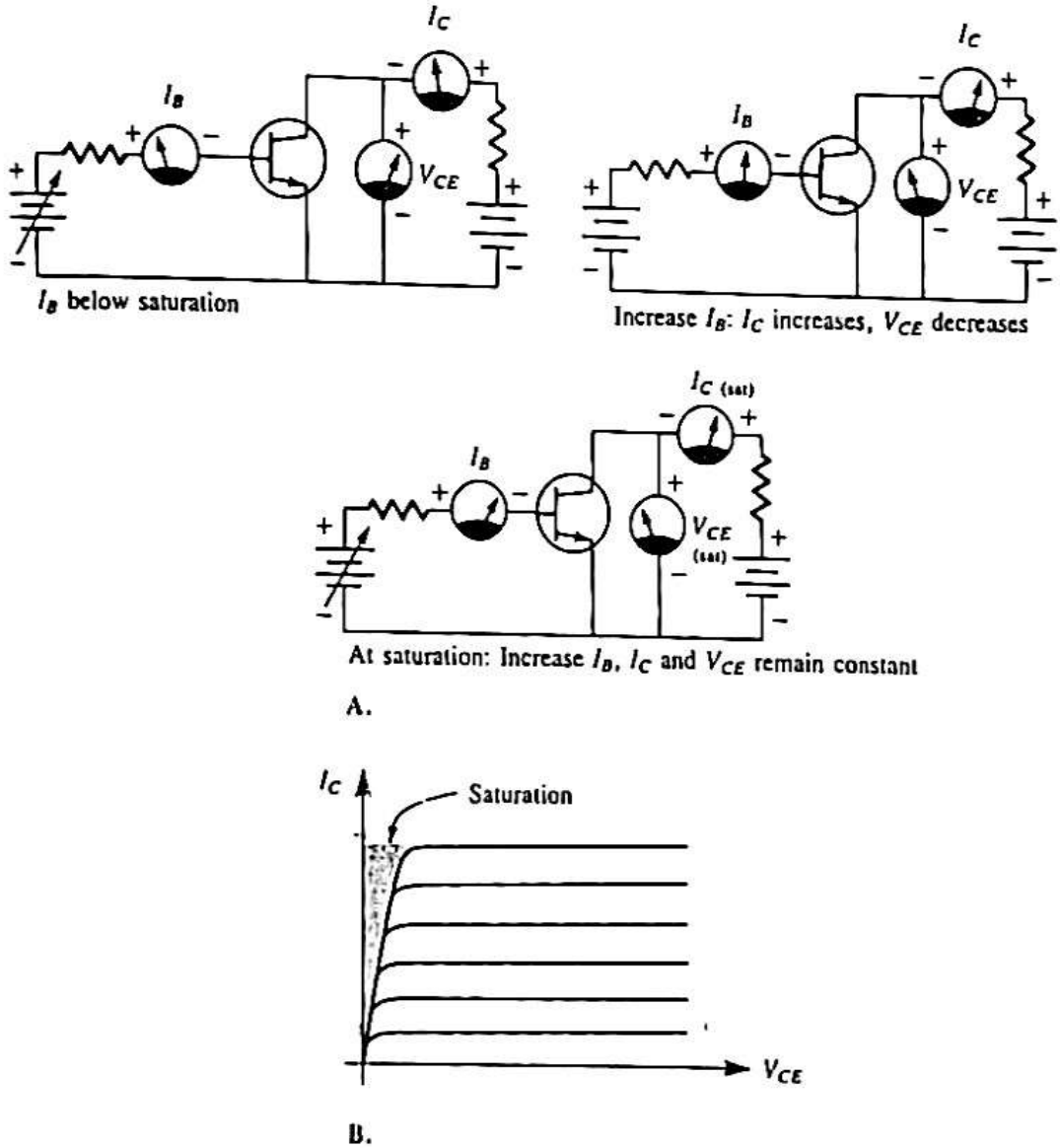


FIGURE 5–17 *Saturation.*

When V_{CE} reaches a value called $V_{CE(sat)}$, the base-collector junction becomes *forward*-biased and I_C can increase no further even with a continued increase in I_B. At the point of saturation, the relation $I_C = \beta_{dc} I_B$ is no longer valid.

$V_{CE(sat)}$ for a transistor occurs somewhere below the knee of the collector curves, as shown in Figure 5–17B, and is usually only a few tenths of a volt for silicon transistors.

Example 5–6

Determine whether or not the transistor in Figure 5–18 is in saturation. Assume $V_{CE(sat)}$ is small enough to neglect. $\beta = 50$

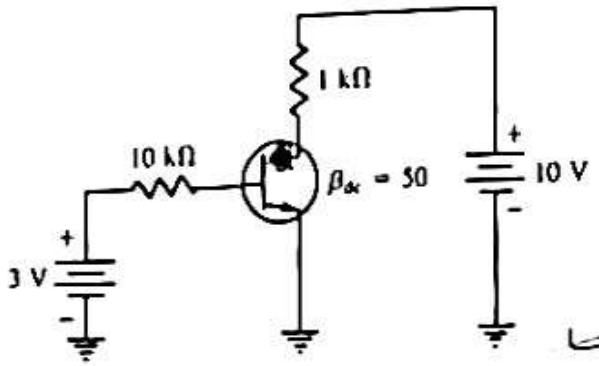


FIGURE 5–18

Solution:

First, determine $I_{C(sat)}$.

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{10\text{ V}}{1\text{ k}\Omega} = 10\text{ mA}$$

Now, let's see if I_B is large enough to produce $I_{C(sat)}$.

$$I_B = \frac{V_{BB} - 0.7\text{ V}}{R_B} = \frac{2.3\text{ V}}{10\text{ k}\Omega} = 0.23\text{ mA}$$

$$I_C = \beta_{dc} I_B = (50)(0.23\text{ mA}) = 11.5\text{ mA}$$

This shows that with the specified β_{dc}, this base current is capable of producing an I_C greater than $I_{C(sat)}$. Therefore, *the transistor is saturated*, and the collector current value of 11.5 mA is never reached.

Review for 5–5

1. $I_B = 8\ \mu\text{A}$ and $I_C = 640\ \mu\text{A}$. Determine β_{dc}.
2. If $\alpha_{dc} = 0.972$, what is β_{dc}?
3. A transistor connected in a common-emitter configuration has an $R_B = 20\text{ k}\Omega$. If $V_{BB} = 8$ V, what is I_B?

5–6 COMMON-COLLECTOR (CC) CONFIGURATION

When a transistor is connected with the *collector* as the common (grounded) terminal, it is a *common-collector* connection, often called an *emitter-follower*. Notice that the collector is *not* at dc ground, but it *is* at ac ground because the V_{CC} source has 0 resistance (ideally) to an ac signal. This is shown for both npn and pnp transistors in Figure 5–19.

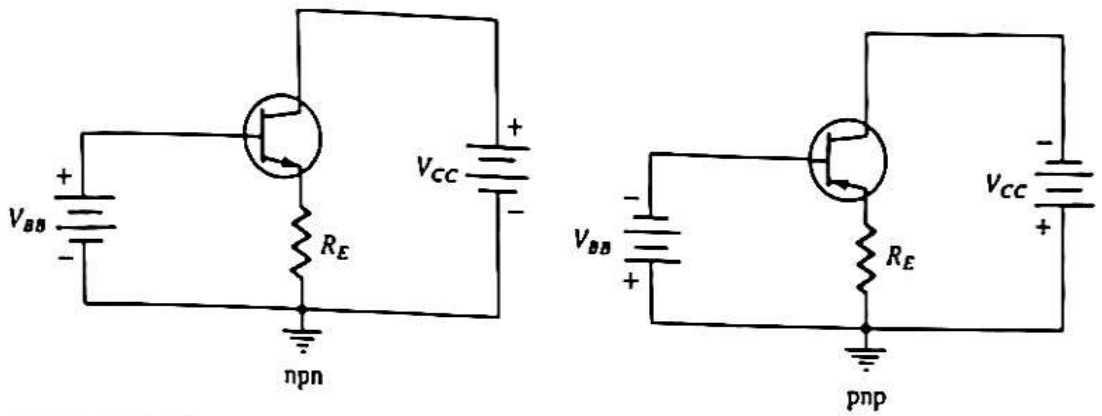


FIGURE 5–19 *Common-collector configuration.*

Again, the *basic* transistor operation is the same as with the other two configurations. V_{BB} forward-biases the base-emitter junction, and V_{CC} reverse-biases the base-collector junction. Notice, in this circuit, that V_{CC} is connected directly to the collector, and an external resistor, R_E, is connected from the emitter to ground. The output voltage is taken at the emitter with respect to ground (across R_E), whereas in the common-emitter circuit the output is taken at the collector with respect to ground.

Current Gain

I_E is the output current, and I_B is the input current. So, the current gain is I_E/I_B. If we assume $I_E \cong I_C$, the current gain is approximately β_{dc} as in the common-emitter configuration.

dc Analysis

The currents and voltages in Figure 5–20 depend on the transistor characteristics and the external circuit values.

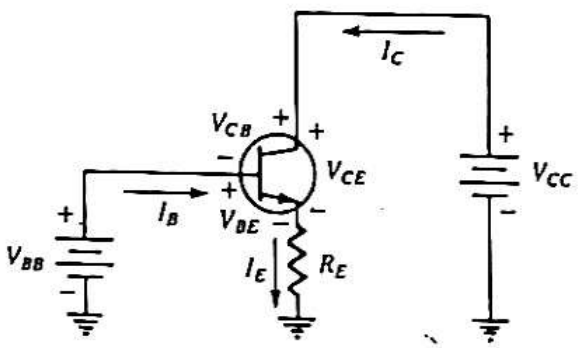


FIGURE 5–20 *Common-collector currents and voltages.*

The voltage at the base is V_{BB}. The emitter is $V_{BB} - V_{BE}$ where $V_{BE} \approx 0.7$ V for silicon. From this we can get expressions for emitter current.

$$I_E = \frac{V_E}{R_E}$$

$$I_E = \frac{V_{BB} - V_{BE}}{R_E} \tag{5–13}$$

Assuming $I_C \cong I_E$

$$I_B \cong \frac{I_E}{\beta_{dc}} \tag{5–14}$$

The collector-to-emitter voltage is

$$V_{CE} = V_{CC} - V_E$$

$$V_{CE} = V_{CC} - I_E R_E \tag{5–15}$$

The collector-to-base voltage is

$$V_{CB} = V_{CC} - V_E - V_{BE} \tag{5–16}$$

V_{CB}

Example 5–7

Determine I_B, I_C, I_E, and the voltage at each transistor terminal with respect to ground (V_E, V_B, and V_C) in Figure 5–21. β_{dc} is 200.

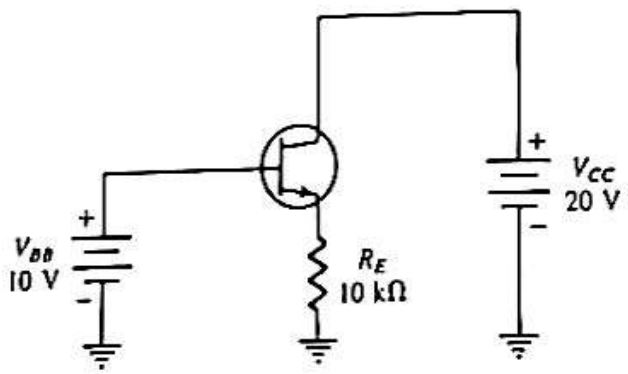


FIGURE 5–21

Solution:

$$I_E = \frac{V_{BB} - V_{BE}}{R_E} = \frac{10\text{ V} - 0.7\text{ V}}{10\text{ k}\Omega} = 0.93\text{ mA}$$

$$I_C \cong I_E = 0.93\text{ mA}$$

$$I_B \cong \frac{I_E}{\beta_{dc}} = \frac{0.93\text{ mA}}{200} = 4.65\ \mu\text{A}$$

$V_C = V_{CC} = 20$ V

$V_B = V_{BB} = 10$ V

$V_E = I_E R_E = (0.93 \text{ mA})(10 \text{ k}\Omega) = 9.3$ V

The results are shown in Figure 5–22.

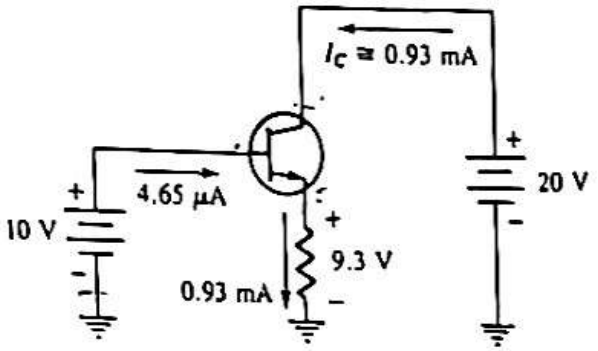


FIGURE 5–22

Review for 5–6

1. A transistor in a particular common-collector configuration has a β_{dc} equal to 90 and a base current of 2 μA. What is the approximate emitter current?
2. In a certain npn common-collector circuit, $V_E = 4.3$ V and $V_{CC} = 12$ V. Determine V_C and V_B.

5–7 TRANSISTOR PARAMETERS AND RATINGS

More about β_{dc}

The β_{dc} is a very important bipolar transistor parameter and we need to examine it further. β_{dc} varies with both collector current and temperature. Keeping the junction temperature constant and increasing I_C causes β_{dc} to increase to a maximum. A further increase in I_C beyond this maximum point causes β_{dc} to decrease.

If I_C is held constant and the temperature is varied, β_{dc} changes directly with the temperature. If the temperature goes up, β_{dc} goes up and vice versa. Figure 5–24 shows the variation of β_{dc} with I_C and junction temperature (T_J) for a typical transistor.

A transistor data sheet usually specifies β_{dc} (h_{FE}) at specific I_C values. Even at fixed values of I_C and temperature, β_{dc} varies from device to device for a given transistor.

The β_{dc} specified at a certain value of I_C is usually the minimum value, $\beta_{dc(min)}$, although the maximum and typical values are also sometimes specified. A typical transistor data sheet is shown in Figure 5–23.

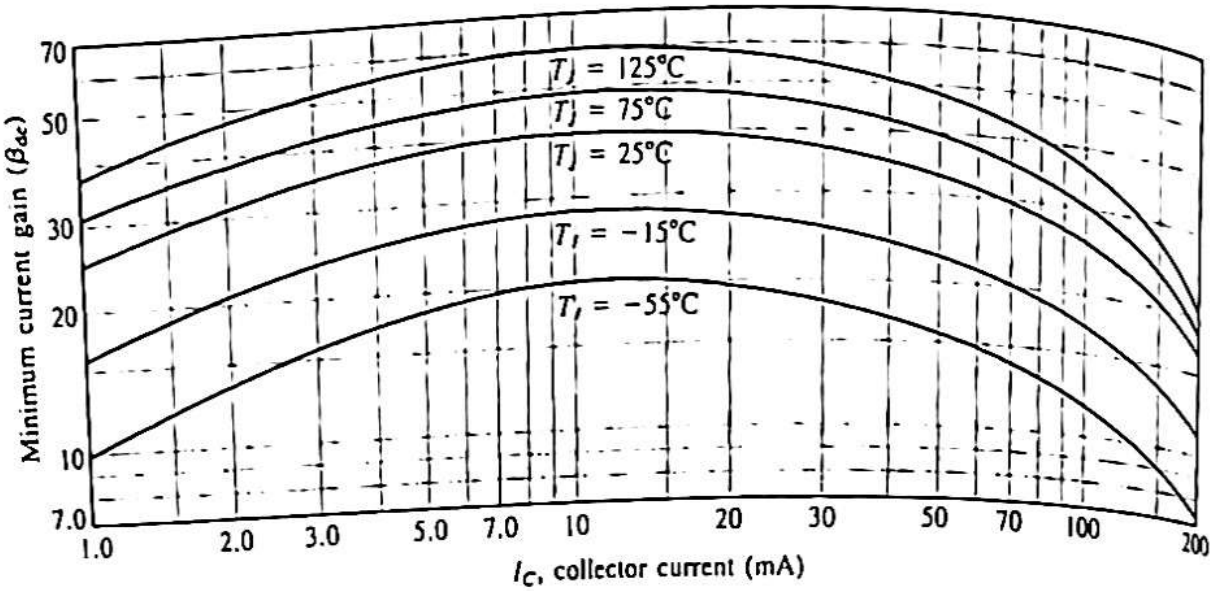


FIGURE 5–24 *Variation of β_{dc} with I_C for several temperatures.*

Maximum Ratings

The transistor, like any other electronic device, has limitations on its operation. These limitations are stated in the form of *maximum ratings* and are normally specified on the manufacturer's data sheet.

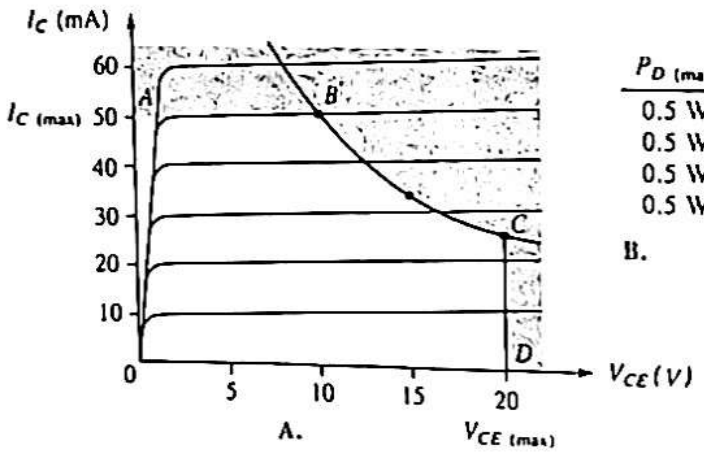
Typically, maximum ratings are given for *collector-to-base voltage, collector-to-emitter voltage, emitter-to-base voltage, collector current,* and *power dissipation.*

The product of V_{CE} and I_C must not exceed the maximum power dissipation. Both V_{CE} and I_C cannot be maximum at the same time. If V_{CE} is maximum, I_C can be calculated as

$$I_C = \frac{P_{D(max)}}{V_{CE}} \tag{5–17}$$

If I_C is maximum, V_{CE} can be calculated by rearranging equation (5–17) as follows:

$$V_{CE} = \frac{P_{D(max)}}{I_C} \tag{5–18}$$



$P_{D\,(max)}$	V_{CE}	I_C
0.5 W	5 V	0.1 A
0.5 W	10 V	0.05 A
0.5 W	15 V	0.033 A
0.5 W	20 V	0.025 A

B.

FIGURE 5–25 *Maximum power dissipation curve.*

For a given transistor, a maximum power dissipation curve can be plotted on the collector curves, as shown in Figure 5–25A. These values are tabulated in part B. The $P_{D(max)}$ for this transistor is 0.5 W, $V_{CE(max)}$ is 20 V, and $I_{C(max)}$ is 50 mA.

The curve shows that this particular transistor cannot be operated in the shaded portion of the graph. $I_{C(max)}$ is the limiting rating between points A and B, $P_{D(max)}$ is the limiting rating between points B and C, and $V_{CE(max)}$ is the limiting rating between points C and D.

Example 5–8

A certain transistor is to be operated with $V_{CE} = 6$ V. If its maximum power rating is 0.25 W, what is the most collector current that it can withstand?

Solution:

$$I_C = \frac{P_{D(max)}}{V_{CE}} = \frac{0.25 \text{ W}}{6 \text{ V}} = 41.67 \text{ mA}$$

Note that this is not necessarily the maximum I_C. It can handle more collector current if V_{CE} is reduced, as long as $P_{D(max)}$ is not exceeded.

Example 5–9

The silicon transistor in Figure 5–26 has the following maximum ratings: $P_{D(max)} = 0.8$ W, $V_{CE(max)} = 15$ V, $I_{C(max)} = 100$ mA, $V_{CB(max)} = 20$ V, and $V_{EB(max)} = 10$ V. Determine the maximum value to which V_{CC} can be adjusted without exceeding a rating. Which rating would be exceeded first?

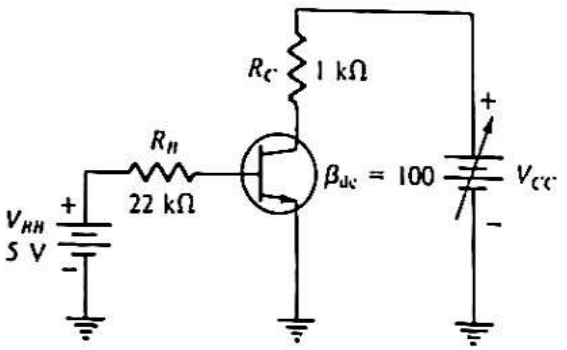


FIGURE 5–26

Solution:

First find I_B so that I_C can be determined.

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{5 \text{ V} - 0.7 \text{ V}}{22 \text{ k}\Omega} = 195.5 \ \mu\text{A}$$

$$I_C = \beta_{dc} I_B = (100)(195.5 \ \mu\text{A}) = 19.55 \text{ mA}$$

Example 5–9 (continued)

I_C is much less than $I_{C(max)}$ and will not change with V_{CC}. It is determined only by I_B and β_{dc}.

The voltage drop across R_C is

$$V_{R_C} = I_C R_C = (19.55 \text{ mA})(1 \text{ k}\Omega) = 19.55 \text{ V}$$

Now we can determine the value of V_{CC} when $V_{CE} = V_{CE(max)} = 15$ V.

$$V_{R_C} = V_{CC} - V_{CE}$$

$$\text{So } V_{CC(max)} = V_{CE(max)} + V_{R_C}$$

$$= 15 \text{ V} + 19.55 \text{ V}$$

$$= 34.55 \text{ V}$$

V_{CC} can be increased to 34.55 V, under the existing conditions, before $V_{CE(max)}$ is exceeded. However, we do not know whether or not $P_{D(max)}$ has been exceeded at this point. Let's find out.

$$P_D = V_{CE(max)} I_C = (15 \text{ V})(19.55 \text{ mA}) = 0.293 \text{ W}$$

Since $P_{D(max)}$ is 0.8 W, it is *not* exceeded when $V_{CE} = 34.55$ V. So, $V_{CE(max)}$ is the limiting rating in this case.

It should be noted that if the base current is removed causing the transistor to turn off, $V_{CE(max)}$ will be exceeded because the entire supply voltage, V_{CC}, will be dropped across the transistor.

Derating $P_{D(max)}$

$P_{D(max)}$ is usually specified at 25°C. For higher temperatures, $P_{D(max)}$ is less. Data sheets often give *derating factors* for determining $P_{D(max)}$ at any temperature above 25°C.

For example, a derating factor of 2 mW/°C indicates that the maximum power dissipation is reduced 2 mW for each °C *increase* in temperature.

Example 5–10

A certain transistor has a $P_{D(max)}$ of 1 W at 25°C. The derating factor is 5 mW/°C. What is the $P_{D(max)}$ at a temperature of 70°C?

Solution:

The change (reduction) in $P_{D(max)}$ is

$$\Delta P_{D(max)} = (5 \text{ mW/°C})(70°\text{C} - 25°\text{C})$$

$$= (5 \text{ mW/°C})(45°\text{C})$$

$$= 225 \text{ mW}$$

Therefore the $P_{D(max)}$ at 70°C is

$$1 \text{ W} - 225 \text{ mW} = 775 \text{ mW} = 0.775 \text{ W}$$

Review for 5–7

1. The β_{dc} of a transistor increases with temperature (T or F).
2. Generally, what effect does an increase in I_C have on the β_{dc}?
3. What is the allowable collector current in a transistor with $P_{D(max)} = 0.32$ W when $V_{CE} = 8$ V?

5–8

TRANSISTOR TESTING

Ohmmeter Check of Transistor Junctions

The ohmmeter provides a simple test for open or shorted junctions. *The base-emitter and base-collector junctions are each treated as a diode for this test.* The junction should show a *low* resistance when forward-biased and a very *high* resistance when reverse-biased. The internal battery of the ohmmeter must provide the bias voltage.

Figure 5–27A shows a *forward-biased* check of an npn transistor. Notice the polarities of the ohmmeter leads. Part B of the figure demonstrates a *reverse-biased* check. For a pnp transistor, the meter polarities are reversed from those shown in Figure 5–27.

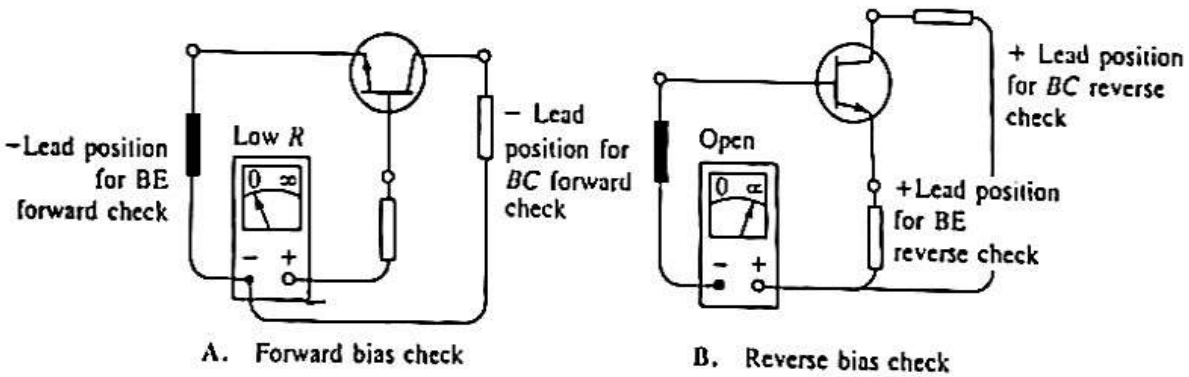


FIGURE 5–27 *Ohmmeter check of npn transistor junctions.*

Leakage Measurement

Very small *leakage* currents exist in all transistors and in most cases are small enough to neglect.